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# Advanced Clock Drivers Device Data Book

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# Advanced Clock Drivers Device Data

## Table of Contents

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# Advanced Clock Drivers Device Data

## FOREWORD

This publication includes technical information for the several product families that comprise Motorola Advanced Clock Drivers products. Motorola's broad portfolio of devices support voltage levels from 2.5 V to 5.0 V in both CMOS I/O and various differential I/O technologies. Advanced Clock Drivers are developed by the Motorola Timing Solutions Operations organization.

All devices are listed in alphanumeric order in the *Device Index* of this book. Just turn to the appropriate page for technical details of the known device.

A *Selector Guide* by product family is provided at the beginning of the book to aid you in identifying devices that meet your application and functional performance requirements.

Complete device specifications are provided in the form of *Data Sheets* which are categorized into the five product types: Clock Generators, Clock Synthesizers, Zero–Delay Buffers, LVCMOS Fanout Buffers, and Differential Fanout Buffers.

Chapters on *Packaging Information* and *Application Notes* include additional information to aid you in the design process.

Refer to the last chapter in this publication for a complete listing of Motorola Authorized Distributors and Worldwide Sales Offices.

The information in this book has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies.



Printed in U.S.A.

## ACCESS ADVANCED CLOCK DRIVERS TECHNICAL INFORMATION ON–LINE

Motorola Semiconductor Products Sector (SPS) has provided a World Wide Web Server to deliver Motorola SPS technical data to the global Internet community. Technical data (for example, data sheets, application notes, and selector guides) is available on the Internet server with full, easy text search capabilities. Ordering literature from the Literature Center is available on–line. Other features of the Motorola SPS Internet server include the availability of a searchable press release database, technical training information with on–line registration capabilities, an on–line technical support form to send technical questions and receive answers through email, information on product groups, full search capabilities of device models, a listing of authorized distributors, and links directly to other Motorola World Wide Web servers. The Motorola SPS URL is **www.motorola.com/semiconductors/**

To access Motorola Timing Solutions Operations information, use either of the following URLs:

**http://www.motorola.com/AdvancedClockDrivers**
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## TO REPLACE DEVICES IN AN EXISTING DESIGN

Call your local Motorola sales office or distributor to determine Motorola's closest replacement device (see Chapter 9).

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Applications assistance is available from your nearest Motorola semiconductor sales office or by calling 1–800–521–6274.

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Silicon Harbour Centre
2 Dai King Street, Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
Phone: 852–26668334

# Device Index

# Chapter One

# Advanced Clock Drivers Selector Guide



The Advanced Clock Drivers products in this Selector Guide are divided into five categories: Clock Generators, Clock Synthesizers, Zero–Delay Buffers, LVCMOS Fanout Buffers, and Differential Fanout Buffers. Clock Characteristic Diagrams are also provided.

**To Replace Devices in an Existing Design**

Call your local Motorola sales office or distributor to determine Motorola's closest replacement device (see Chapter 9).

**Access Data On–Line**

Use the Motorola SPS Internet to access Motorola Semiconductor Product data at **www.motorola.com/semiconductors/**. The SPS Internet provides you with instant access to data sheets, selector guide information, package outlines, on–line technical support and much more.
To access Motorola Timing Solutions Operations information, use either of the following URLs:

**http://www.motorola.com/AdvancedClockDrivers**
**http://www.motorola.com/TimingSolutions**

**Applications Assistance**

Applications assistance is available from your nearest Motorola semiconductor sales office or by calling 1–800–521–6274.

# Clock Generator Reference Table

1

## Introduction

This classification of product uses PLL technology to generate output clocks that are synchronous, and in most cases phase aligned, to an input reference clock. Limited frequency synthesis and zero delay performance is provided.

| Device | Processor and application | Temp. Range (°C) ($T_A$) | VCC (V) | Package | Output frequency range (MHz) | Max output skew (ps) | Max period jitter (ps) | Input | No. of outputs | Status |
|---|---|---|---|---|---|---|---|---|---|---|
| MPC9315 | Telecom/Networking Applications | –40 to 85 | 3.3/ 2.5 | 32 LQFP | 18 to 200 | 120 | ±8 (rms) | 2 selectable LVCMOS | 8 LVCMOS | P |
| MPC9330 | Pentium or PowerPC603/740/750 Class Processor Designs (on–board crystal oscillator) | –40 to 85 | 3.3/ 3.5 | 32 LQFP | 16 to 200 | 150 | TBD | XTAL or LVCMOS | 6 LVCMOS | IN |
| MPC9331 | Pentium or PowerPC603/740/750 Class Processor Designs (faster VCO than 930) | –40 to 85 | 3.3/ 2.5 | 32 LQFP | 16 to 200 | 150 | TBD | LVCMOS or LVPECL | 6 LVCMOS | IN |
| MPC9350 | Networking and Telecommunications Ideal for PowerQUICC II and PowerPC MPC74XX applications | –40 to 85 | 3.3/ 2.5 | 32 LQFP | 25 to 200 | 200 | —— | XTAL or LVCMOS | 9 LVCMOS | S |
| MPC9351 | Networking and Telecommunications Ideal for PowerQUICC II and PowerPC MPC74XX applications | –40 to 85 | 3.3/ 2.5 | 32 LQFP | 25 to 200 | 100 | —— | LVCMOS or LVPECL | 9 LVCMOS | P |
| MPC9352 | General Purpose or RISC/CSIC Class Processor Designs | –40 to 85 | 3.3/ 2.5 | 32 LQFP | 16 to 200 | 150 | TBD | LVCMOS | 11 LVCMOS | IN |
| MPC9600 | General purpose 2.5 V, high fanout zero delay buffer | –40 to 85 | 3.3/ 2.5 | 48 LQFP | 25 to 200 | 150 | 50 | LVCMOS or LVPECL | 21 LVCMOS | P |
| MPC9772 | General Purpose or RISC/CSIC Class Designs (independent output enable/disable “lo–power” scheme) | 0 to 70 | 3.3/ 2.5 | 52 LQFP | 25 to 200 | 300 | TBD | XTAL or LVCMOS | 12 LVCMOS | IN |
| MPC9773 | Pentium or PowerPC603/740/750 Class Designs (output enable/disable “lo–power” scheme) | 0 to 70 | 3.3/ 2.5 | 52 LQFP | 25 to 200 | 300 | TBD | LVCMOS or LVPECL | 12 LVCMOS | IN |
| MPC9774 | Fault Tolerant (redundant Clock Source needed) Pentium/PowerPC603/740/750/RISC Class Processor Design | 0 to 70 | 3.3/ 2.5 | 52 LQFP | 25 to 200 | 300 | TBD | LVCMOS | 15 LVCMOS | IN |
| MPC9893 | Systems with clock redundancy needs (high–end computing and telecomm), FAILOVER Clock | –40 to 85 | 3.3/ 2.5 | 48 LQFP | 25 – 200 | TBD | TBD | LVCMOS | 9 LVCMOS | IN |
| MPC9990 | IA64, HSTL Clock Generator | 0 to 70 | 3.3/ 2.5 | 48 LQFP | 75 to 300 | 50 | 75 | LVPECL | 10 HSTL + feedback | IN |
| MPC9991 | Telecom Applications, Work Station, Mainframe (differential input locks onto external clock reference) | –40 to 85 | 3.3/ 2.5 | 52 LQFP | 25 – 400 | 150 | TBD | LVPECL | 14 Differential Pairs | IN |
| MPC9992 | Pentium or PowerPC603/740/750 Class Designs (output enable/disable “lo–power” scheme) | –40 to 85 | 3.3/ 2.5 | 32 LQFP | 20 – 400 | 150 | TBD | LVPECL or XTAL | 7 Differential Pairs | IN |
| MPC9993 | Systems with clock redundancy needs (high–end computing and telecomm) Differential LVPECL 50 MHz to 90 MHz input frequency | –40 to 85 | 3.3/ 2.5 | 32 LQFP | 50 – 200 | 150 | TBD | LVPECL | 5 Differential Pairs | IN |
| MC88915TFN55 | PC, Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom | –40 to 85 | 5.0 | 28 PLCC | 55 | 500 | —— | CMOS | 8 LVCMOS | P |

**Legend:**
IN = In Development (TARGET specifications)  P = Production (FINAL specifications)  S = Sampling (PRELIM specifications)

# Clock Generator Reference Table (continued)



| Device | Processor and application | Temp. Range (°C) ($T_A$) | VCC (V) | Package | Output frequency range (MHz) | Max output skew (ps) | Max period jitter (ps) | Input | No. of outputs | Status |
|---|---|---|---|---|---|---|---|---|---|---|
| MC88915TFN70 | PC, Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom | –40 to 85 | 5.0 | 28 PLCC | 70 | 500 | —— | CMOS | 8 LVCMOS | P |
| MC88915TFN100 | PC, Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom | –40 to 85 | 5.0 | 28 PLCC | 100 | 500 | —— | CMOS | 8 LVCMOS | P |
| MC88915TFN133 | PC, Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom | –40 to 85 | 5.0 | 28 PLCC | 133 | 500 | —— | CMOS | 8 LVCMOS | P |
| MC88915TFN160 | PC, Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom | 0 to 70 | 5.0 | 28 PLCC | 160 | 500 | —— | CMOS | 8 LVCMOS | P |

**Legend:**
IN = In Development (TARGET specifications)  P = Production (FINAL specifications)  S = Sampling (PRELIM specifications)

# Clock Synthesizer Reference Table

1

## Introduction

This classification of products uses PLL technology to synthesize high frequency clocks from low cost crystal sources. Programmable frequency steps are typically 1 MHz or less with output frequencies as high as 800 MHz.

| Device | Processor and application | Temp. Range (°C) ($T_A$) | VCC (V) | Package | Output frequency range (MHz) | Max period jitter (ps) | Input | Outputs | Status |
|---|---|---|---|---|---|---|---|---|---|
| MPC9229 | Clock source for 25 MHz to 450 MHz processor designs (serial and/or parallel) 1 MHz steps | 0 to 70 | 3.3 | 28 PLCC<br>32 LQFP | 450 MHz | 25 | XTAL | LVPECL | IN |
| MPC9230 | Clock source for 50 MHz to 900 MHz processor designs (serial and/or parallel) 1 MHz steps | 0 to 70 | 3.3 | 28 PLCC<br>32 LQFP | 900 MHz | 25 | XTAL<br>or<br>LVCMOS | LVPECL | IN |
| MPC9239 | Clock source for 50 MHz to 900 MHz processor designs (serial and/or parallel) 16.66 MHz steps | 0 to 70 | 3.3 | 28 PLCC | 900 MHz | 25 | XTAL<br>or<br>LVCMOS | LVPECL | IN |

**Legend:**

IN = In Development (TARGET specifications)  P = Production (FINAL specifications)  S = Sampling (PRELIM specifications)

# Zero-Delay Buffer Reference Table

## Introduction

This classification of products uses PLL technology to reproduce exact copies, in frequency and phase, of the input reference clock. These specialized products provide superior AC performance to clock generators, but lack any frequency synthesis capabilities.



| Device | Processor and application | Temp. Range (°C) ($T_A$) | VCC (V) | Package | Output frequency range (MHz) | Max output skew (ps) | Max period jitter (ps) | Input | Outputs | Status |
|---|---|---|---|---|---|---|---|---|---|---|
| MPC9608 | General Purpose Zero–delay applications, Companion to PowerQUICK and PPC designs, DRAM applications | –40 to 85 | 3.3/ 2.5 | 32 LQFP | 12.5 to 200 | 150 | 10 (RMS) | LVCMOS | 10 LVCMOS | IN |
| MPC9653 | High Performance Clock Tree Design, PC100SDRAM | –40 to 85 | 3.3/ 2.5 | 32 LQFP | 200 | 150 | TBD | LVPECL Ref LVCMOS fdbk | 8 + feedback LVCMOS | IN |
| MPC9658 | Very High Performance Clock Tree Design up to 200 MHz, PC100SDRAM | –40 to 85 | 3.3/ 2.5 | 32 LQFP | 200 | 150 | TBD | LVPECL Ref LVCMOS fdbk | 10 + feedback LVCMOS | IN |
| MPC961C | General Purpose also PowerQUICC: Zero–delay applications (CMOS clock signal retiming without insertion delay) DRAM driver | –40 to 85 | 3.3/ 2.5 | 32 LQFP | 50 to 200 | 150 | 10 (RMS) | LVCMOS Ref LVCMOS fdbk | 17 + feedback LVCMOS | P |
| MPC961P | Zero–delay applications (PECL clock signal retiming without insertion delay) | –40 to 85 | 3.3/ 2.5 | 32 LQFP | 50 to 200 | 150 | 10 (RMS) | LVPECL Ref LVCMOS fdbk | 17 + feedback LVCMOS | P |
| MPC9857V | Clock driver for 184–pin DDR SDRAM Modules | 0 to 70 | 2.5 | 48 TSSOP | 167 | 100 | —— | SSTL2 | 11 SSTL2 | IN |

**Legend:**

IN = In Development (TARGET specifications)  P = Production (FINAL specifications)  S = Sampling (PRELIM specifications)

# LVCMOS Fanout Buffer Reference Table

## Introduction

1

This classification of product uses digital circuitry to produce multiple copies of its input clock. In some cases the output frequencies will be divided down versions of the input clock.

| Device | Processor and application | Temp. Range (°C) (Ambient) | VCC (V) | Package | Max output frequency (MHz) | Max output skew (ps) | Max part–part skew (ns) | Input | Outputs | Status |
|---|---|---|---|---|---|---|---|---|---|---|
| MPC905 | Pentium PCI Processor Bus Clock or PCI Bus Hi–Speed Transmission Line Driver | 0 to 70 | 3.3 | 16 SOIC | 100 | 500 | —— | XTAL or external LVCMOS | 6 | P |
| MPC940L | General Purpose or RISC/CSIC PCI Clock Distribution to Synchronous Memory (better performance than MPC9109) | 0 to 70 | 3.3/ 2.5 | 32 QFP/ LQFP | 250 | 150 | 1.7 | LVPECL or LVCMOS | 18 | P |
| MPC941 | General Purpose or RISC/CSIC PCI Clock Distribution to Synchronous Memory (more outputs than MPC940) | –40 to 85 | 3.3/ 2.5 | 48 QFP | 250 | 250 | 1.2 | LVPECL or LVCMOS | 27 | P |
| MPC942C | Pentium II and other high performance synchronous designs (CMOS inputs) | 0 to 70 | 3.3/ 2.5 | 32 LQFP | 250 | 250 | 1 | LVTTL or LVCMOS | 18 | P |
| MPC942P | Pentium II and other high performance synchronous designs (PECL inputs) | 0 to 70 | 3.3/ 2.5 | 32 LQFP | 250 | 250 | 1 | LVPECL | 18 | P |
| MPC9443 | Low Voltage High–performance Telecom, Networking and computing Applications | –40 to 85 | 3.3/ 2.5 † | 48 LQFP | 250 | 200 | —— | LVPECL or LVCMOS | 16 | S |
| MPC9446 | Low Voltage Mid–range and High–performance Telecom, Networking and Computing Applications | –40 to 85 | 3.3/ 2.5 † | 32 LQFP | 250 | 200 | —— | LVCMOS | 10 | S |
| MPC9447 | General Purpose or RISC/CSIC Class Processor Clock Fanout for L2 Cache | –40 to 85 | 3.3/ 2.5 | 32 LQFP | 275 | 150 | TBD | LVTTL | 9 | IN |
| MPC9448 | General Purpose or RISC/CSIC Class Processor Clock Fanout for L2 Cache (faster & more outputs than the MPC947) | –40 to 85 | 3.3/ 2.5 | 32 LQFP | 275 | 150 | TBD | LVPECL or LVCMOS | 12 | IN |
| MPC9449 | General Purpose or RISC/CSIC Class Processor PCI Clock Distribution to Synch Memory (5 more outputs than the MPC946) | –40 to 85 | 3.3/ 2.5 | 32 LQFP | 200 | 200 | TBD | LVPECL or LVCMOS | 15 | IN |
| MPC9456 | Low Voltage Mid–range and High–performance Telecom, Networking and Computing Applications | –40 to 85 | 3.3/ 2.5 † | 32 LQFP | 250 | 250 | —— | LVPECL | 10 | IN |

† Supports single and mixed mode power supply

**Legend:**

IN = In Development (TARGET specifications)  P = Production (FINAL specifications)  S = Sampling (PRELIM specifications)

# Differential Fanout Buffer Reference Table

## Introduction

This classification of product uses digital circuitry to produce multiple copies of its input clock. In some cases the output frequencies will be divided down versions of the input clock.



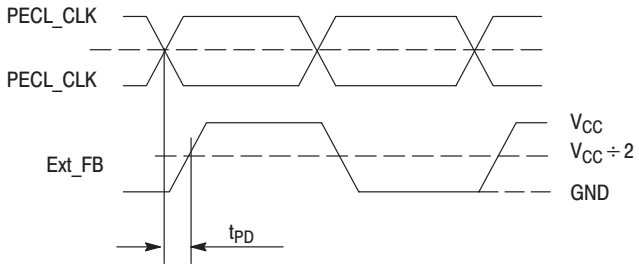
| Device | Processor and application | Temp. Range (°C) ($T_J$) | VCC (V) | Package | Max part–part skew | Max output Skew (ps) | Output technology | Input | Outputs | Status |
|---|---|---|---|---|---|---|---|---|---|---|
| MC100ES6111 | Clock distribution schemes requiring “very low” part–to–part and output–to–output skews | 0 to 110 | 3.3/ 2.5 | 32 LQFP | TBD | 35 | 3 GHz LVPECL | ECL/ LVPECL or HSTL | 1:10 | IN |
| MC100ES6210 | Clock distribution schemes requiring “very low” part–to–part and output–to–output skews | 0 to 110 | 3.3/ 2.5 | 32 LQFP | TBD | 35 | 3 GHz LVPECL | ECL/ LVPECL | Dual 1:5 | S |
| MC100ES6220 | LV/PECL Designs needing low skew. Telecom Back-Bone Equipment, Semi Test Equipment | 0 to 110 | 3.3/ 2.5 | 52 LQFP exposed pad | TBD | 50 | 3 GHz LVPECL | ECL/ LVPECL | Dual 1:10 DIFF | IN |
| MC100ES6221 | LV/PECL Designs needing low skew. Telecom Back-Bone Equipment, Semi Test Equipment | 0 to 110 | 3.3/ 2.5 | 52 LQFP exposed pad | TBD | 50 | 3 GHz LVPECL | ECL/ LVPECL | 1:20 DIFF | IN |
| MC100ES6222 | LV/PECL Designs needing low skew. Telecom Back-Bone Equipment, Semi Test Equipment | 0 to 110 | 3.3/ 2.5 | 52 LQFP exposed pad | TBD | 50 | 3 GHz LVPECL | ECL/ LVPECL | 1:15 DIFF | IN |
| MC100ES6226 | Clock distribution schemes requiring “extremely low” part–to–part and output–to–output skews | 0 to 110 | 3/ 2.5 | 32 LQFP | TBD | 35 | 3 GHz LVPECL | LVPECL | 1:9 | P |
| MC100ES6254 | Differential 2x2 clock switch and Fanout Buffer | 0 to 110 | 3/ 2.5 | 32 LQFP | TBD | 35 | 3 GHz LVPECL | LVPECL | Single 1:6 or Double 1:3 | S |
| MC100EP8111 | Clock distribution schemes requiring “extremely low” part–to–part and output–to–output skews | –40 to 85 ($T_A$) | 3.3 | 32 LQFP | 200 | 50 | HSTL | HSTL or LVPECL | 1:10 | S |
| MC100ES8223 | ECL/PECL Designs needing low skew. Telecom Back-Bone Equipment, Semi Test Equipment | 0 to 110 | 3.3/ 2.5 | 64 LQFP exposed pad | TBD | 50 | 800 MHz | LVPECL or HSTL | 1:22 DIFF | IN |

**Legend:**

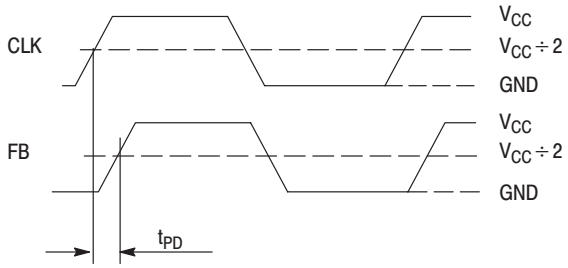
IN = In Development (TARGET specifications)  P = Production (FINAL specifications)  S = Sampling (PRELIM specifications)

# Clock Characteristic Diagrams

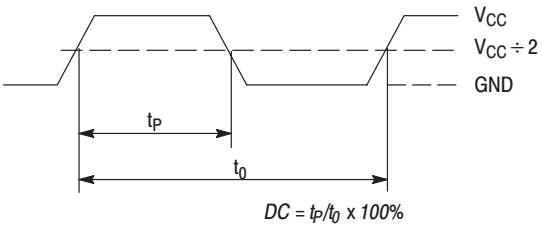





**Propagation delay ($t_{PD}$, static phase offset) test reference (PECL)**

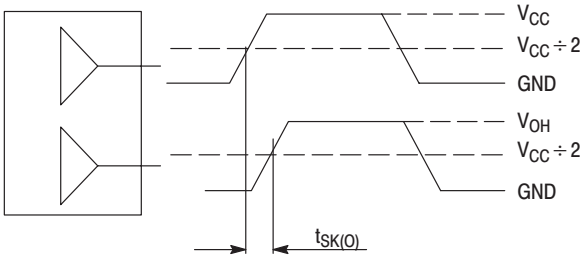



**Propagation delay ($t_{PD}$, static phase offset) test reference (CMOS)**



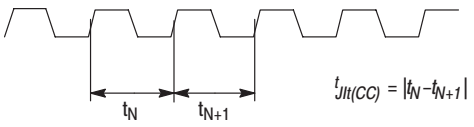

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Output Duty Cycle (DC)**



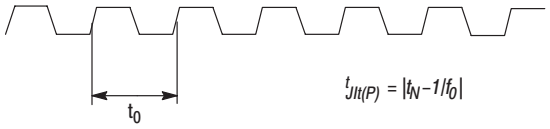

The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Output–to–output Skew $t_{SK(O)}$**



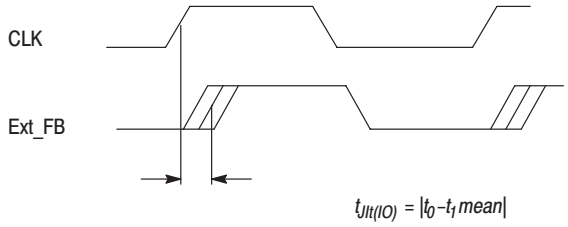

The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

**Cycle–to–cycle Jitter**



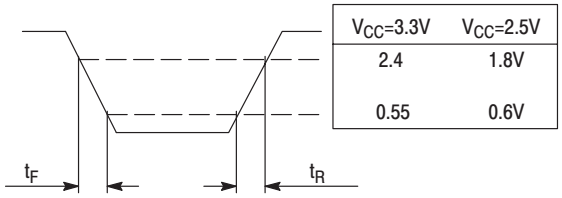

The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

**Period Jitter**




The deviation in $t_0$ for a controlled edge with respect to a $t_0$ mean in a random sample of cycles

**I/O (Phase) Jitter**




**Transition Time Test Reference**

# Chapter Two
# Clock Generator Data Sheets

2

### Clock Generator Device Index

**Order Number: MC88915T/D**
**Rev 5, 08/2001**

**MC88915TFN55**
**MC88915TFN70**
**MC88915TFN100**
**MC88915TFN133**
**MC88915TFN160**

**LOW SKEW CMOS**
**PLL CLOCK DRIVER**

# Low Skew CMOS PLL Clock Drivers, 3-State

## 55, 70, 100, 133 and 160MHz Versions

2

The MC88915T Clock Driver utilizes phase–locked loop technology to lock its low skew outputs' frequency and phase onto an input reference clock. It is designed to provide clock distribution for high performance PC's and workstations. For a 3.3V version, see the MC88LV915T data sheet.

The PLL allows the high current, low skew outputs to lock onto a single clock input and distribute it with essentially zero delay to multiple components on a board. The PLL also allows the MC88915T to multiply a low frequency input clock and distribute it locally at a higher (2X) system frequency. Multiple 88915's can lock onto a single reference clock, which is ideal for applications when a central system clock must be distributed synchronously to multiple boards (see Figure 7).

Five "Q" outputs (Q0–Q4) are provided with less than 500 ps skew between their rising edges. The $\overline{Q5}$ output is inverted (180° phase shift) from the "Q" outputs. The 2X_Q output runs at twice the "Q" output frequency, while the Q/2 runs at 1/2 the "Q" frequency.

The VCO is designed to run optimally between 20 MHz and the 2X_Q $F_{max}$ specification. The wiring diagrams in Figure 5 detail the different feedback configurations which create specific input/output frequency relationships. Possible frequency ratios of the "Q" outputs to the SYNC input are 2:1, 1:1, and 1:2.

The FREQ_SEL pin provides one bit programmable divide–by in the feedback path of the PLL. It selects between divide–by–1 and divide–by–2 of the VCO before its signal reaches the internal clock distribution section of the chip (see the block diagram on page 2). In most applications FREQ_SEL should be held high (÷1). If a low frequency reference clock input is used, holding FREQ_SEL low (÷2) will allow the VCO to run in its optimal range (>20MHz and >40MHz for the TFN133 version).

In normal phase–locked operation the PLL_EN pin is held high. Pulling the PLL_EN pin low disables the VCO and puts the 88915 in a static "test mode". In this mode there is no frequency limitation on the input clock, which is necessary for a low frequency board test environment. The second SYNC input can be used as a test clock input to further simplify board–level testing (see detailed description on page 11).

Pulling the $\overline{OE}/\overline{RST}$ pin low puts the clock outputs 2X_Q, Q0–Q4, $\overline{Q5}$ and Q/2 into a high impedance state (3–state). After the $\overline{OE}/\overline{RST}$ pin goes back high Q0–Q4, $\overline{Q5}$ and Q/2 will be reset in the low state, with 2X_Q being the inverse of the selected SYNC input. Assuming PLL_EN is low, the outputs will remain reset until the 88915 sees a SYNC input pulse.

A lock indicator output (LOCK) will go high when the loop is in steady–state phase and frequency lock. The LOCK output will go low if phase–lock is lost or when the PLL_EN pin is low. The LOCK output will go high no later than 10ms after the 88915 sees a SYNC signal and full 5V $V_{CC}$.

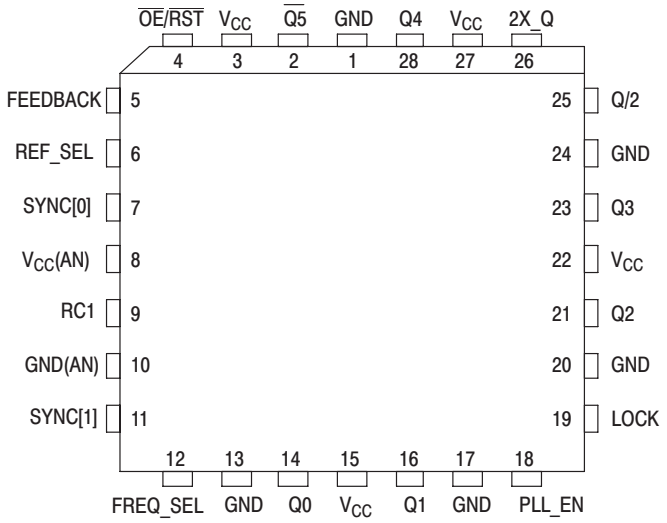
### Features

- Five Outputs (Q0–Q4) with Output–Output Skew < 500 ps each being phase and frequency locked to the SYNC input
- The phase variation from part–to–part between the SYNC and FEEDBACK inputs is less than 550 ps (derived from the $t_{PD}$ specification, which defines the part–to–part skew)
- Input/Output phase–locked frequency ratios of 1:2, 1:1, and 2:1 are available
- Input frequency range from 5MHz – 2X_Q FMAX spec. (10MHz – 2X_Q FMAX for the TFN133 version)
- Additional outputs available at 2X and +2 the system "Q" frequency. Also a $\overline{Q}$ (180° phase shift) output available
- All outputs have ±36 mA drive (equal high and low) at CMOS levels, and can drive either CMOS or TTL inputs. All inputs are TTL–level compatible. ±88mA $I_{OL}/I_{OH}$ specifications guarantee 50Ω transmission line switching on the incident edge
- Test Mode pin (PLL_EN) provided for low frequency testing. Two selectable CLOCK inputs for test or redundancy purposes. All outputs can go into high impedance (3–state) for board test purposes
- Lock Indicator (LOCK) accuracy indicates a phase–locked state



**Rev 5**

**Pinout: 28–Lead PLCC** (Top View)




**FN SUFFIX**
PLASTIC PLCC
CASE 776–02

## PIN SUMMARY

| Pin Name | Num | I/O | Function |
|---|---|---|---|
| SYNC[0] | 1 | Input | Reference clock input |
| SYNC[1] | 1 | Input | Reference clock input |
| REF_SEL | 1 | Input | Chooses reference between sync[0] & Sync[1] |
| FREQ_SEL | 1 | Input | Doubles VCO Internal Frequency (low) |
| FEEDBACK | 1 | Input | Feedback input to phase detector |
| RC1 | 1 | Input | Input for external RC network |
| Q(0–4) | 5 | Output | Clock output (locked to sync) |
| $\overline{Q5}$ | 1 | Output | Inverse of clock output |
| 2x_Q | 1 | Output | 2 x clock output (Q) frequency (synchronous) |
| Q/2 | 1 | Output | Clock output(Q) frequency ÷ 2 (synchronous) |
| LOCK | 1 | Output | Indicates phase lock has been achieved (high when locked) |
| $\overline{OE}/\overline{RST}$ | 1 | Input | Output Enable/Asynchronous reset (active low) |
| PLL_EN | 1 | Input | Disables phase–lock for low freq. testing |
| $V_{CC}$,GND | 11 | | Power and ground pins (note pins 8, 10 are “analog” supply pins for internal PLL only) |

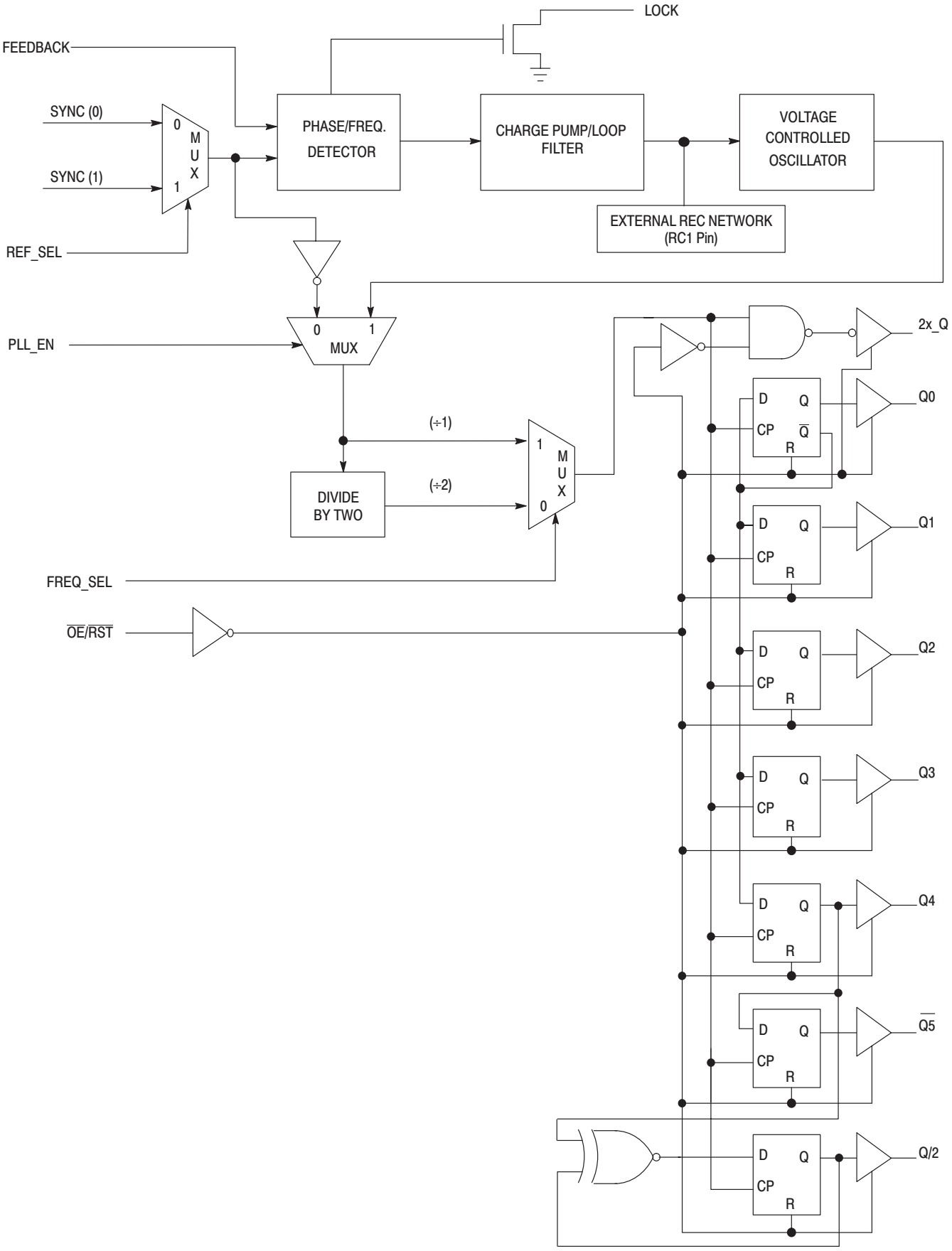



**Figure 1. MC88915T Block Diagram** (All Versions)

# MC88915TFN55 and MC88915TFN70

## SYNC INPUT TIMING REQUIREMENTS

| Symbol | Parameter | Minimum | | Maximum | Unit |
|---|---|---|---|---|---|
| | | TFN70 | TFN55 | | |
| $t_{RISE/FALL}$,SYNC Inputs | Rise/Fall Time, SYNC Inputs From 0.8 to 2.0V | — | — | 3.0 | ns |
| $t_{CYCLE}$, SYNC Inputs | Input Clock Period SYNC Inputs | 28.5 [1] | 36.0 [1] | 200 [2] | ns |
| Duty Cycle SYNC Inputs | Input Duty Cycle SYNC Inputs | 50% ±25% | | | |

1. These $t_{CYCLE}$ minimum values are valid when 'Q' output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 5b.
2. Information in Table 1 and in Note 3 of the AC specification notes describe this specification and its limits depending on what output is fed back, and if FREQ_SEL is high or low.

## DC ELECTRICAL CHARACTERISTICS

(Voltages Referenced to GND) $T_A$ =–40° C to +85° C for 55MHz Version; $T_A$ =0° C to +70° C for 70MHz Version; $V_{CC}$ = 5.0 V ± 5%

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Target Limit | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ – 0.1 V | 4.75<br>5.25 | 2.0<br>2.0 | V |
| $V_{IL}$ | Maximum Low–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ – 0.1 V | 4.75<br>5.25 | 0.8<br>0.8 | V |
| $V_{OH}$ | Minimum High–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = –36 mA [1] | 4.75<br>5.25 | 4.01<br>4.51 | V |
| $V_{OL}$ | Maximum Low–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OL}$ = 36 mA [1] | 4.75<br>5.25 | 0.44<br>0.44 | V |
| $I_{in}$ | Maximum Input Leakage Current | $V_I$ = $V_{CC}$ or GND | 5.25 | ±1.0 | µA |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | $V_I$ = $V_{CC}$ – 2.1 V | 5.25 | 2.0 [2] | mA |
| $I_{OLD}$ | Minimum Dynamic Output Current [3] | $V_{OLD}$ = 1.0V Max | 5.25 | 88 | mA |
| $I_{OHD}$ | | $V_{OHD}$ = 3.85V Min | 5.25 | –88 | mA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_I$ = $V_{CC}$ or GND | 5.25 | 1.0 | mA |
| $I_{OZ}$ | Maximum 3–State Leakage Current | $V_I$ = $V_{IH}$ or $V_{IL}$;$V_O$ = $V_{CC}$ or GND | 5.25 | ±50 [4] | µA |

1. $I_{OL}$ and $I_{OH}$ are 12mA and –12mA respectively for the LOCK output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration is 2.0ms, one output loaded at a time.
4. Specification value for $I_{OZ}$ is preliminary, will be finalized upon 'MC' status.

## CAPACITANCE AND POWER SPECIFICATIONS

| Symbol | Parameter | Typical Values | Unit | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = 5.0 V |
| $C_{PD}$ | Power Dissipation Capacitance | 40 | pF | $V_{CC}$ = 5.0 V |
| $PD_1$ | Power Dissipation @ 50MHz with 50Ω Thevenin Termination | 23mW/Output<br>184mW/Device | mW | $V_{CC}$ = 5.0 V<br>T = 25°C |
| $PD_2$ | Power Dissipation @ 50MHz with 50Ω Parallel Termination to GND | 57mW/Output<br>456mW/Device | mW | $V_{CC}$ = 5.0 V<br>T = 25° C |

NOTE: $PD_1$ and $PD_2$ mW/Output numbers are for a 'Q' output.

## MC88915TFN55 and MC88915TFN70 (continued)

**FREQUENCY SPECIFICATIONS** ($T_A$ =–40° C to +85° C, $V_{CC}$ = 5.0 V ±5%)

| Symbol | Parameter | Guaranteed Minimum | | Unit |
|---|---|---|---|---|
| | | TFN70 | TFN55 | |
| $f_{max}$ [1] | Maximum Operating Frequency (2X_Q Output) | 70 | 55 | MHz |
| | Maximum Operating Frequency (Q0–Q4,$\overline{Q5}$ Output) | 35 | 27.5 | MHz |

1. Maximum Operating Frequency is guaranteed with the part in a phase–locked condition, and all outputs loaded with 50Ω terminated to $V_{CC}$/2.

**AC CHARACTERISTICS** ($T_A$ =–40° C to +85° C, $V_{CC}$ = 5.0V ±5%, Load = 50Ω Terminated to $V_{CC}$/2)

| Symbol | Parameter | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $t_{RISE/FALL}$ Outputs | Rise/Fall Time, All Outputs (Between 0.2$V_{CC}$ and 0.8$V_{CC}$) | 1.0 | 2.5 | ns | Into a 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{RISE/FALL}$[1] 2X_Q Output | Rise/Fall Time Into a 20pF Load, With Termination Specified in Note [2] | 0.5 | 1.6 | ns | $t_{RISE}$: 0.8V – 2.0V<br>$t_{FALL}$: 2.0V – 0.8V |
| $t_{PULSE\ WIDTH}$[1] (Q0–Q4, $\overline{Q5}$, Q/2) | Output Pulse Width: Q0, Q1, Q2, Q3, Q4, $\overline{Q5}$, Q/2 @ $V_{CC}$/2 | 0.5$t_{CYCLE}$ – 0.5 [2] | 0.5$t_{CYCLE}$ + 0.5 [2] | ns | Into a 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{PULSE\ WIDTH}$[1] (2X_Q Output) | Output Pulse Width: 66MHz<br>2X_Q @ 1.5V 50MHz<br>40MHz | 0.5$t_{CYCLE}$ – 0.5 [2]<br>0.5$t_{CYCLE}$ – 1.0<br>0.5$t_{CYCLE}$ – 1.5 | 0.5$t_{CYCLE}$ + 0.5 [2]<br>0.5$t_{CYCLE}$ + 1.0<br>0.5$t_{CYCLE}$ + 1.5 | ns | Must Use Termination Specified in Note **2** |
| $t_{PULSE\ WIDTH}$[1] (2X_Q Output) | Output Pulse Width: 50–65MHz<br>2X_Q @ $V_{CC}$/2 40–49MHz<br>66–70MHz | 0.5$t_{CYCLE}$ – 1.0 [2]<br>0.5$t_{CYCLE}$ – 1.5<br>0.5$t_{CYCLE}$ – 0.5 | 0.5$t_{CYCLE}$ + 1.0 [2]<br>0.5$t_{CYCLE}$ + 1.5<br>0.5$t_{CYCLE}$ + 0.5 | ns | Into a 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{PD}$ [1,3] SYNC Feedback | SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins) | (With 1MΩ from RC1 to An $V_{CC}$) | | ns | See Note **4** and Figure 2 for Detailed Explanation |
| | | –1.05 | –0.40 | | |
| | | (With 1MΩ from RC1 to An GND) | | | |
| | | +1.25 | +3.25 | | |
| $t_{SKEWr}$ [1,4] (Rising) See Note [5] | Output–to–Output Skew Between Outputs Q0–Q4, Q/2 (Rising Edges Only) | — | 500 | ps | All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{SKEWf}$ [1,4] (Falling) | Output–to–Output Skew Between Outputs Q0–Q4 (Falling Edges Only) | — | 500 | ps | All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{SKEWall}$[1,4] | Output–to–Output Skew 2X_Q, Q/2, Q0–Q4 Rising, $\overline{Q5}$ Falling | — | 750 | ps | All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{LOCK}$[5] | Time Required to Acquire Phase–Lock From Time SYNC Input Signal is Received | 1.0 | 10 | ms | Also Time to LOCK Indicator High |
| $t_{PZL}$[6] | Output Enable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2 | 3.0 | 14 | ns | Measured With the PLL_EN Pin Low |
| $t_{PHZ}$,$t_{PLZ}$[6] | Output Disable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2 | 3.0 | 14 | ns | Measured With the PLL_EN Pin Low |

1. These specifications are not tested, they are guaranteed by statistcal characterization. See AC specification Note 1.
2. $T_{CYCLE}$ in this spec is 1/Frequency at which the particular output is running.
3. The $T_{PD}$ specification's min/max values may shift closer to zero if a larger pullup resistor is used.
4. Under equally loaded conditions and at a fixed temperature and voltage.
5. With $V_{CC}$ fully powered–on, and an output properly connected to the FEEDBACK pin. $t_{LOCK}$ maximum is with C1 = 0.1µF, $t_{LOCK}$ minimum is with C1 = 0.01µF.
6. The $t_{PZL}$, $t_{PHZ}$, $t_{PLZ}$ minimum and maximum specifications are estimates, the final guaranteed values will be available when 'MC' status is reached.

## MC88915TFN100

### SYNC INPUT TIMING REQUIREMENTS

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{RISE/FALL}$,SYNC Inputs | Rise/Fall Time, SYNC Inputs From 0.8 to 2.0V | — | 3.0 | ns |
| $t_{CYCLE}$, SYNC Inputs | Input Clock Period SYNC Inputs | 20.0 [1] | 200 [2] | ns |
| Duty Cycle SYNC Inputs | Input Duty Cycle SYNC Inputs | 50% ±25% | | |

1. These $t_{CYCLE}$ minimum values are valid when 'Q' output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 5b.
2. Information in Table 1 and in Note 3 of the AC specification notes describe this specification and its limits depending on what output is fed back, and if FREQ_SEL is high or low.

2

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND) $T_A$ =–40° C to +85° C, $V_{CC}$ = 5.0 V ± 5%

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Target Limit | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ – 0.1 V | 4.75<br>5.25 | 2.0<br>2.0 | V |
| $V_{IL}$ | Maximum Low–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ – 0.1 V | 4.75<br>5.25 | 0.8<br>0.8 | V |
| $V_{OH}$ | Minimum High–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = –36 mA [1] | 4.75<br>5.25 | 4.01<br>4.51 | V |
| $V_{OL}$ | Maximum Low–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OL}$ = 36 mA [1] | 4.75<br>5.25 | 0.44<br>0.44 | V |
| $I_{in}$ | Maximum Input Leakage Current | $V_I$ = $V_{CC}$ or GND | 5.25 | ±1.0 | µA |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | $V_I$ = $V_{CC}$ – 2.1 V | 5.25 | 2.0 [2] | mA |
| $I_{OLD}$ | Minimum Dynamic Output Current [3] | $V_{OLD}$ = 1.0V Max | 5.25 | 88 | mA |
| $I_{OHD}$ | | $V_{OHD}$ = 3.85V Min | 5.25 | –88 | mA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_I$ = $V_{CC}$ or GND | 5.25 | 1.0 | mA |
| $I_{OZ}$ | Maximum 3–State Leakage Current | $V_I$ = $V_{IH}$ or $V_{IL}$;$V_O$ = $V_{CC}$ or GND | 5.25 | ±50 [4] | µA |

1. $I_{OL}$ and $I_{OH}$ are 12mA and –12mA respectively for the LOCK output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration is 2.0ms, one output loaded at a time.
4. Specification value for $I_{OZ}$ is preliminary, will be finalized upon 'MC' status.

### CAPACITANCE AND POWER SPECIFICATIONS

| Symbol | Parameter | Typical Values | Unit | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = 5.0 V |
| $C_{PD}$ | Power Dissipation Capacitance | 40 | pF | $V_{CC}$ = 5.0 V |
| $PD_1$ | Power Dissipation @ 50MHz with 50Ω Thevenin Termination | 23mW/Output<br>184mW/Device | mW | $V_{CC}$ = 5.0 V<br>T = 25°C |
| $PD_2$ | Power Dissipation @ 50MHz with 50Ω Parallel Termination to GND | 57mW/Output<br>456mW/Device | mW | $V_{CC}$ = 5.0 V<br>T = 25° C |

NOTE: $PD_1$ and $PD_2$ mW/Output numbers are for a 'Q' output.

### FREQUENCY SPECIFICATIONS ($T_A$ =–40° C to +85° C, $V_{CC}$ = 5.0 V ±5%)

| Symbol | Parameter | Guaranteed Minimum TFN100 | Unit |
|---|---|---|---|
| $f_{max}$ [1] | Maximum Operating Frequency (2X_Q Output) | 100 | MHz |
| | Maximum Operating Frequency (Q0–Q4,$\overline{Q5}$ Output) | 50 | MHz |

1. Maximum Operating Frequency is guaranteed with the part in a phase–locked condition, and all outputs loaded with 50Ω terminated to $V_{CC}$/2.

## MC88915TFN100 (continued)

**AC CHARACTERISTICS** ($T_A$ =–40° C to +85° C, $V_{CC}$ = 5.0V ±5%, Load = 50Ω Terminated to $V_{CC}$/2)

| Symbol | Parameter | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $t_{RISE/FALL}$ Outputs | Rise/Fall Time, All Outputs (Between 0.2$V_{CC}$ and 0.8$V_{CC}$) | 1.0 | 2.5 | ns | Into a 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{RISE/FALL}$[1] 2X_Q Output | Rise/Fall Time Into a 20pF Load, With Termination Specified in Note [2] | 0.5 | 1.6 | ns | $t_{RISE}$: 0.8V – 2.0V<br>$t_{FALL}$: 2.0V – 0.8V |
| $t_{PULSE\ WIDTH}$[1] (Q0–Q4, $\overline{Q5}$, Q/2) | Output Pulse Width: Q0, Q1, Q2, Q3, Q4, $\overline{Q5}$, Q/2 @ $V_{CC}$/2 | 0.5$t_{CYCLE}$ – 0.5 [2] | 0.5$t_{CYCLE}$ + 0.5 [2] | ns | Into a 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{PULSE\ WIDTH}$[1] (2X_Q Output) | Output Pulse Width: 2X_Q @ 1.5V | 0.5$t_{CYCLE}$ – 0.5 [2] | 0.5$t_{CYCLE}$ + 0.5 [2] | ns | Must Use Termination Specified in Note **2** |
| $t_{PULSE\ WIDTH}$[1] (2X_Q Output) | Output Pulse Width: 2X_Q @ $V_{CC}$/2<br>40–49MHz<br>50–65MHz<br>66–100MHz | 0.5$t_{CYCLE}$ – 1.5 [2]<br>0.5$t_{CYCLE}$ – 1.0<br>0.5$t_{CYCLE}$ – 0.5 | 0.5$t_{CYCLE}$ + 1.5 [2]<br>0.5$t_{CYCLE}$ + 1.0<br>0.5$t_{CYCLE}$ + 0.5 | ns | Into a 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{PD}$ [1,3] SYNC Feedback | SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins) | (With 1MΩ from RC1 to An $V_{CC}$) | | ns | See Note **4** and Figure 2 for Detailed Explanation |
| | | –1.05 | –0.30 | | |
| | | (With 1MΩ from RC1 to An GND) | | | |
| | | +1.25 | +3.25 | | |
| $t_{SKEWr}$ [1,4] (Rising) See Note [5] | Output–to–Output Skew Between Outputs Q0–Q4, Q/2 (Rising Edges Only) | — | 500 | ps | All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{SKEWf}$ [1,4] (Falling) | Output–to–Output Skew Between Outputs Q0–Q4 (Falling Edges Only) | — | 500 | ps | All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{SKEWall}$[1,4] | Output–to–Output Skew 2X_Q, Q/2, Q0–Q4 Rising, $\overline{Q5}$ Falling | — | 750 | ps | All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{LOCK}$[5] | Time Required to Acquire Phase–Lock From Time SYNC Input Signal is Received | 1.0 | 10 | ms | Also Time to LOCK Indicator High |
| $t_{PZL}$[6] | Output Enable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2 | 3.0 | 14 | ns | Measured With the PLL_EN Pin Low |
| $t_{PHZ}$,$t_{PLZ}$[6] | Output Disable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2 | 3.0 | 14 | ns | Measured With the PLL_EN Pin Low |

1. These specifications are not tested, they are guaranteed by statistcal characterization. See AC specification Note 1.
2. $T_{CYCLE}$ in this spec is 1/Frequency at which the particular output is running.
3. The $T_{PD}$ specification's min/max values may shift closer to zero if a larger pullup resistor is used.
4. Under equally loaded conditions and at a fixed temperature and voltage.
5. With $V_{CC}$ fully powered–on, and an output properly connected to the FEEDBACK pin. $t_{LOCK}$ maximum is with C1 = 0.1µF, $t_{LOCK}$ minimum is with C1 = 0.01µF.
6. The $t_{PZL}$, $t_{PHZ}$, $t_{PLZ}$ minimum and maximum specifications are estimates, the final guaranteed values will be available when 'MC' status is reached.

## MC88915TFN133

### SYNC INPUT TIMING REQUIREMENTS

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{RISE/FALL}$,SYNC Inputs | Rise/Fall Time, SYNC Inputs From 0.8 to 2.0V | — | 3.0 | ns |
| $t_{CYCLE}$, SYNC Inputs | Input Clock Period SYNC Inputs | 15.0 [1] | 100 [2] | ns |
| Duty Cycle SYNC Inputs | Input Duty Cycle SYNC Inputs | 50% ±25% | | |

1. These $t_{CYCLE}$ minimum values are valid when 'Q' output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 5b.
2. Information in Table 1 and in Note 3 of the AC specification notes describe this specification and its limits depending on what output is fed back, and if FREQ_SEL is high or low.

2

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND) $T_A$ =–40° C to +85° C, $V_{CC}$ = 5.0 V ± 5%

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Target Limit | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ – 0.1 V | 4.75<br>5.25 | 2.0<br>2.0 | V |
| $V_{IL}$ | Maximum Low–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ – 0.1 V | 4.75<br>5.25 | 0.8<br>0.8 | V |
| $V_{OH}$ | Minimum High–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = –36 mA [1] | 4.75<br>5.25 | 4.01<br>4.51 | V |
| $V_{OL}$ | Maximum Low–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OL}$ = 36 mA [1] | 4.75<br>5.25 | 0.44<br>0.44 | V |
| $I_{in}$ | Maximum Input Leakage Current | $V_I$ = $V_{CC}$ or GND | 5.25 | ±1.0 | µA |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | $V_I$ = $V_{CC}$ – 2.1 V | 5.25 | 2.0 [2] | mA |
| $I_{OLD}$ | Minimum Dynamic Output Current [3] | $V_{OLD}$ = 1.0V Max | 5.25 | 88 | mA |
| $I_{OHD}$ | | $V_{OHD}$ = 3.85V Min | 5.25 | –88 | mA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_I$ = $V_{CC}$ or GND | 5.25 | 1.0 | mA |
| $I_{OZ}$ | Maximum 3–State Leakage Current | $V_I$ = $V_{IH}$ or $V_{IL}$;$V_O$ = $V_{CC}$ or GND | 5.25 | ±50 [4] | µA |

1. $I_{OL}$ and $I_{OH}$ are 12mA and –12mA respectively for the LOCK output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration is 2.0ms, one output loaded at a time.
4. Specification value for $I_{OZ}$ is preliminary, will be finalized upon 'MC' status.

### CAPACITANCE AND POWER SPECIFICATIONS

| Symbol | Parameter | Typical Values | Unit | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = 5.0 V |
| $C_{PD}$ | Power Dissipation Capacitance | 40 | pF | $V_{CC}$ = 5.0 V |
| $PD_1$ | Power Dissipation @ 50MHz with 50Ω Thevenin Termination | 23mW/Output<br>184mW/Device | mW | $V_{CC}$ = 5.0 V<br>T = 25°C |
| $PD_2$ | Power Dissipation @ 50MHz with 50Ω Parallel Termination to GND | 57mW/Output<br>456mW/Device | mW | $V_{CC}$ = 5.0 V<br>T = 25° C |

NOTE: $PD_1$ and $PD_2$ mW/Output numbers are for a 'Q' output.

### FREQUENCY SPECIFICATIONS ($T_A$ =–40° C to +85° C, $V_{CC}$ = 5.0 V ±5%)

| Symbol | Parameter | Guaranteed Minimum TFN133 | Unit |
|---|---|---|---|
| $f_{max}$ [1] | Maximum Operating Frequency (2X_Q Output) | 133 | MHz |
| | Maximum Operating Frequency (Q0–Q4,$\overline{Q5}$ Output) | 66 | MHz |

1. Maximum Operating Frequency is guaranteed with the part in a phase–locked condition, and all outputs loaded with 50Ω terminated to $V_{CC}$/2.

## MC88915TFN133 (continued)

**AC CHARACTERISTICS** ($T_A$ =–40° C to +85° C, $V_{CC}$ = 5.0V ±5%, Load = 50Ω Terminated to $V_{CC}$/2)

| Symbol | Parameter | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $t_{RISE/FALL}$ Outputs | Rise/Fall Time, All Outputs (Between 0.2$V_{CC}$ and 0.8$V_{CC}$) | 1.0 | 2.5 | ns | Into a 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{RISE/FALL}$[1] 2X_Q Output | Rise/Fall Time Into a 20pF Load, With Termination Specified in Note [2] | 0.5 | 1.6 | ns | $t_{RISE}$: 0.8V – 2.0V<br>$t_{FALL}$: 2.0V – 0.8V |
| $t_{PULSE\ WIDTH}$[1] (Q0–Q4, $\overline{Q5}$, Q/2) | Output Pulse Width: Q0, Q1, Q2, Q3, Q4, $\overline{Q5}$, Q/2 @ $V_{CC}$/2 | 0.5$t_{CYCLE}$ – 0.5 [2] | 0.5$t_{CYCLE}$ + 0.5 [2] | ns | Into a 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{PULSE\ WIDTH}$[1] (2X_Q Output) | Output Pulse Width: 66–133MHz<br>2X_Q @ 1.5V 40–65MHz | 0.5$t_{CYCLE}$ – 0.5 [2]<br>0.5$t_{CYCLE}$ – 0.9 | 0.5$t_{CYCLE}$ + 0.5 [2]<br>0.5$t_{CYCLE}$ + 0.9 | ns | Must Use Termination Specified in Note **2** |
| $t_{PULSE\ WIDTH}$[1] (2X_Q Output) | Output Pulse Width: 66–133MHz<br>2X_Q @ $V_{CC}$/2 40–65MHz | 0.5$t_{CYCLE}$ – 0.5 [2]<br>0.5$t_{CYCLE}$ – 0.9 | 0.5$t_{CYCLE}$ + 0.5 [2]<br>0.5$t_{CYCLE}$ + 0.9 | ns | Into a 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{PD}$ [1,3] SYNC Feedback | SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins) | (With 1MΩ from RC1 to An $V_{CC}$) | | ns | See Note **4** and Figure 2 for Detailed Explanation |
| | | –1.05 | –0.25 | | |
| | | (With 1MΩ from RC1 to An GND) | | | |
| | | +1.25 | +3.25 | | |
| $t_{SKEWr}$ [1,4] (Rising) See Note [5] | Output–to–Output Skew Between Outputs Q0–Q4, Q/2 (Rising Edges Only) | — | 500 | ps | All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{SKEWf}$ [1,4] (Falling) | Output–to–Output Skew Between Outputs Q0–Q4 (Falling Edges Only) | — | 500 | ps | All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{SKEWall}$[1,4] | Output–to–Output Skew 2X_Q, Q/2, Q0–Q4 Rising, $\overline{Q5}$ Falling | — | 750 | ps | All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{LOCK}$[5] | Time Required to Acquire Phase–Lock From Time SYNC Input Signal is Received | 1.0 | 10 | ms | Also Time to LOCK Indicator High |
| $t_{PZL}$[6] | Output Enable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2 | 3.0 | 14 | ns | Measured With the PLL_EN Pin Low |
| $t_{PHZ}$,$t_{PLZ}$[6] | Output Disable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2 | 3.0 | 14 | ns | Measured With the PLL_EN Pin Low |

1. These specifications are not tested, they are guaranteed by statistcal characterization. See AC specification Note 1.
2. $T_{CYCLE}$ in this spec is 1/Frequency at which the particular output is running.
3. The $T_{PD}$ specification's min/max values may shift closer to zero if a larger pullup resistor is used.
4. Under equally loaded conditions and at a fixed temperature and voltage.
5. With $V_{CC}$ fully powered–on, and an output properly connected to the FEEDBACK pin. $t_{LOCK}$ maximum is with C1 = 0.1µF, $t_{LOCK}$ minimum is with C1 = 0.01µF.
6. The $t_{PZL}$, $t_{PHZ}$, $t_{PLZ}$ minimum and maximum specifications are estimates, the final guaranteed values will be available when 'MC' status is reached.

## MC88915TFN160

### SYNC INPUT TIMING REQUIREMENTS

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{RISE/FALL}$,SYNC Inputs | Rise/Fall Time, SYNC Inputs From 0.8 to 2.0V | — | 3.0 | ns |
| $t_{CYCLE}$, SYNC Inputs | Input Clock Period SYNC Inputs | 12.5 | 100 | ns |
| Duty Cycle SYNC Inputs | Input Duty Cycle SYNC Inputs | 50% ±25% | | |

1. These $t_{CYCLE}$ minimum values are valid when 'Q' output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 5b.
2. Information in Table 1 and in Note 3 of the AC specification notes describe this specification and its limits depending on what output is fed back, and if FREQ_SEL is high or low.



### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND) $T_A$ =0° C to +70° C, $V_{CC}$ = 5.0 V ± 5%

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Target Limit | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ – 0.1 V | 4.75<br>5.25 | 2.0<br>2.0 | V |
| $V_{IL}$ | Maximum Low–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ – 0.1 V | 4.75<br>5.25 | 0.8<br>0.8 | V |
| $V_{OH}$ | Minimum High–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = –36 mA [1] | 4.75<br>5.25 | 4.01<br>4.51 | V |
| $V_{OL}$ | Maximum Low–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OL}$ = 36 mA [1] | 4.75<br>5.25 | 0.44<br>0.44 | V |
| $I_{in}$ | Maximum Input Leakage Current | $V_I$ = $V_{CC}$ or GND | 5.25 | ±1.0 | µA |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | $V_I$ = $V_{CC}$ – 2.1 V | 5.25 | 2.0 [2] | mA |
| $I_{OLD}$ | Minimum Dynamic Output Current [3] | $V_{OLD}$ = 1.0V Max | 5.25 | 88 | mA |
| $I_{OHD}$ | | $V_{OHD}$ = 3.85V Min | 5.25 | –88 | mA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_I$ = $V_{CC}$ or GND | 5.25 | 1.0 | mA |
| $I_{OZ}$ | Maximum 3–State Leakage Current | $V_I$ = $V_{IH}$ or $V_{IL}$;$V_O$ = $V_{CC}$ or GND | 5.25 | ±50 [4] | µA |

1. $I_{OL}$ and $I_{OH}$ are 12mA and –12mA respectively for the LOCK output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration is 2.0ms, one output loaded at a time.
4. Specification value for $I_{OZ}$ is preliminary, will be finalized upon 'MC' status.

### CAPACITANCE AND POWER SPECIFICATIONS

| Symbol | Parameter | Typical Values | Unit | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = 5.0 V |
| $C_{PD}$ | Power Dissipation Capacitance | 40 | pF | $V_{CC}$ = 5.0 V |
| $PD_1$ | Power Dissipation @ 50MHz with 50Ω Thevenin Termination | 15mW/Output<br>120mW/Device | mW | $V_{CC}$ = 5.0 V<br>T = 25°C |
| $PD_2$ | Power Dissipation @ 50MHz with 50Ω Parallel Termination to GND | 57mW/Output<br>456mW/Device | mW | $V_{CC}$ = 5.0 V<br>T = 25° C |

NOTE: $PD_1$ and $PD_2$ mW/Output numbers are for a 'Q' output.

### FREQUENCY SPECIFICATIONS ($T_A$ =0° C to +70° C, $V_{CC}$ = 5.0 V ±5%)

| Symbol | Parameter | Guaranteed Minimum TFN160 | Unit |
|---|---|---|---|
| $f_{max}$ [1] | Maximum Operating Frequency (2X_Q Output) | 160 | MHz |
| | Maximum Operating Frequency (Q0–Q4,$\overline{Q5}$ Output) | 80 | MHz |

1. Maximum Operating Frequency is guaranteed with the part in a phase–locked condition, and all outputs loaded with 50Ω terminated to $V_{CC}$/2.

## MC88915TFN160 (continued)

**AC CHARACTERISTICS** ($T_A$ =0° C to +70° C, $V_{CC}$ = 5.0V ±5%, Load = 50Ω Terminated to $V_{CC}/2$)

| Symbol | Parameter | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $t_{RISE/FALL}$ Outputs | Rise/Fall Time, All Outputs (Between 0.2$V_{CC}$ and 0.8$V_{CC}$) | 1.0 | 2.5 | ns | Into a 50Ω Load Terminated to $V_{CC}/2$ |
| $t_{RISE/FALL}$ 2X_Q Output | Rise/Fall Time | 0.5 | 1.6 | ns | $t_{RISE}$: 0.8V – 2.0V<br>$t_{FALL}$: 2.0V – 0.8V |
| $t_{PULSE\ WIDTH}$ (Q0–Q4, $\overline{Q5}$, Q/2) | Output Pulse Width: Q0, Q1, Q2, Q3, Q4, $\overline{Q5}$, Q/2 @ $V_{CC}/2$ | $0.5t_{CYCLE}$ – 0.5 [2] | $0.5t_{CYCLE}$ + 0.5 [2] | ns | Into a 50Ω Load Terminated to $V_{CC}/2$ |
| $t_{PULSE\ WIDTH}$ (2X_Q Output) | Output Pulse Width: 2X_Q @ $V_{CC}$<br>80MHz<br>100MHz<br>133MHz<br>160MHz | <br>$0.5t_{CYCLE}$ – 0.7<br>$0.5t_{CYCLE}$ – 0.5<br>$0.5t_{CYCLE}$ – 0.5<br>TBD | <br>$0.5t_{CYCLE}$ + 0.7<br>$0.5t_{CYCLE}$ + 0.5<br>$0.5t_{CYCLE}$ + 0.5<br>TBD | ns | |
| $t_{PD}$[1] SYNC Feedback | SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins)<br>133MHz<br>160MHz | (With 1MΩ from RC1 to An $V_{CC}$)<br>–1.05<br>–0.9 | <br>–0.25<br>–0.10 | ns | See Note **2** and Figure 2 for Detailed Explanation |
| $t_{CYCLE}$ (2x_Q Output) | Cycle–to–Cycle Variation<br>133MHz<br>160MHz | $t_{CYCLE}$ – 300ps<br>$t_{CYCLE}$ – 300ps | $t_{CYCLE}$ + 300ps<br>$t_{CYCLE}$ + 300ps | | |
| $t_{SKEWr}$[3] (Rising) See Note **4** | Output–to–Output Skew Between Outputs Q0–Q4, Q/2 (Rising Edges Only) | — | 500 | ps | All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}/2$ |
| $t_{SKEWf}$[3] (Falling) | Output–to–Output Skew Between Outputs Q0–Q4 (Falling Edges Only) | — | 500 | ps | All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}/2$ |
| $t_{SKEWall}$[3] | Output–to–Output Skew 2X_Q, Q/2, Q0–Q4 Rising, $\overline{Q5}$ Falling | — | 750 | ps | All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}/2$ |
| $t_{LOCK}$[4] | Time Required to Acquire Phase–Lock From Time SYNC Input Signal is Received | 1.0 | 10 | ms | Also Time to LOCK Indicator High |
| $t_{PZL}$[5] | Output Enable Time $\overline{OE}/\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2 | 3.0 | 14 | ns | Measured With the PLL_EN Pin Low |
| $t_{PHZ}$,$t_{PLZ}$[5] | Output Disable Time $\overline{OE}/\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2 | 3.0 | 14 | ns | Measured With the PLL_EN Pin Low |

1. $T_{CYCLE}$ in this spec is 1/Frequency at which the particular output is running.
2. The $T_{PD}$ specification's min/max values may shift closer to zero if a larger pullup resistor is used.
3. Under equally loaded conditions and at a fixed temperature and voltage.
4. With $V_{CC}$ fully powered–on, and an output properly connected to the FEEDBACK pin. $t_{LOCK}$ maximum is with C1 = 0.1µF, $t_{LOCK}$ minimum is with C1 = 0.01µF.
5. The $t_{PZL}$, $t_{PHZ}$, $t_{PLZ}$ minimum and maximum specifications are estimates, the final guaranteed values will be available when 'MC' status is reached.

# Applications Information for All Versions



**General AC Specification Notes**

1. Several specifications can only be measured when the MC88915TFN55, 70 and 100 are in phase–locked operation. It is not possible to have the part in phase–lock on ATE (automated test equipment). Statistical characterization techniques were used to guarantee those specifications which cannot be measured on the ATE. MC88915TFN55, 70 and 100 units were fabricated with key transistor properties intentionally varied to create a 14 cell designed experimental matrix. IC performance was characterized over a range of transistor properties (represented by the 14 cells) in excess of the expected process variation of the wafer fabrication area, to set performance limits of ATE testable specifications within those which are to be guaranteed by statistical characterization. In this way all units passing the ATE test will meet or exceed the non–tested specifications limits.
2. These two specs ($t_{RISE/FALL}$ and $t_{PULSE}$ Width 2X_Q output) guarantee that the MC88915T meets the 40MHz and 33MHz MC68040 P–Clock input specification (at 80MHz and 66MHz, respectively). For these two specs to be guaranteed by Motorola, the termination scheme shown below in Figure 1 must be used.
3. The wiring Diagrams and explanations in Figure 5 demonstrate the input and output frequency relationships for three possible feedback configurations. The allowable SYNC input range for each case is also indicated. There are two allowable SYNC frequency ranges, depending whether FREQ_SEL is high or low. Although not shown, it is possible to feed back the $\overline{Q5}$ output, thus creating a 180° phase shift between the SYNC input and the “Q” outputs. Table 1 below summarizes the allowable SYNC frequency range for each possible configuration.

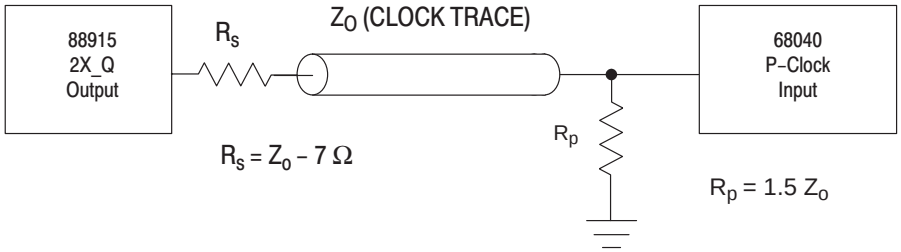
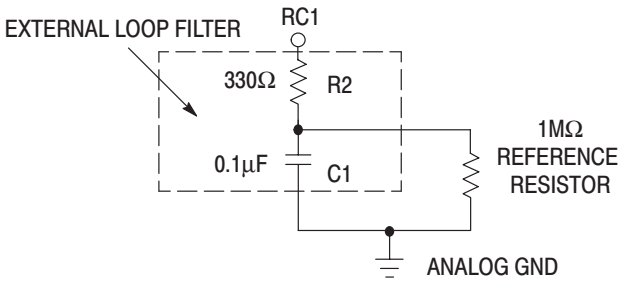


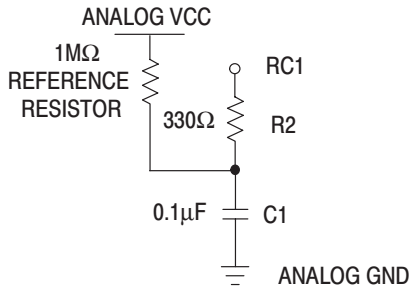

**Figure 1. MC68040 P–Clock Input Termination Scheme**

**Table 1. Allowable SYNC Input Frequency Ranges for Different Feedback Configurations.**

| FREQ_SEL Level | Feedback Output | Allowable SYNC Input Frequency Range (MHZ) | Corresponding VCO Frequency Range | Phase Relationships of the “Q” Outputs to Rising SYNC Edge |
|---|---|---|---|---|
| HIGH | Q/2 | 5 to (2X_Q FMAX Spec)/4 | 20 to (2X_Q FMAX Spec) | 0° |
| HIGH | Any “Q” (Q0–Q4) | 10 to (2X_Q FMAX Spec)/2 | 20 to (2X_Q FMAX Spec) | 0° |
| HIGH | $\overline{Q5}$ | 10 to (2X_Q FMAX Spec)/2 | 20 to (2X_Q FMAX Spec) | 180° |
| HIGH | 2X_Q | 20 to (2X_Q FMAX Spec) | 20 to (2X_Q FMAX Spec) | 0° |
| LOW | Q/2 | 2.5 to (2X_Q FMAX Spec)/8 | 20 to (2X_Q FMAX Spec) | 0° |
| LOW | Any “Q” (Q0–Q4) | 5 to (2X_Q FMAX Spec)/4 | 20 to (2X_Q FMAX Spec) | 0° |
| LOW | $\overline{Q5}$ | 5 to (2X_Q FMAX Spec)/4 | 20 to (2X_Q FMAXSpec) | 180° |
| LOW | 2X_Q | 10 to (2X_Q FMAX Spec)/2 | 20 to (2X_Q FMAXSpec) | 0° |

4. A 1MΩ resistor tied to either Analog $V_{CC}$ or Analog GND as shown in Figure 2 is required to ensure no jitter is present on the MC88915T outputs. This technique causes a phase offset between the SYNC input and the output connected to the FEEDBACK input, measured at the input pins. The $t_{PD}$ spec describes how this offset varies with process, temperature, and voltage. The specs were arrived at by measuring the phase relationship for the 14 lots described in note 1 while the part was in phase–locked operation. The actual measurements were made with a 10MHz SYNC input (1.0ns edge rate from 0.8V – 2.0V) with the Q/2 output fed back. The phase measurements were made at 1.5V. The Q/2 output was terminated at the FEEDBACK input with 100Ω to $V_{CC}$ and 100Ω to ground.

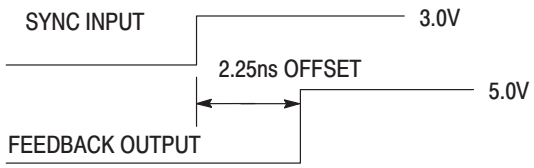



2

With the 1MΩ resistor tied in this fashion, the $t_{PD}$ specification measured at the input pins is:

$t_{PD}$ = 2.25ns ± 1.0ns




With the 1MΩ resistor tied in this fashion, the $t_{PD}$ specification measured at the input pins is:

$t_{PD}$ = –0.775ns ± 0.275ns

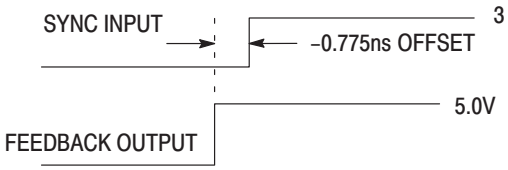



**Figure 2. Depiction of the Fixed SYNC to Feedback Offset (tPD) Which is Present When a 1MΩ Resistor is Tied to $V_{CC}$ or Ground**

5. The $t_{SKEWr}$ specification guarantees that the rising edges of outputs Q/2, Q0, Q1, Q2, Q3, and Q4 will always fall within a 500ps window within one part. However, if the relative position of each output within this window is not specified, the 500 ps window must be added to each side of the tPD specification limits to calculate the total part–to–part skew. For this reason the absolute distribution of these outputs are provided in table 2. When taking the skew data, Q0 was used as a reference, so all measurements are relative to this output. The information in Table 2 is derived from measurements taken from the 14 process lots described in Note 1, over the temperature and voltage range.

**Table 2. Relative Positions of Outputs Q/2, Q0–Q4, 2X_Q, Within the 500ps $t_{SKEWr}$ Spec Window**

| Output | – (ps) | + (ps) |
|---|---|---|
| Q0 | 0 | 0 |
| Q1 | –72 | 40 |
| Q2 | –44 | 276 |
| Q3 | –40 | 255 |
| Q4 | –274 | –34 |
| Q/2 | –16 | 250 |
| 2X_Q | –633 | –35 |

6. **Calculation of Total Output–to–Skew between multiple parts (Part–to–Part skew)**

   By combining the $t_{PD}$ specification and the information in Note 5, the worst case output–to–output skew between multiple 88915's connected in parallel can be calculated. This calculation assumes that all parts have a common SYNC input clock with equal delay of that input signal to each part. This skew value is valid at the 88915 output pins only (equally loaded), it does not include PCB trace delays due to varying loads.

   With a 1 MΩ resistor tied to analog $V_{CC}$ as shown in note 4, the $t_{PD}$ spec. limits between SYNC and the Q/2 output (connected to the FEEDBACK pin) are –1.05ns and –0.5ns. To calculate the skew of any given output between two or more parts, the absolute value of the distribution of that output given in table 2 must be subtracted and added to the lower and upper $t_{PD}$ spec limits respectively. For output Q2, [276 – (–44)] = 320ps is the absolute value of the distribution. Therefore [–1.05ns – 0.32ns] = –1.37ns is the lower $t_{PD}$ limit, and [–0.5ns + 0.32ns] = –0.18ns is the upper limit. Therefore the worst case skew of output Q2 between any number of parts is |(–1.37) – (–0.18)| = 1.19ns. Q2 has the worst case skew distribution of any output, so 1.2ns is the absolute worst case output–to–output skew between multiple parts.

7. Note 4 explains that the $t_{PD}$ specification was measured and is guaranteed for the configuration of the Q/2 output connected to the FEEDBACK pin and the SYNC input running at 10MHz. The fixed offset ($t_{PD}$) as described above has some dependence on the input frequency and at what frequency the VCO is running. The graphs of Figure 3 demonstrate this dependence.

   The data presented in Figure 3 is from devices representing process extremes, and the measurements were also taken at the voltage extremes ($V_{CC}$ = 5.25V and 4.75V). Therefore the data in Figure 3 is a realistic representation of the variation of $t_{PD}$.

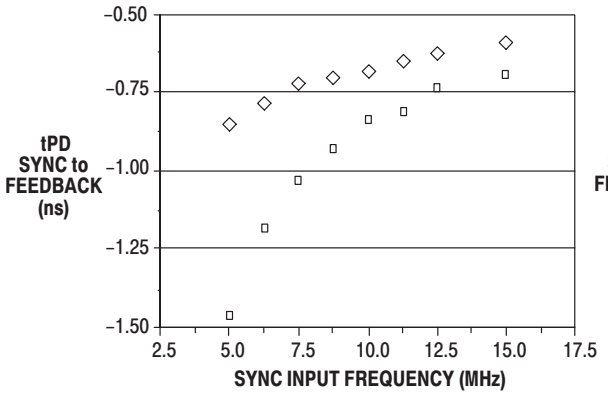



**Figure 3a.**

**$t_{PD}$ versus Frequency Variation for Q/2 Output Fed Back, Including Process and Voltage Variation @ 25°C (With 1MΩ Resistor Tied to Analog $V_{CC}$)**

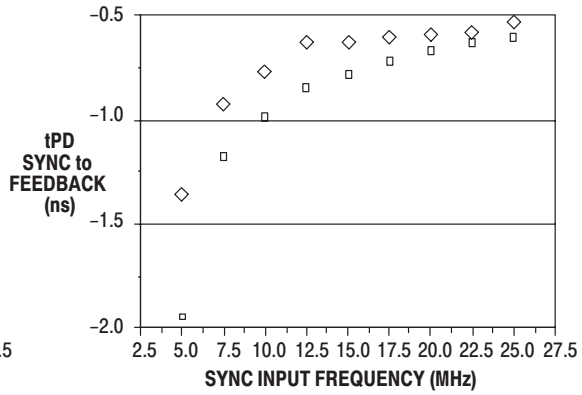



**Figure 3b.**

**$t_{PD}$ versus Frequency Variation for Q4 Output Fed Back, Including Process and Voltage Variation @ 25°C (With 1MΩ Resistor Tied to Analog $V_{CC}$)**

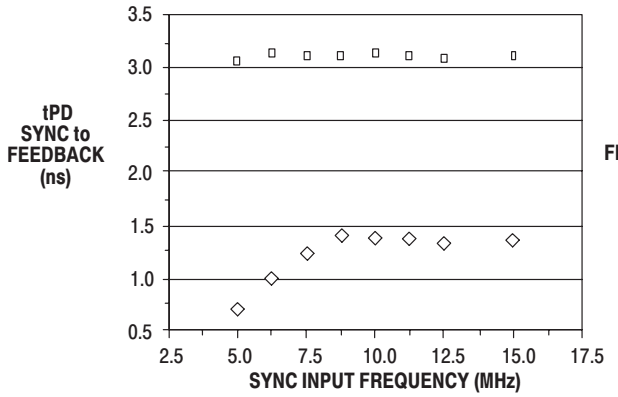



**Figure 3c.**

**$t_{PD}$ versus Frequency Variation for Q/2 Output Fed Back, Including Process and Voltage Variation @ 25°C (With 1MΩ Resistor Tied to Analog GND)**

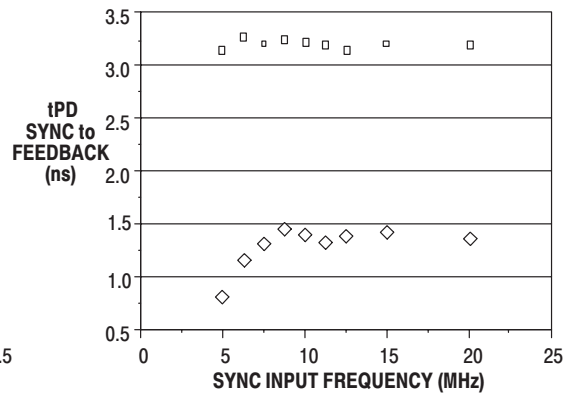



**Figure 3d.**

**$t_{PD}$ versus Frequency Variation for Q4 Output Fed Back, Including Process and Voltage Variation @ 25°C (With 1MΩ Resistor Tied to Analog GND)**

8. The lock indicator pin (LOCK) will reliably indicate a phase–locked condition at SYNC input frequencies down to 10MHz. At frequencies below 10MHz, the frequency of correction pulses going into the phase detector form the SYNC and FEEDBACK pins may not be sufficient to allow the lock indicator circuitry to accurately predict a phase–locked conditition. The MC88915T is guaranteed to provide stable phase–locked operation down to the appropriate minimum input frequency given in Table 1, even though the LOCK pin may be LOW at frequencies below 10MHZ. The exact minimum frequency where the lock indicator functionality can be guaranteed will be available when the MC88915T reaches ‘MC’ status.

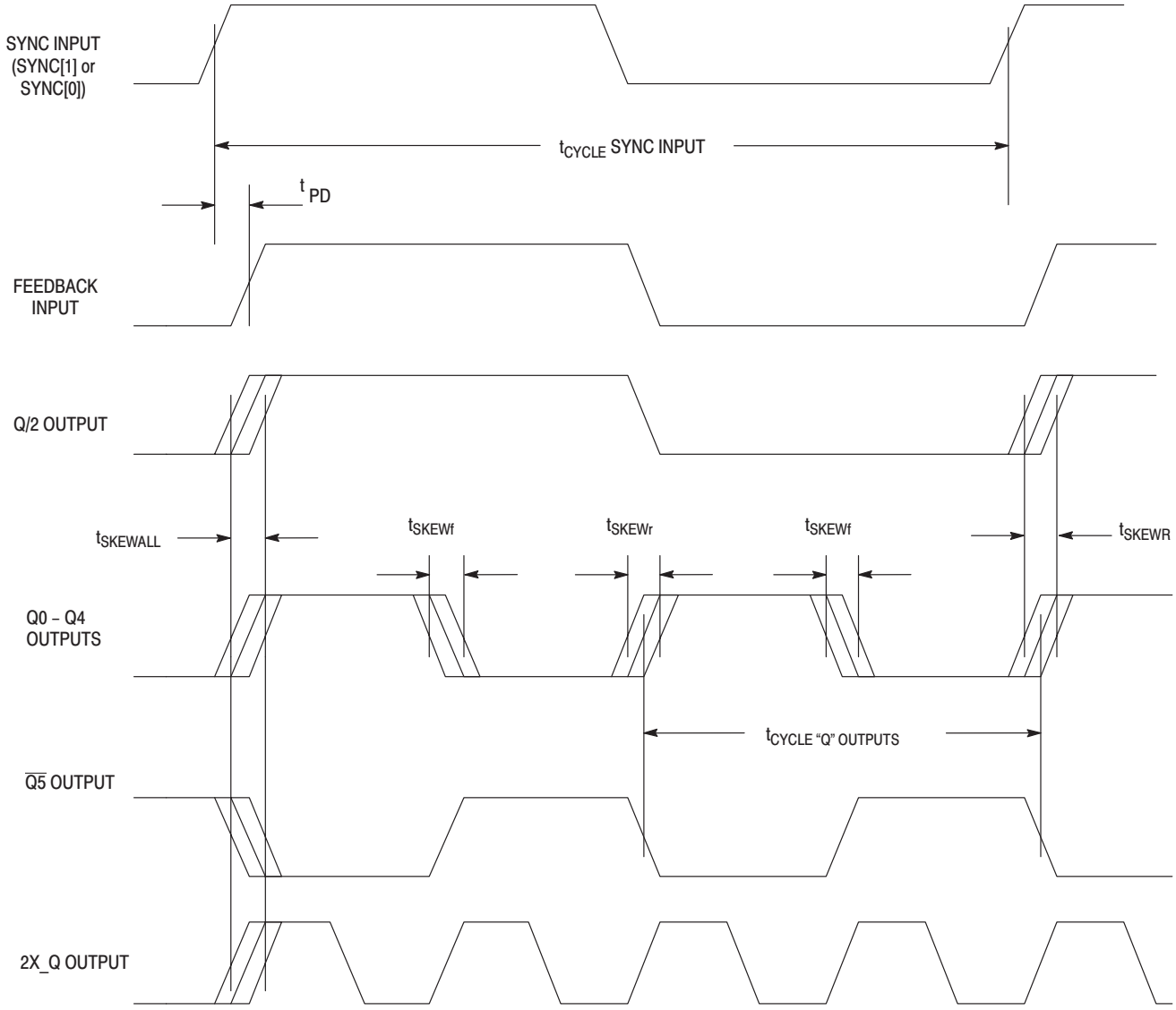
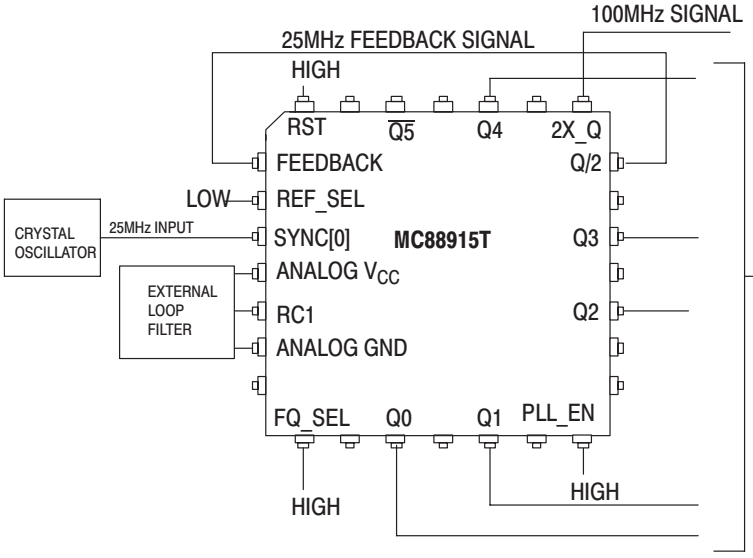



**Figure 4. Output/Input Switching Waveforms and Timing Diagrams**

(These waveforms represent the hook–up configuration of Figure 5a on page 26)

**Timing Notes:**

- The MC88915T aligns rising edges of the FEEDBACK input and SYNC input, therefore the SYNC input does not require a 50% duty cycle.
- All skew specs are measured between the $V_{CC}/2$ crossing point of the appropriate output edges.All skews are specified as 'windows', not as a ± deviation around a center point.
- If a "Q" output is connected to the FEEDBACK input (this situation is not shown), the "Q" output frequency would match the SYNC input frequency, the 2X_Q output would run at twice the SYNC frequency, and the Q/2 output would run at half the SYNC frequency.




**1:2 Input to "Q" Output Frequency Relationship**

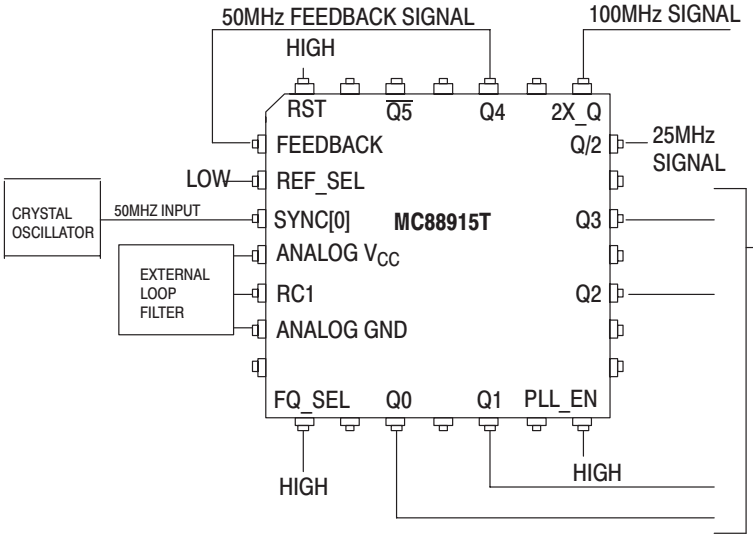
In this application, the Q/2 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q/2 and SYNC, thus the Q/2 frequency will equal the SYNC frequency. The "Q" outputs (Q0–Q4, $\overline{Q5}$) will always run at 2X the Q/2 frequency, and the 2X_Q output will run at 4X the Q/2 frequency.

**Allowable Input Frequency Range:**

**5MHz to (2X_Q FMAX Spec)/4** (for FREQ_SEL HIGH)
**2.5MHz to (2X_Q FMAX Spec)/8** (for FREQ_SEL LOW)

Note: If the $\overline{OE}/\overline{RST}$ input is active, a pull–up or pull–down resistor isn't necessary at the FEEDBACK pin so it won't when the fed back output goes into 3–state.

**Figure 5a. Wiring Diagram and Frequency Relationships With Q/2 Output Feed Back**



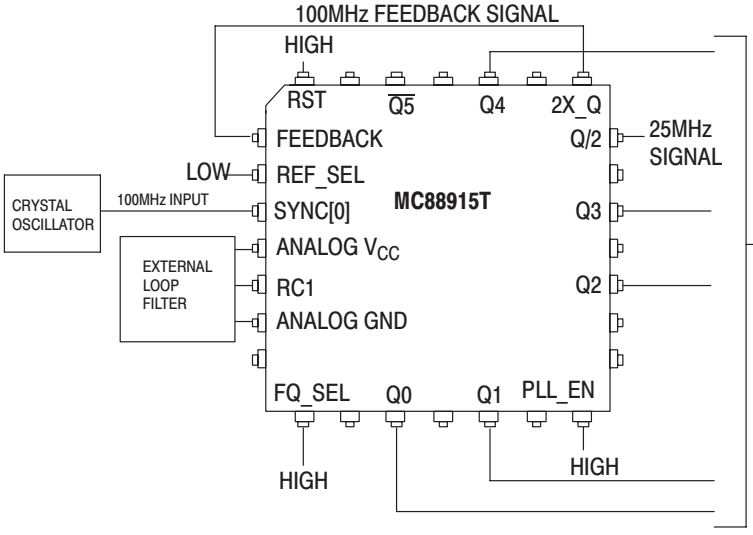

**1:1 Input to "Q" Output Frequency Relationship**

In this application, the Q4 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q4 and SYNC, thus the Q4 frequency (and the rest of the "Q" outputs) will equal the SYNC frequency. The Q/2 output will always run at 1/2 the "Q" frequency, and the 2X_Q output will run at 2X the "Q" frequency.

**Allowable Input Frequency Range:**

**10MHz to (2X_Q FMAX Spec)/2** (for FREQ_SEL HIGH)
**5MHz to (2X_Q FMAX Spec)/4** (for FREQ_SEL LOW)

**Figure 5b. Wiring Diagram and Frequency Relationships With Q4 Output Feed Back**




**2:1 Input to "Q" Output Frequency Relationship**

In this application, the 2X_Q output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of 2X_Q and SYNC, thus the 2X_Q frequency will equal the SYNC frequency. The Q/2 output will always run at 1/4 the 2X_Q frequency, and the "Q" outputs will run at 1/2 the 2X_Q frequency.

**Allowable Input Frequency Range:**

**20MHz to (2X_Q FMAX Spec)** (for FREQ_SEL HIGH)
**10MHz to (2X_Q FMAX Spec)/2** (for FREQ_SEL LOW)

**Figure 5c. Wiring Diagram and Frequency Relationships with 2X_Q Output Feed Back**

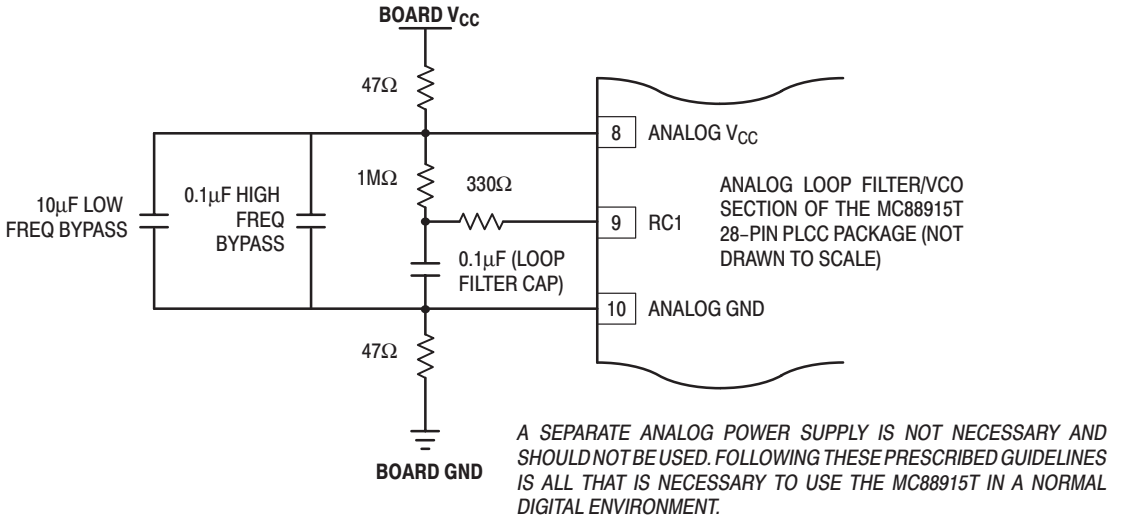



**Figure 6. Recommended Loop Filter and Analog Isolation Scheme for the MC88915T**

**Notes Concerning Loop Filter and Board Layout Issues**

1. Figure 6 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter–free operation:

1a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the RC1 pin.

1b. The 47Ω resistors, the 10μF low frequency bypass capacitor, and the 0.1μF high frequency bypass capacitor form a wide bandwidth filter that will minimize the 88915T's sensitivity to voltage transients from the system digital $V_{CC}$ supply and ground planes. This filter will typically ensure that a 100mV step deviation on the digital $V_{CC}$ supply will cause no more than a 100pS phase deviation on the 88915T outputs. A 250mV step deviation on $V_{CC}$ using the recommended filter values should cause no more than a 250pS phase deviation; if a 25μF bypass capacitor is used (instead of 10μF) a 250mV $V_{CC}$ step should cause no more than a 100pS phase deviation.

If good bypass techniques are used on a board design near components which may cause digital $V_{CC}$ and ground noise, the above described $V_{CC}$ step deviations should not occur at the 88915T's digital $V_{CC}$ supply. The purpose of the bypass filtering scheme shown in Figure 6 is to give the 88915T additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.

1c. There are no special requirements set forth for the loop filter resistors (1MΩ and 330Ω). The loop filter capacitor (0.1μF) can be a ceramic chip capacitior, the same as a standard bypass capacitor.

1d. The 1M reference resistor injects current into the internal charge pump of the PLL, causing a fixed offset between the outputs and the SYNC input. This also prevents excessive jitter caused by inherent PLL dead–band. If the VCO (2X_Q output) is running above 40MHz, the 1MΩ resistor provides the correct amount of current injection into the charge pump (2–3μA). For the TFN55, 70 or 100, if the VCO is running below 40MHz, a 1.5MΩ reference resistor should be used (instead of 1MΩ).

2. In addition to the bypass capacitors used in the analog filter of Figure 6, there should be a 0.1μF bypass capacitor between each of the other (digital) four $V_{CC}$ pins and the board ground plane. This will reduce output switching noise caused by the 88915T outputs, in addition to reducing potential for noise in the 'analog' section of the chip. These bypass capacitors should also be tied as close to the 88915T package as possible.

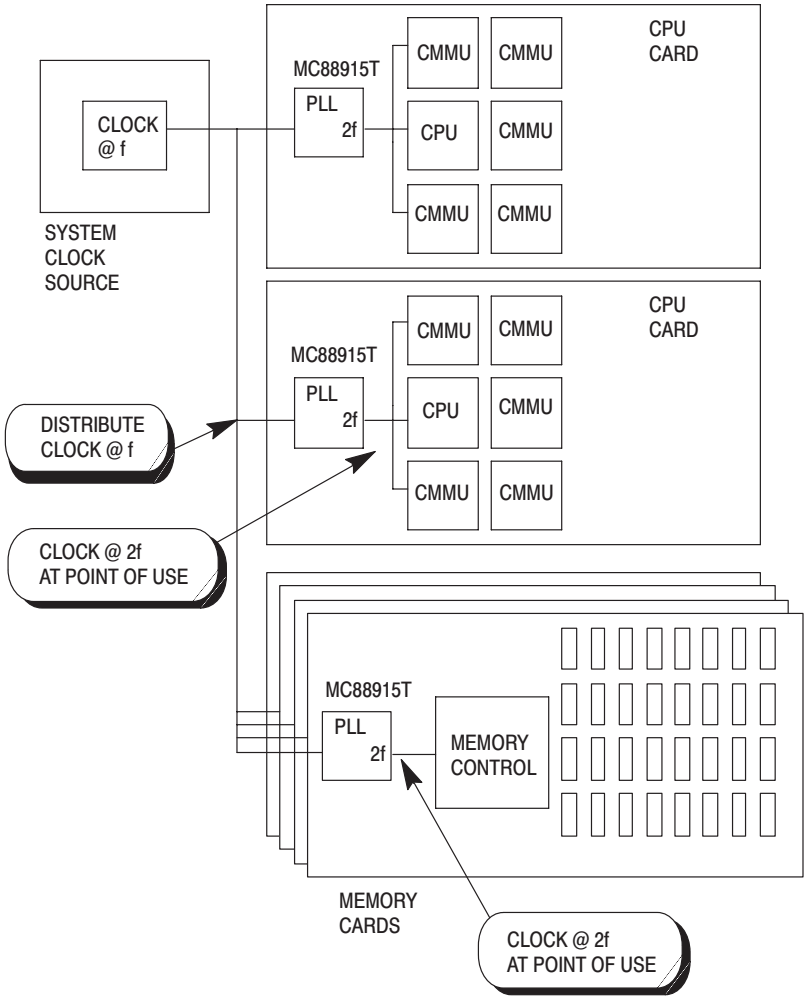



**Figure 7. Representation of a Potential Multi–Processing Application Utilizing the MC88915T for Frequency Multiplication and Low Board–to–Board Skew**

**MC88915T System Level Testing Functionality**

3–state functionality has been added to the 100MHz version of the MC88915T to ease system board testing. Bringing the $\overline{OE}/\overline{RST}$ pin low will put all outputs (except for LOCK) into the high impedance state. As long as the PLL_EN pin is low, the Q0–Q4, Q5, and the Q/2 outputs will remain reset in the low state after the $\overline{OE}/\overline{RST}$ until a falling SYNC edge is seen. The 2X_Q output will be the inverse of the SYNC signal in this mode. If the 3–state functionality will be used, a pull–up or pull–down resistor must be tied to the FEEDBACK input pin to prevent it from floating when the fedback output goes into high impedance.

With the PLL_EN pin low the selected SYNC signal is gated directly into the internal clock distribution network, bypassing and disabling the VCO. In this mode the outputs are directly driven by the SYNC input (per the block diagram). This mode can also be used for low frequency board testing.

Note: If the outputs are put into 3–state during normal PLL operation, the loop will be broken and phase–lock will be lost. It will take a maximum of 10mS (tLOCK spec) to regain phase–lock after the $\overline{OE}/\overline{RST}$ pin goes back high.

**Order Number: MC88LV915T/D**
**Rev 3, 08/2001**

# Low Voltage Low Skew CMOS PLL Clock Driver, 3-State

**MC88LV915T**

**2**

**LOW SKEW CMOS PLL CLOCK DRIVER**

The MC88LV915T Clock Driver utilizes phase–locked loop technology to lock its low skew outputs' frequency and phase onto an input reference clock. It is designed to provide clock distribution for high performance PC's and workstations.

The PLL allows the high current, low skew outputs to lock onto a single clock input and distribute it with essentially zero delay to multiple components on a board. The PLL also allows the MC88LV915T to multiply a low frequency input clock and distribute it locally at a higher (2X) system frequency. Multiple 88LV915's can lock onto a single reference clock, which is ideal for applications when a central system clock must be distributed synchronously to multiple boards (see Figure 4 on Page 37).

Five "Q" outputs (Q0–Q4) are provided with less than 500 ps skew between their rising edges. The $\overline{Q5}$ output is inverted (180° phase shift) from the "Q" outputs. The 2X_Q output runs at twice the "Q" output frequency, while the Q/2 runs at 1/2 the "Q" frequency.

The VCO is designed to run optimally between 20 MHz and the 2X_Q $F_{max}$ specification. The wiring diagrams in Figure 2 detail the different feedback configurations which create specific input/output frequency relationships. Possible frequency ratios of the "Q" outputs to the SYNC input are 2:1, 1:1, and 1:2.

The FREQ_SEL pin provides one bit programmable divide–by in the feedback path of the PLL. It selects between divide–by–1 and divide–by–2 of the VCO before its signal reaches the internal clock distribution section of the chip (see the block diagram on page 2). In most applications FREQ_SEL should be held high (÷1). If a low frequency reference clock input is used, holding FREQ_SEL low (÷2) will allow the VCO to run in its optimal range (>20MHz).

In normal phase–locked operation the PLL_EN pin is held high. Pulling the PLL_EN pin low disables the VCO and puts the 88LV915T in a static "test mode". In this mode there is no frequency limitation on the input clock, which is necessary for a low frequency board test environment. The second SYNC input can be used as a test clock input to further simplify board–level testing (see detailed description on page 11).

Pulling the $\overline{OE}/\overline{RST}$ pin low puts the clock outputs 2X_Q, Q0–Q4, $\overline{Q5}$ and Q/2 into a high impedance state (3–state). After the $\overline{OE}/\overline{RST}$ pin goes back high Q0–Q4, $\overline{Q5}$ and Q/2 will be reset in the low state, with 2X_Q being the inverse of the selected SYNC input. Assuming PLL_EN is low, the outputs will remain reset until the 88LV915 sees a SYNC input pulse.

A lock indicator output (LOCK) will go high when the loop is in steady–state phase and frequency lock. The LOCK output will go low if phase–lock is lost or when the PLL_EN pin is low. The LOCK output will go high no later than 10ms after the 88LV915 sees a SYNC signal and full 5V $V_{CC}$.

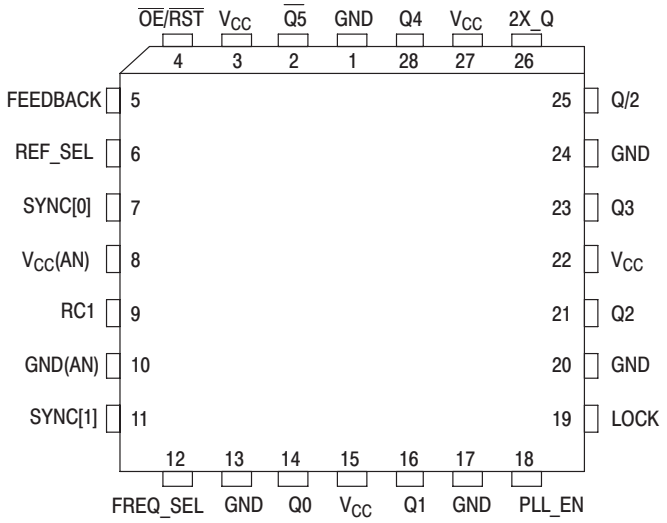
**Features**

- Five Outputs (Q0–Q4) with Output–Output Skew < 500 ps each being phase and frequency locked to the SYNC input
- The phase variation from part–to–part between the SYNC and FEEDBACK inputs is less than 550 ps (derived from the $t_{PD}$ specification, which defines the part–to–part skew)
- Input/Output phase–locked frequency ratios of 1:2, 1:1, and 2:1 are available
- Input frequency range from 5MHz – 2X_Q FMAX spec.
- Additional outputs available at 2X and +2 the system "Q" frequency. Also a $\overline{Q}$ (180° phase shift) output available
- All outputs have ±36 mA drive (equal high and low) at CMOS levels, and can drive either CMOS or TTL inputs. All inputs are TTL–level compatible. ±88mA $I_{OL}/I_{OH}$ specifications guarantee 50Ω transmission line switching on the incident edge
- Test Mode pin (PLL_EN) provided for low frequency testing. Two selectable CLOCK inputs for test or redundancy purposes. All outputs can go into high impedance (3–state) for board test purposes
- Lock Indicator (LOCK) accuracy indicates a phase–locked state



**Rev 3**

**Pinout: 28–Lead PLCC** (Top View)

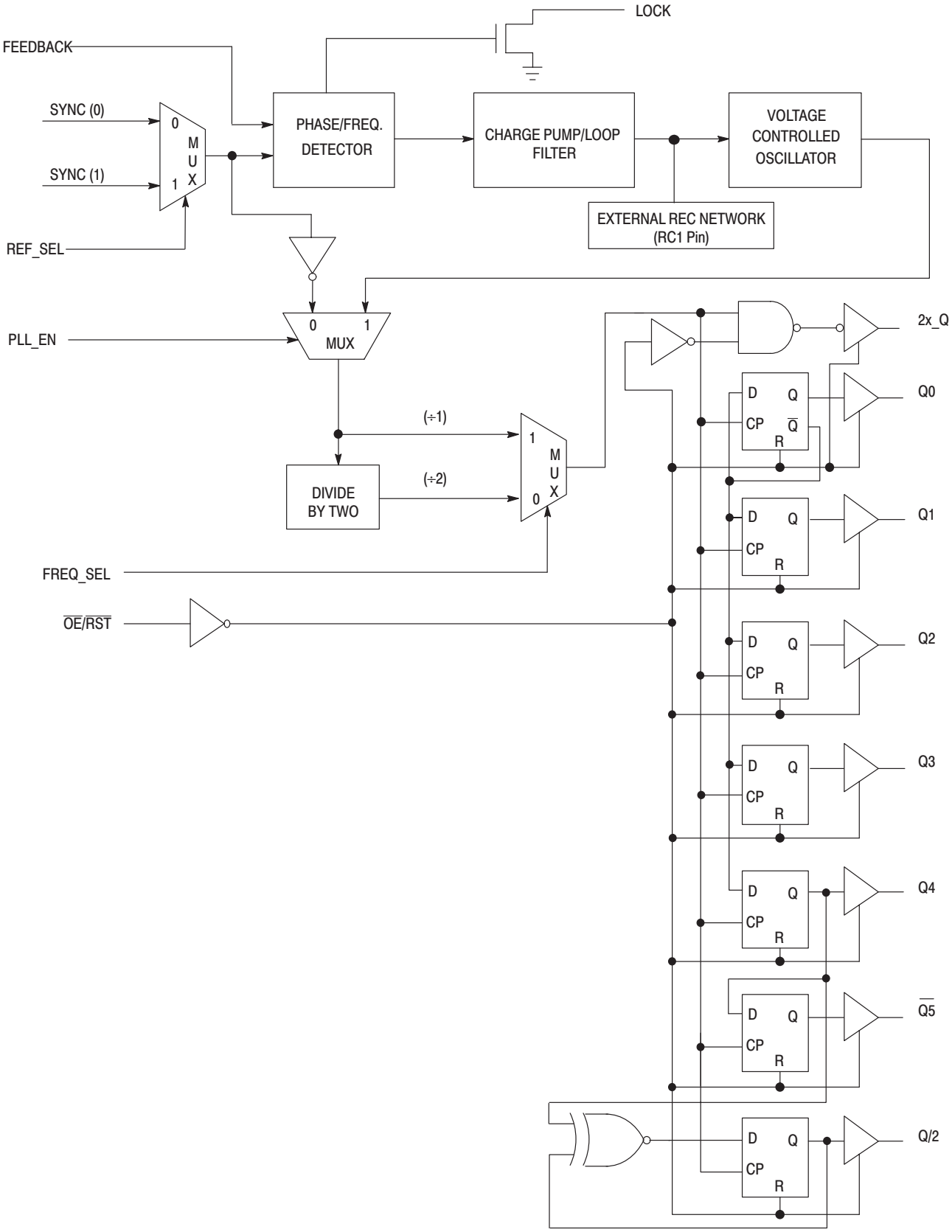



**FN SUFFIX**
PLASTIC PLCC
CASE 776–02

## PIN SUMMARY

| Pin Name | Num | I/O | Function |
|---|---|---|---|
| SYNC[0] | 1 | Input | Reference clock input |
| SYNC[1] | 1 | Input | Reference clock input |
| REF_SEL | 1 | Input | Chooses reference between sync[0] & Sync[1] |
| FREQ_SEL | 1 | Input | Doubles VCO Internal Frequency (low) |
| FEEDBACK | 1 | Input | Feedback input to phase detector |
| RC1 | 1 | Input | Input for external RC network |
| Q(0–4) | 5 | Output | Clock output (locked to sync) |
| $\overline{Q5}$ | 1 | Output | Inverse of clock output |
| 2x_Q | 1 | Output | 2 x clock output (Q) frequency (synchronous) |
| Q/2 | 1 | Output | Clock output(Q) frequency ÷ 2 (synchronous) |
| LOCK | 1 | Output | Indicates phase lock has been achieved (high when locked) |
| $\overline{OE}/\overline{RST}$ | 1 | Input | Output Enable/Asynchronous reset (active low) |
| PLL_EN | 1 | Input | Disables phase–lock for low freq. testing |
| $V_{CC}$,GND | 11 | | Power and ground pins (note pins 8, 10 are “analog” supply pins for internal PLL only) |

**MC88LV915T BLOCK DIAGRAM**



### MAXIMUM RATINGS*

| Symbol | Parameter | Limits | Unit |
|---|---|---|---|
| $V_{CC}$, $AV_{CC}$ | DC Supply Voltage Referenced to GND | –0.5 to 7.0 | V |
| $V_{in}$ | DC Input Voltage (Referenced to GND) | –0.5 to $V_{CC}$ +0.5 | V |
| $V_{out}$ | DC Output Voltage (Referenced to GND) | –0.5 to $V_{CC}$ +0.5 | V |
| $I_{in}$ | DC Input Current, Per Pin | ±20 | mA |
| $I_{out}$ | DC Output Sink/Source Current, Per Pin | ±50 | mA |
| $I_{CC}$ | DC $V_{CC}$ or GND Current Per Output Pin | ±50 | mA |
| $T_{stg}$ | Storage Temperature | –65 to +150 | °C |

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 3.3 ±0.3 | V |
| $V_{in}$ | DC Input Voltage | 0 to $V_{CC}$ | V |
| $V_{out}$ | DC Output Voltage | 0 to $V_{CC}$ | V |
| $T_A$ | Ambient Operating Temperature | 0 to 70 | °C |
| ESD | Static Discharge Voltage | > 1000 | V |

### DC CHARACTERISTICS ($T_A$ = 0°C to 70°C; $V_{CC}$ = 3.3V ± 0.3V)

| Symbol | Parameter | $V_{CC}$ | Guaranteed Limits | Unit | Condition |
|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High Level Input Voltage | 3.0<br>3.3 | 2.0<br>2.0 | V | $V_{OUT}$ = 0.1V or<br>$V_{CC}$ – 0.1V |
| $V_{IL}$ | Minimum Low Level Input Voltage | 3.0<br>3.3 | 0.8<br>0.8 | V | $V_{OUT}$ = 0.1V or<br>$V_{CC}$ – 0.1V |
| $V_{OH}$ | Minimum High Level Output Voltage | 3.0<br>3.3 | 2.4<br>2.7 | V | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OH}$= –24mA |
| $V_{OL}$ | Minimum Low Level Output Voltage | 3.0<br>3.3 | 0.44<br>0.44 | V | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OH}$= 24mA |
| $I_{IN}$ | Maximum Input Leakage Current | 3.6 | ±1.0 | µA | $V_I$ = $V_{CC}$, GND |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | 3.6 | 2.0 | mA | $V_I$ = $V_{CC}$ – 2.1V |
| $I_{OLD}$ | Minimum Dynamic[3] Output Current | 3.6 | +50 | mA | $V_{OLD}$ = 1.25V |
| $I_{OHD}$ | | 3.6 | –50 | mA | $V_{OHD}$ =2.35V |
| $I_{CC}$ | Maximum Quiescent Supply Current | 3.6 | TBD | µA | $V_I$ = $V_{CC}$, GND |

1. $I_{OL}$ is +12mA for the $\overline{RST}$_$\overline{OUT}$ output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration 2.0ms, one output loaded at a time.

### SYNC INPUT TIMING REQUIREMENTS

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{RISE/FALL}$<br>SYNC Input | Rise/Fall Time, SYNC Input<br>From 0.8V to 2.0V | — | 5.0 | ns |
| $t_{CYCLE}$,<br>SYNC Input | Input Clock Period<br>SYNC Input | $\frac{1}{f_{2X\_Q}/4}$ | 100 | ns |
| Duty Cycle | Duty Cycle, SYNC Input | 50% ± 25% | | |

**FREQUENCY SPECIFICATIONS** ($T_A$ = 0°C to 70°C; $V_{CC}$ = 3.3V ± 0.3V)

| Symbol | Parameter | Guaranteed Minimum | Unit |
|---|---|---|---|
| Fmax (2X_Q) | Maximum Operating Frequency, 2X_Q Output | 100 | MHz |
| Fmax ('Q') | Maximum Operating Frequency, Q0–Q3 Outputs | 50 | MHz |

NOTE: Maximum Operating Frequency is guaranteed with the 88LV926 in a phase–locked condition.



**AC CHARACTERISTICS** ($T_A$ =0° C to +70° C, $V_{CC}$ = 3.3V ±0.3V, Load = 50Ω Terminated to $V_{CC}$/2)

| Symbol | Parameter | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $t_{RISE/FALL}$ Outputs | Rise/Fall Time, All Outputs (Between 0.8 to 2.0V) | 0.5 | 2.0 | ns | Into a 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{PULSE\ WIDTH}$ (Q0–Q4, $\overline{Q5}$, Q/2) | Output Pulse Width: Q0, Q1, Q2, Q3, Q4, $\overline{Q5}$, Q/2 @ $V_{CC}$/2 | $0.5t_{CYCLE}$ – 0.5 [1] | $0.5t_{CYCLE}$ + 0.5 [1] | ns | Into a 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{PULSE\ WIDTH}$ (2X_Q Output) | Output Pulse Width: 2X_Q @ 1.5V<br>40MHz<br>66MHz<br>80MHz<br>100MHz | <br>$0.5t_{CYCLE}$ – 1.5<br>$0.5t_{CYCLE}$ – 1.0<br>$0.5t_{CYCLE}$ – 1.0<br>$0.5t_{CYCLE}$ – 1.0 | <br>$0.5t_{CYCLE}$ + 0.5<br>$0.5t_{CYCLE}$ + 0.5<br>$0.5t_{CYCLE}$ + 0.5<br>$0.5t_{CYCLE}$ + 0.5 | ns | Into a 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{CYCLE}$ (2x_Q Output) | Cycle–to–Cycle Variation 2x_Q @ $V_{CC}$/2<br>40MHz<br>66MHz<br>80MHz<br>100MHz | <br>$t_{CYCLE}$ – 600ps<br>$t_{CYCLE}$ – 300ps<br>$t_{CYCLE}$ – 300ps<br>$t_{CYCLE}$ – 400ps | <br>$t_{CYCLE}$ + 600ps<br>$t_{CYCLE}$ + 300ps<br>$t_{CYCLE}$ + 300ps<br>$t_{CYCLE}$ + 400ps | | |
| $t_{PD}$ [2] SYNC Feedback | | (With 1MΩ from RC1 to An $V_{CC}$) | | ns | |
| | SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins)<br>66MHz<br>80MHz<br>100MHz | <br>–1.65<br>–1.45<br>–1.25 | <br>–1.05<br>–0.85<br>–0.65 | | |
| $t_{SKEWr}$ [3] (Rising) See Note **4** | Output–to–Output Skew Between Outputs Q0–Q4, Q/2 (Rising Edges Only) | — | 500 | ps | All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{SKEWf}$ [3] (Falling) | Output–to–Output Skew Between Outputs Q0–Q4 (Falling Edges Only) | — | 750 | ps | All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{SKEWall}$ [3] | Output–to–Output Skew 2X_Q, Q/2, Q0–Q4 Rising, $\overline{Q5}$ Falling | — | 750 | ps | All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{LOCK}$ [4] | Time Required to Acquire Phase–Lock From Time SYNC Input Signal is Received | 1.0 | 10 | ms | Also Time to LOCK Indicator High |
| $t_{PZL}$ [5] | Output Enable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2 | 3.0 | 14 | ns | Measured With the PLL_EN Pin Low |
| $t_{PHZ}$,$t_{PLZ}$ [5] | Output Disable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2 | 3.0 | 14 | ns | Measured With the PLL_EN Pin Low |

1. $T_{CYCLE}$ in this spec is 1/Frequency at which the particular output is running.
2. The $T_{PD}$ specification's min/max values may shift closer to zero if a larger pullup resistor is used.
3. Under equally loaded conditions and at a fixed temperature and voltage.
4. With $V_{CC}$ fully powered–on, and an output properly connected to the FEEDBACK pin. $t_{LOCK}$ maximum is with C1 = 0.1µF, $t_{LOCK}$ minimum is with C1 = 0.01µF.
5. The $t_{PZL}$, $t_{PHZ}$, $t_{PLZ}$ minimum and maximum specifications are estimates, the final guaranteed values will be available when 'MC' status is reached.

## Applications Information for All Versions

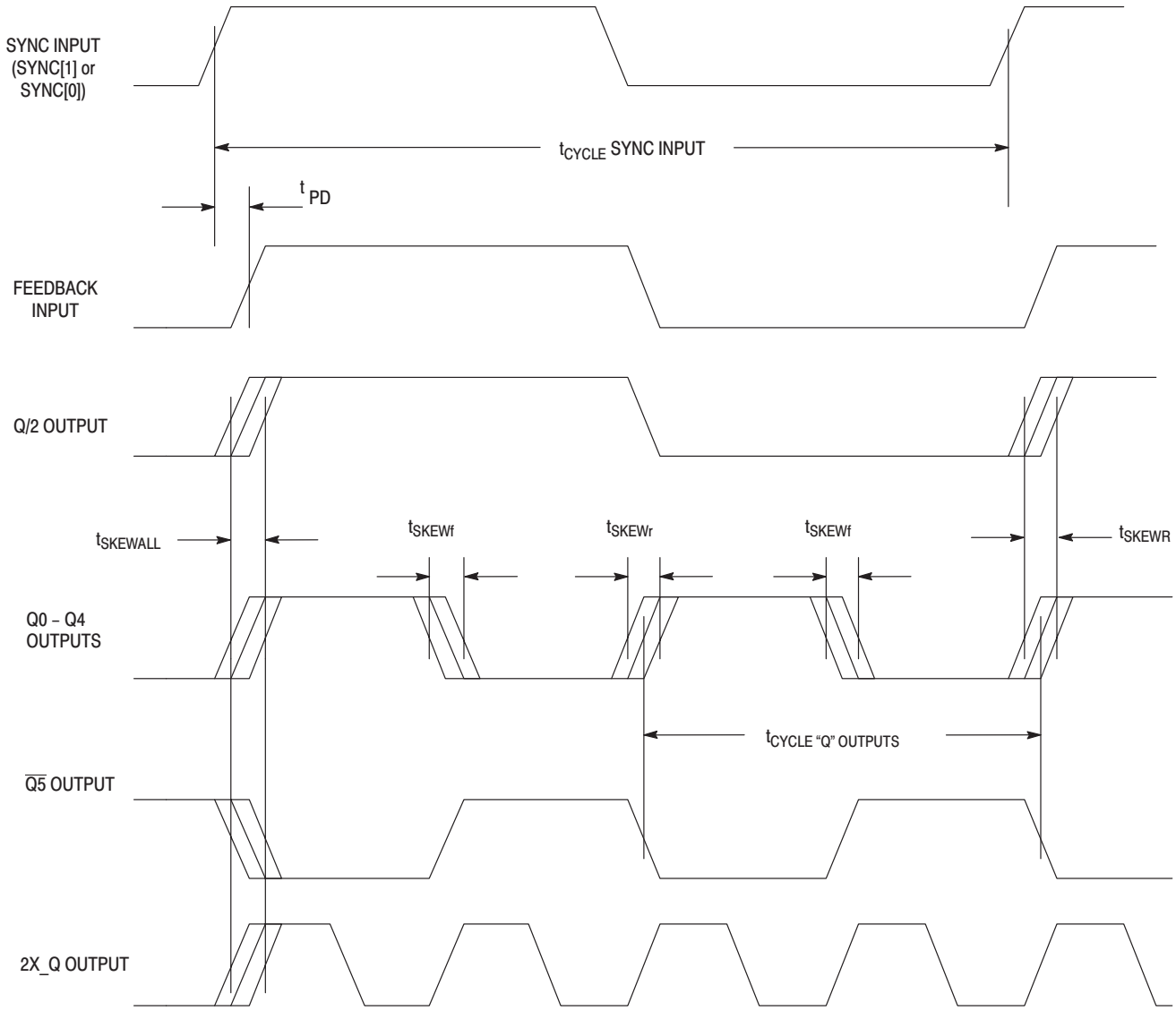
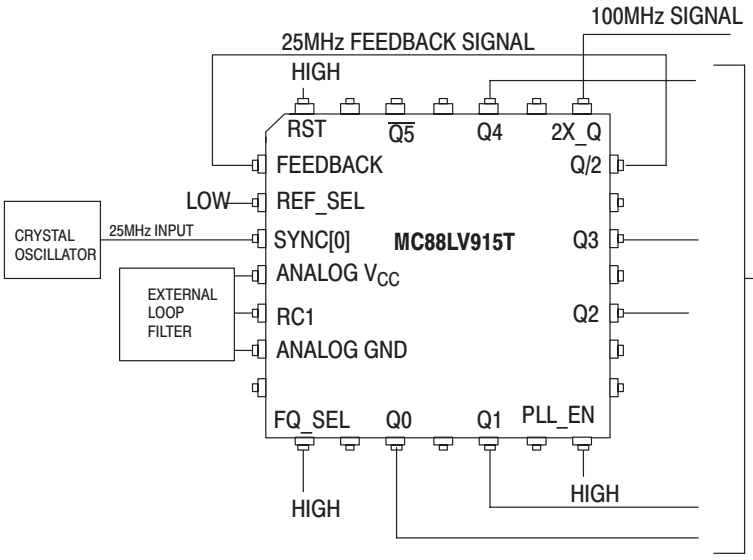



**Figure 1. Output/Input Switching Waveforms and Timing Diagrams**

(These waveforms represent the hook–up configuration of Figure 2a on page 35)

**Timing Notes:**

- The MC88LV915T aligns rising edges of the FEEDBACK input and SYNC input, therefore the SYNC input does not require a 50% duty cycle.
- All skew specs are measured between the $V_{CC}/2$ crossing point of the appropriate output edges.All skews are specified as 'windows', not as a ± deviation around a center point.
- If a "Q" output is connected to the FEEDBACK input (this situation is not shown), the "Q" output frequency would match the SYNC input frequency, the 2X_Q output would run at twice the SYNC frequency, and the Q/2 output would run at half the SYNC frequency.




**1:2 Input to "Q" Output Frequency Relationship**

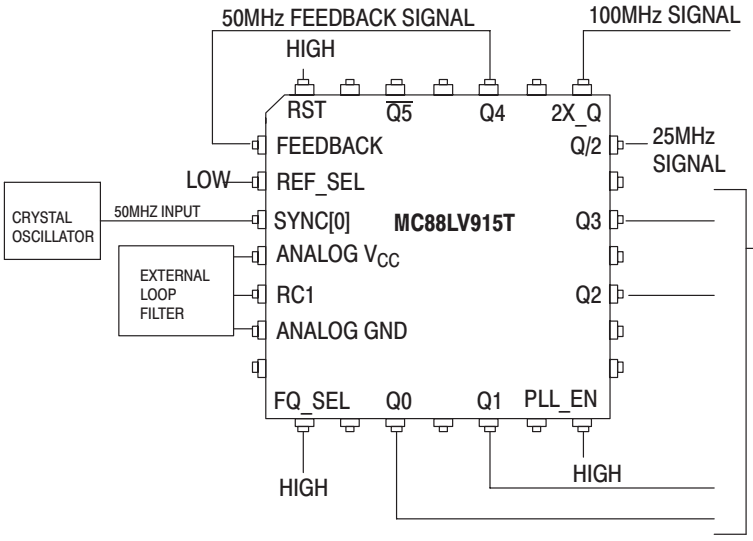
In this application, the Q/2 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q/2 and SYNC, thus the Q/2 frequency will equal the SYNC frequency. The "Q" outputs (Q0–Q4, $\overline{Q5}$) will always run at 2X the Q/2 frequency, and the 2X_Q output will run at 4X the Q/2 frequency.

**Allowable Input Frequency Range:**

**5MHz to (2X_Q FMAX Spec)/4** (for FREQ_SEL HIGH)
**2.5MHz to (2X_Q FMAX Spec)/8** (for FREQ_SEL LOW)

Note: If the $\overline{OE}/\overline{RST}$ input is active, a pull–up or pull–down resistor isn't necessary at the FEEDBACK pin so it won't when the fed back output goes into 3–state.

**Figure 2a. Wiring Diagram and Frequency Relationships With Q/2 Output Feed Back**



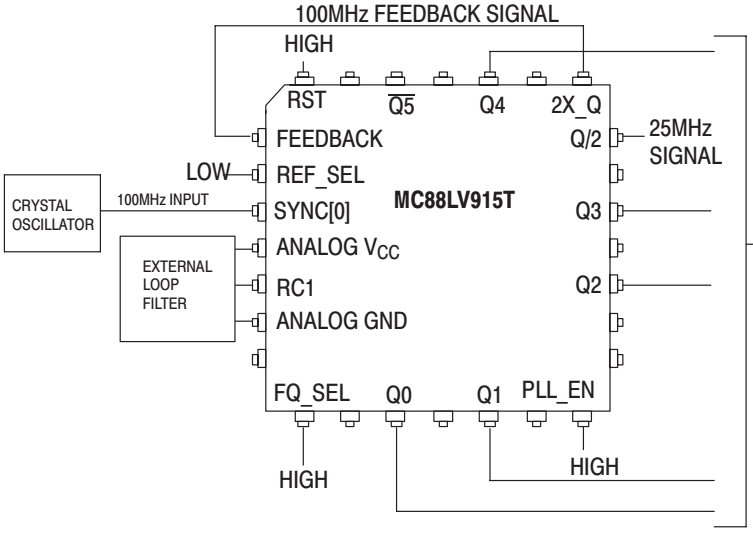

**1:1 Input to "Q" Output Frequency Relationship**

In this application, the Q4 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q4 and SYNC, thus the Q4 frequency (and the rest of the "Q" outputs) will equal the SYNC frequency. The Q/2 output will always run at 1/2 the "Q" frequency, and the 2X_Q output will run at 2X the "Q" frequency.

**Allowable Input Frequency Range:**

**10MHz to (2X_Q FMAX Spec)/2** (for FREQ_SEL HIGH)
**5MHz to (2X_Q FMAX Spec)/4** (for FREQ_SEL LOW)

**Figure 2b. Wiring Diagram and Frequency Relationships With Q4 Output Feed Back**




**2:1 Input to "Q" Output Frequency Relationship**

In this application, the 2X_Q output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of 2X_Q and SYNC, thus the 2X_Q frequency will equal the SYNC frequency. The Q/2 output will always run at 1/4 the 2X_Q frequency, and the "Q" outputs will run at 1/2 the 2X_Q frequency.

**Allowable Input Frequency Range:**

**20MHz to (2X_Q FMAX Spec)** (for FREQ_SEL HIGH)
**10MHz to (2X_Q FMAX Spec)/2** (for FREQ_SEL LOW)

**Figure 2c. Wiring Diagram and Frequency Relationships with 2X_Q Output Feed Back**

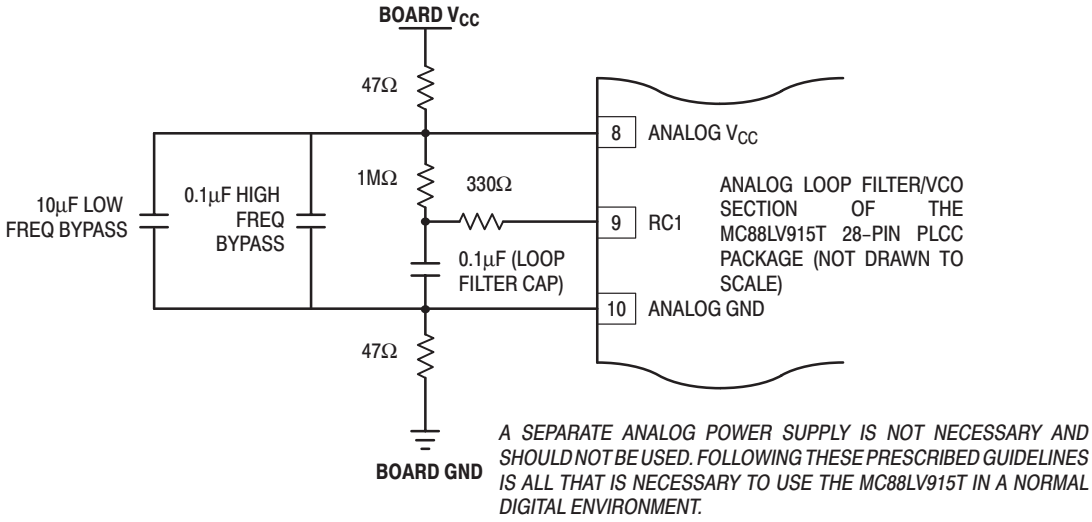



**Figure 3. Recommended Loop Filter and Analog Isolation Scheme for the MC88LV915T**

**Notes Concerning Loop Filter and Board Layout Issues**

1.Figure 3 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter–free operation:

1a.All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the RC1 pin.

1b.The 47Ω resistors, the 10μF low frequency bypass capacitor, and the 0.1μF high frequency bypass capacitor form a wide bandwidth filter that will minimize the 88LV915T's sensitivity to voltage transients from the system digital $V_{CC}$ supply and ground planes. This filter will typically ensure that a 100mV step deviation on the digital $V_{CC}$ supply will cause no more than a 100pS phase deviation on the 88LV915T outputs. A 250mV step deviation on $V_{CC}$ using the recommended filter values should cause no more than a 250pS phase deviation; if a 25μF bypass capacitor is used (instead of 10μF) a 250mV $V_{CC}$ step should cause no more than a 100pS phase deviation.

If good bypass techniques are used on a board design near components which may cause digital $V_{CC}$ and ground noise, the above described $V_{CC}$ step deviations should not occur at the 88LV915T's digital $V_{CC}$ supply. The purpose of the bypass filtering scheme shown in Figure 3 is to give the 88LV915T additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.

1c.There are no special requirements set forth for the loop filter resistors (1MΩ and 330Ω). The loop filter capacitor (0.1μF) can be a ceramic chip capacitior, the same as a standard bypass capacitor.

1d.The 1M reference resistor injects current into the internal charge pump of the PLL, causing a fixed offset between the outputs and the SYNC input. This also prevents excessive jitter caused by inherent PLL dead–band. If the VCO (2X_Q output) is running above 40MHz, the 1MΩ resistor provides the correct amount of current injection into the charge pump (2–3μA). For the TFN55, 70 or 100, if the VCO is running below 40MHz, a 1.5MΩ reference resistor should be used (instead of 1MΩ).

2. In addition to the bypass capacitors used in the analog filter of Figure 3, there should be a 0.1μF bypass capacitor between each of the other (digital) four $V_{CC}$ pins and the board ground plane. This will reduce output switching noise caused by the 88LV915T outputs, in addition to reducing potential for noise in the 'analog' section of the chip. These bypass capacitors should also be tied as close to the 88LV915T package as possible.

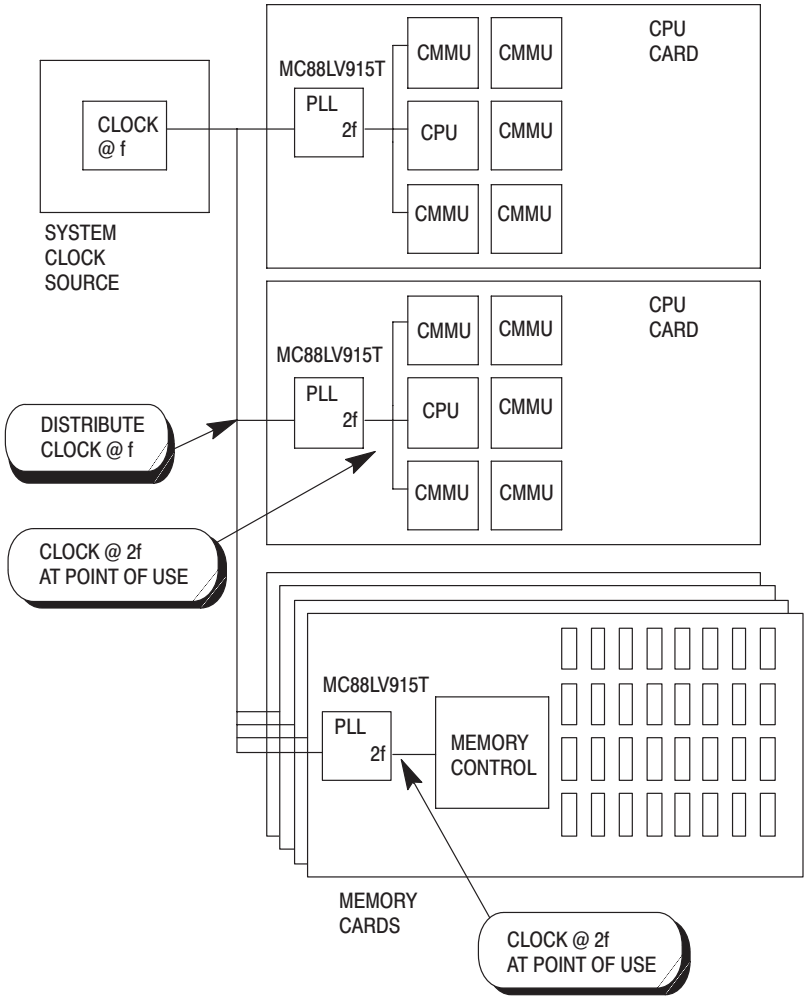



**Figure 4. Representation of a Potential Multi–Processing Application Utilizing the MC88LV915T for Frequency Multiplication and Low Board–to–Board Skew**

**MC88LV915T System Level Testing Functionality**

3–state functionality has been added to the 100MHz version of the MC88LV915T to ease system board testing. Bringing the $\overline{OE}/\overline{RST}$ pin low will put all outputs (except for LOCK) into the high impedance state. As long as the PLL_EN pin is low, the Q0–Q4, Q5, and the Q/2 outputs will remain reset in the low state after the $\overline{OE}/\overline{RST}$ until a falling SYNC edge is seen. The 2X_Q output will be the inverse of the SYNC signal in this mode. If the 3–state functionality will be used, a pull–up or pull–down resistor must be tied to the FEEDBACK input pin to prevent it from floating when the fedback output goes into high impedance.

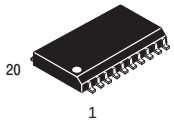
With the PLL_EN pin low the selected SYNC signal is gated directly into the internal clock distribution network, bypassing and disabling the VCO. In this mode the outputs are directly driven by the SYNC input (per the block diagram). This mode can also be used for low frequency board testing.

Note: If the outputs are put into 3–state during normal PLL operation, the loop will be broken and phase–lock will be lost. It will take a maximum of 10mS (tLOCK spec) to regain phase–lock after the $\overline{OE}/\overline{RST}$ pin goes back high.

# Low Skew CMOS PLL 68060 Clock Driver

**MC88LV926**

**LOW SKEW CMOS PLL 68060 CLOCK DRIVER**




**DW SUFFIX**
PLASTIC SOIC PACKAGE
CASE 751D

2

The MC88LV926 Clock Driver utilizes phase–locked loop technology to lock its low skew outputs' frequency and phase onto an input reference clock. It is designed to provide clock distribution for CISC microprocessor or single processor RISC systems. The $\overline{\text{RST}}$_$\overline{\text{IN}}$/$\overline{\text{RST}}$_$\overline{\text{OUT}}$(LOCK) pins provide a processor reset function designed specifically for the MC68/EC/LC030/040/060 microprocessor family. To support the 68060 processor, the 88LV926 operates from a 3.3V as well as a 5.0V supply.

The PLL allows the high current, low skew outputs to lock onto a single clock input and distribute it with essentially zero delay to multiple locations on a board. The PLL also allows the MC88LV926 to multiply a low frequency input clock and distribute it locally at a higher (2X) system frequency.

- 2X_Q Output Meets All Requirements of the 50 and 66MHz 68060 Microprocessor PCLK Input Specifications
- Low Voltage 3.3V $V_{CC}$
- Three Outputs (Q0–Q2) With Output–Output Skew <500ps
- $\overline{\text{CLKEN}}$ Output for Half Speed Bus Applications
- The Phase Variation From Part–to–Part Between SYNC and the 'Q' Outputs Is Less Than 600ps (Derived From the $T_{PD}$ Specification, Which Defines the Part–to–Part Skew)
- SYNC Input Frequency Range From 5MHZ to 2X_Q $F_{Max}$/4
- All Outputs Have ±36mA Drive (Equal High and Low) CMOS Levels
- Can Drive Either CMOS or TTL Inputs. All Inputs Are TTL–Level Compatible with $V_{CC}$ = 3.3V
- Test Mode Pin (PLL_EN) Provided for Low Frequency Testing

Three 'Q' outputs (Q0–Q2) are provided with less than 500ps skew between their rising edges. A 2X_Q output runs at twice the 'Q' output frequency. The 2X_Q output is ideal for 68060 systems which require a 2X processor clock input, and it meets the tight duty cycle spec of the 50 and 66MHz 68060. The QCLKEN output is designed to drive the $\overline{\text{CLKEN}}$ input of the 68060 when the bus logic runs at half of the microprocessor clock rate. The QCLKEN output is skewed relative to the 2X_Q output to ensure that $\overline{\text{CLKEN}}$ setup and hold times of the 68060 are satisfied. A Q/2 frequency is fed back internally, providing a fixed 2X multiplication from the 'Q' outputs to the SYNC input. Since the feedback is done internally (no external feedback pin is provided) the input/output frequency relationships are fixed. The $\overline{\text{Q3}}$ output provides an inverted clock output to allow flexibility in the clock tree design.

In normal phase–locked operation the PLL_EN pin is held high. Pulling the PLL_EN pin low disables the VCO and puts the 88LV926 in a static 'test mode'. In this mode there is no frequency limitation on the input clock, which is necessary for a low frequency board test environment.

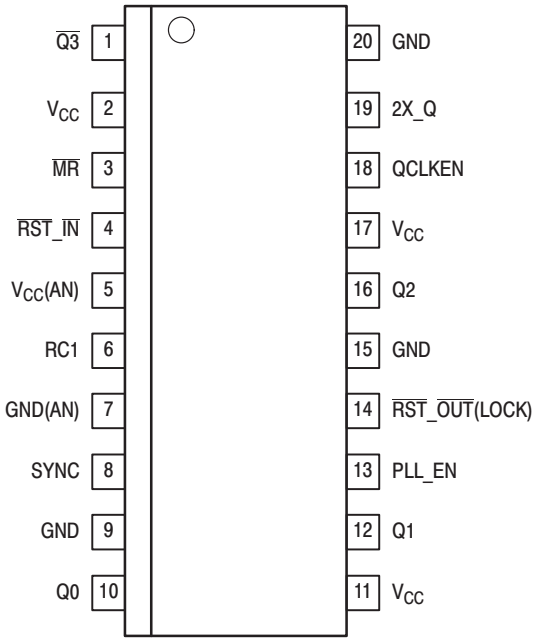
The $\overline{\text{RST}}$_$\overline{\text{OUT}}$(LOCK) pin doubles as a phase–lock indicator. When the $\overline{\text{RST}}$_$\overline{\text{IN}}$ pin is held high, the open drain $\overline{\text{RST}}$_$\overline{\text{OUT}}$ pin will be pulled actively low until phase–lock is achieved. When phase–lock occurs, the $\overline{\text{RST}}$_$\overline{\text{OUT}}$(LOCK) is released and a pull–up resistor will pull the signal high. To give a processor reset signal, the $\overline{\text{RST}}$_$\overline{\text{IN}}$ pin is toggled low, and the $\overline{\text{RST}}$_$\overline{\text{OUT}}$(LOCK) pin will stay low for 1024 cycles of the 'Q' output frequency after the RST_IN pin is brought back high.

**Description of the $\overline{\text{RST}}$_$\overline{\text{IN}}$/$\overline{\text{RST}}$_$\overline{\text{OUT}}$(LOCK) Functionality**

The $\overline{\text{RST}}$_$\overline{\text{IN}}$ and $\overline{\text{RST}}$_$\overline{\text{OUT}}$(LOCK) pins provide a 68030/040/060 processor reset function, with the $\overline{\text{RST}}$_$\overline{\text{OUT}}$ pin also acting as a lock indicator. If the $\overline{\text{RST}}$_$\overline{\text{IN}}$ pin is held high during system power–up, the $\overline{\text{RST}}$_$\overline{\text{OUT}}$ pin will be in the low state until steady state phase/frequency lock to the input reference is achieved. 1024 'Q' output cycles after phase–lock is achieved the $\overline{\text{RST}}$_$\overline{\text{OUT}}$(LOCK) pin will go into a high impedance state, allowing it to be pulled high by an external pull–up resistor (see the AC/DC specs for the characteristics of the $\overline{\text{RST}}$_$\overline{\text{OUT}}$(LOCK) pin). If the $\overline{\text{RST}}$_$\overline{\text{IN}}$ pin is held low during power–up, the $\overline{\text{RST}}$_$\overline{\text{OUT}}$(LOCK) pin will remain low.

**Rev 4**

**Figure 1. Pinout: 20–Lead Wide SOIC Package**
(Top View)






**Description of the RST_IN/RST_OUT(LOCK) Functionality** (continued)

After the system start–up is complete and the 88LV926 is phase–locked to the SYNC input signal (RST_OUT high), the processor reset functionality can be utilized. When the RST_IN pin is toggled low (min. pulse width=10nS), RST_OUT(LOCK) will go to the low state and remain there for 1024 cycles of the 'Q' output frequency (512 SYNC cycles). During the time in which the RST_OUT(LOCK) is actively pulled low, all the 88LV926 clock outputs will continue operating correctly and in a locked condition to the SYNC input (clock signals to the 68030/040/060 family of processors must continue while the processor is in reset). A propagation delay after the 1024th cycle RST_OUT(LOCK) goes back to the high impedance state to be pulled high by the resistor.

*Power Supply Ramp Rate Restriction for Correct 030/040 Processor Reset Operation During System Start–up*

Because the RST_OUT(LOCK) pin is an indicator of phase–lock to the reference source, some constraints must be placed on the power supply ramp rate to make sure the RST_OUT(LOCK) signal holds the processor in reset during system start–up (power–up). With the recommended loop filter values (see Figure 5.) the lock time is approximately 10ms. The phase–lock loop will begin attempting to lock to a reference source (if it is present) when VCC reaches 2V. If the $V_{CC}$ ramp rate is significantly slower than 10ms, then the PLL could lock to the reference source, causing RST_OUT(LOCK) to go high before the 88LV926 and '030/040 processor is fully powered up, violating the processor reset specification. Therefore, if it is necessary for the RST_IN pin to be held high during power–up, the $V_{CC}$ ramp rate must be less than 10mS for proper 68030/040/060 reset operation.

This ramp rate restriction can be ignored if the RST_IN pin can be held low during system start–up (which holds RST_OUT low). The RST_OUT(LOCK) pin will then be pulled back high 1024 cycles after the RST_IN pin goes high.

**CAPACITANCE AND POWER SPECIFICATIONS**

| Symbol | Parameter | Value Typ | Unit | Test Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5* | pF | $V_{CC}$ = 5.0V |
| $C_{PD}$ | Power Dissipation Capacitance | 40* | pF | $V_{CC}$ = 5.0V |
| $PD_1$ | Power Dissipation at 33MHz With 50Ω Thevenin Termination | 15mW/Output* 90mW/Device | mW | $V_{CC}$ = 5.0V T = 25°C |
| $PD_2$ | Power Dissipation at 33MHz With 50Ω Parallel Termination to GND | 37.5mW/Output* 225mW/Device | mW | $V_{CC}$ = 5.0V T = 25°C |

* Value at $V_{CC}$ = 3.3V TBD.

**MAXIMUM RATINGS***

| Symbol | Parameter | Limits | Unit |
|---|---|---|---|
| $V_{CC}$, $AV_{CC}$ | DC Supply Voltage Referenced to GND | –0.5 to 7.0 | V |
| $V_{in}$ | DC Input Voltage (Referenced to GND) | –0.5 to $V_{CC}$ +0.5 | V |
| $V_{out}$ | DC Output Voltage (Referenced to GND) | –0.5 to $V_{CC}$ +0.5 | V |
| $I_{in}$ | DC Input Current, Per Pin | ±20 | mA |
| $I_{out}$ | DC Output Sink/Source Current, Per Pin | ±50 | mA |
| $I_{CC}$ | DC $V_{CC}$ or GND Current Per Output Pin | ±50 | mA |
| $T_{stg}$ | Storage Temperature | –65 to +150 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

**RECOMMENDED OPERATING CONDITIONS**

| Symbol | Parameter | Limits | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 3.3 ±0.3 | V |
| $V_{in}$ | DC Input Voltage | 0 to $V_{CC}$ | V |
| $V_{out}$ | DC Output Voltage | 0 to $V_{CC}$ | V |
| $T_A$ | Ambient Operating Temperature | 0 to 70 | °C |
| ESD | Static Discharge Voltage | > 1500 | V |

**DC CHARACTERISTICS** ($T_A$ = 0°C to 70°C; $V_{CC}$ = 3.3V ± 0.3V)[4]

| Symbol | Parameter | $V_{CC}$ | Guaranteed Limits | Unit | Condition |
|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High Level Input Voltage[4] | 3.0<br>3.3 | 2.0<br>2.0 | V | $V_{OUT}$ = 0.1V or<br>$V_{CC}$ – 0.1V |
| $V_{IL}$ | Minimum Low Level Input Voltage | 3.0<br>3.3 | 0.8<br>0.8 | V | $V_{OUT}$ = 0.1V or<br>$V_{CC}$ – 0.1V |
| $V_{OH}$ | Minimum High Level Output Voltage | 3.0<br>3.3 | 2.2<br>2.5 | V | $V_{IN}$ = $V_{IH}$ or<br>$V_{IL\ =\ -24mA}$<br>$I_{OH}$ = –24mA |
| $V_{OL}$ | Minimum Low Level Output Voltage | 3.0<br>3.3 | 0.55<br>0.55 | V | $V_{IN}$ = $V_{IH}$ or<br>$V_{IL\ =\ +24mA}$[1]<br>$I_{OH}$ = +24mA |
| $I_{IN}$ | Maximum Input Leakage Current | 3.3 | ±1.0 | µA | $V_I$ = $V_{CC}$, GND |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | 3.3 | 2.0 [2] | mA | $V_I$ = $V_{CC}$ – 2.1V |
| $I_{OLD}$ | Minimum Dynamic[3] Output Current | 3.3 | 50 | mA | $V_{OLD}$ = 1.25V Max |
| $I_{OHD}$ | | 3.3 | –50 | mA | $V_{OHD}$ = 2.35 Min |
| $I_{CC}$ | Maximum Quiescent Supply Current | 3.3 | 750 | µA | $V_I$ = $V_{CC}$, GND |

1. $I_{OL}$ is +12mA for the $\overline{RST}\_\overline{OUT}$ output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration 2.0ms, one output loaded at a time.
4. The MC88LV926 can also be operated from a 5.0V supply. $V_{OH}$ output levels will vary 1:1 with $V_{CC}$, input levels and current specs will be unchanged, except $V_{IH}$; when $V_{CC}$ > 4.0 volts, $V_{IH}$ minimum level is 2.7 volts.

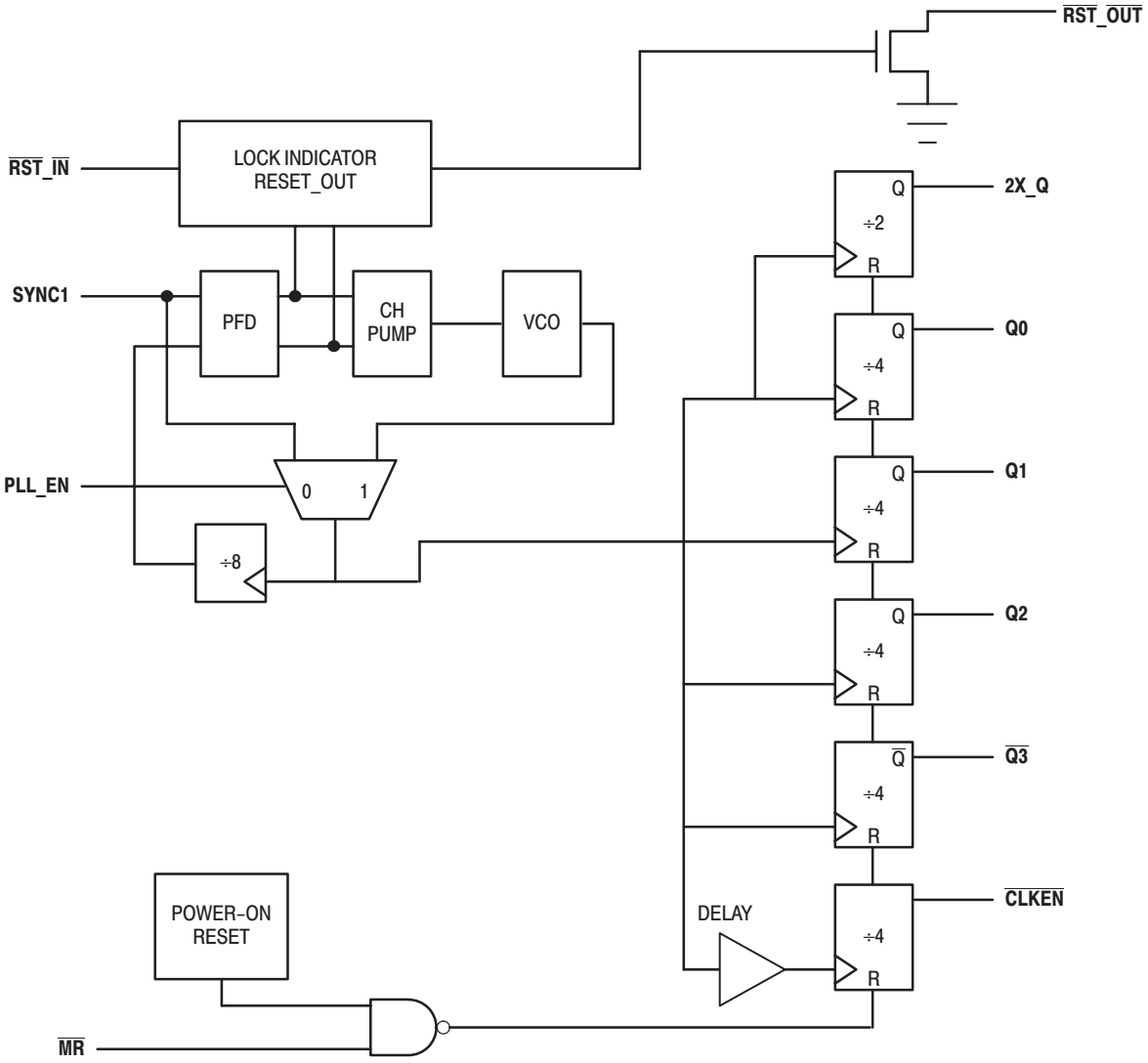



**Figure 2. MC88LV926 Logic Block Diagram**

## SYNC INPUT TIMING REQUIREMENTS

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{RISE/FALL}$ SYNC Input | Rise/Fall Time, SYNC Input From 0.8V to 2.0V | — | 5.0 | ns |
| $t_{CYCLE}$, SYNC Input | Input Clock Period SYNC Input[1] | $\frac{1}{f_{2X\_Q}/4}$ | 200[1] | ns |
| Duty Cycle | Duty Cycle, SYNC Input | 50% ± 25% | | |

1. When $V_{CC}$ > 4.0 volts, Maximum SYNC Input Period is 125ns.

## FREQUENCY SPECIFICATIONS ($T_A$ = 0°C to 70°C; $V_{CC}$ = 3.3V ± 0.3V or 5.0V ±5%)

| Symbol | Parameter | Guaranteed Minimum | Unit |
|---|---|---|---|
| Fmax (2X_Q) | Maximum Operating Frequency, 2X_Q Output | 66 | MHz |
| Fmax ('Q') | Maximum Operating Frequency, Q0–Q3 Outputs | 33 | MHz |

Maximum Operating Frequency is guaranteed with the 88LV926 in a phase–locked condition.

**AC CHARACTERISTICS** ($T_A$ = 0°C to 70°C; $V_{CC}$ = 3.3V ± 0.3V or 5.0V ±5%)

| Symbol | Parameter | Mimimum | Maximum | Unit | Condition |
|---|---|---|---|---|---|
| $t_{RISE/FALL}$ All Outputs | Rise/Fall Time, into 50Ω Load | 0.3 | 1.6 | ns | $t_{RISE}$ – 0.8V to 2.0V<br>$t_{FALL}$ – 2.0V to 0.8V |
| $t_{RISE/FALL}$ 2X_Q Output | Rise/Fall Time into a 50Ω Load | 0.5 | 1.6 | ns | $t_{RISE}$ – 0.8V to 2.0V<br>$t_{FALL}$ – 2.0V to 0.8V |
| $t_{pulse\ width(a)}$[1] (Q0, Q1, Q2, $\overline{Q3}$) | Output Pulse Width<br>Q0, Q1, Q2, Q3 at 1.65V | $0.5t_{cycle}$ – 0.5 | $0.5t_{cycle}$ + 0.5 | ns | 50Ω Load Terminated to $V_{CC}$/2 (See Application Note 3) |
| $t_{pulse\ width(b)}$[1] (2X_Q Output) | Output Pulse Width<br>2X_Q at 1.65V | $0.5t_{cycle}$ – 0.5 | $0.5t_{cycle}$ + 0.5 | ns | 50Ω Load Terminated to $V_{CC}$/2 (See Application Note 3) |
| $t_{SKEWr}$[2] (Rising) | Output–to–Output Skew<br>Between Outputs Q0–Q2<br>(Rising Edge Only) | — | 500 | ps | Into a 50Ω Load Terminated to $V_{CC}$/2 (See Timing Diagram in Figure 4.) |
| $t_{SKEWf}$[2] (Falling) | Output–to–Output Skew<br>Between Outputs Q0–Q2<br>(Falling Edge Only) | — | 1.0 | ns | Into a 50Ω Load Terminated to $V_{CC}$/2 (See Timing Diagram in Figure 4.) |
| $t_{SKEWall}$[2] | Output–to–Output Skew<br>2X_Q, Q0–Q2, $\overline{Q3}$ | — | 750 | ps | Into a 50Ω Load Terminated to $V_{CC}$/2 (See Timing Diagram in Figure 4.) |
| $t_{SKEW}$ QCLKEN[1,2] | Output–to–Output Skew<br>$\overline{QCLKEN}$ to 2X_Q 2X_Q = 50MHz<br>2X_Q = 66MHz | <br>9.7[6]<br>7.0[6] | — | ns | Into a 50Ω Load Terminated to $V_{CC}$/2 (See Timing Diagram in Figure 4.) |
| $t_{LOCK}$[3] | Phase–Lock Acquisition Time,<br>All Outputs to SYNC Input | 1 | 10 | ms | |
| $t_{PHL}$ $\overline{MR}$ – Q[1] | Propagation Delay,<br>$\overline{MR}$ to Any Output (High–Low) | 1.5 | 13.5 | ns | Into a 50Ω Load Terminated to $V_{CC}$/2 |
| $t_{REC}$, $\overline{MR}$ to SYNC[5, 1] | Reset Recovery Time rising $\overline{MR}$ edge to falling SYNC edge | 9 | — | ns | |
| $t_W$, $\overline{MR}$ LOW[5, 1] | Minimum Pulse Width, $\overline{MR}$ input Low | 5 | — | ns | |
| $t_W$, $\overline{RST\_IN}$ LOW[1] | Minimum Pulse Width, $\overline{RST\_IN}$ Low | 10 | — | ns | When in Phase–Lock |
| $t_{PZL}$[1] | Output Enable Time<br>$\overline{RST\_IN}$ Low to $\overline{RST\_OUT}$ Low | 1.5 | 16.5 | ns | See Application Note 5 |
| $t_{PLZ}$[1] | Output Enable Time<br>$\overline{RST\_IN}$ High to $\overline{RST\_OUT}$ High Z | 1016 ‘Q’ Cycles<br>(508 Q/2 Cycles) | 1024 ‘Q’ Cycles<br>(512 Q/2 Cycles) | ns | See Application Note 5 |

1. These specifications are not tested, they are guaranteed by statistical characterization. See Application Note 1 for a discussion of this methodology.
2. Under equally loaded conditions and at a fixed temperature and voltage.
3. With $V_{CC}$ fully powered–on: $t_{CLOCK}$ Max is with C1 = 0.1µF; $t_{LOCK}$ Min is with C1 = 0.01µF.
4. See Application Note 4 for the distribution in time of each output referenced to SYNC.
5. Specification is valid only when the PLL_EN pin is low.
6. Guaranteed that $\overline{QCLKEN}$ will meet the setup and hold time requirement of the 68060.

**Application Notes**

1. Several specifications can only be measured when the MC88LV926 is in phase–locked operation. It is not possible to have the part in phase–lock on ATE (automated test equipment). Statistical characterization techniques were used to guarantee those specifications which cannot be measured on the ATE. MC88LV926 units were fabricated with key transistor properties intentionally varied to create a 14 cell designed experimental matrix. IC performance was characterized over a range of transistor properties (represented by the 14 cells) in excess of the expected process variation of the wafer fabrication area. Response Surface Modeling (RSM) techniques were used to relate IC performance to the CMOS transistor properties over operation voltage and temperature. IC performance to each specification and fab variation were used in conjunction with Yield Surface Modeling™ (YSM™) methodology to set performance limits of ATE testable specifications within those which are to be guaranteed by statistical characterization. In this way, all units passing the ATE test will meet or exceed the non–tested specifications limits.
2. A 470KΩ resistor tied to either Analog $V_{CC}$ or Analog GND, as shown in Figure 1., is required to ensure no jitter is present on the MC88LV926 outputs. This technique causes a phase offset between the SYNC input and the Q0 output, measured at the pins. The $t_{PD}$ spec describes how this offset varies with process, temperature, and voltage. The specs were arrived at by measuring the phase relationship for the 14 lots described in note 1 while the part was in phase–locked operation. The actual measurements were made with a 10MHz SYNC input (1.0ns edge rate from 0.8V to 2.0V). The phase measurements were made at 1.5V. See Figure 1. for a graphical description.
3. Two specs ($t_{RISE/FALL}$ and $t_{PULSE}$ Width 2X_Q output, see AC Specifications) guarantee that the MC88LV926 meets the 33MHz and 66MHz 68060 P–Clock input specification.



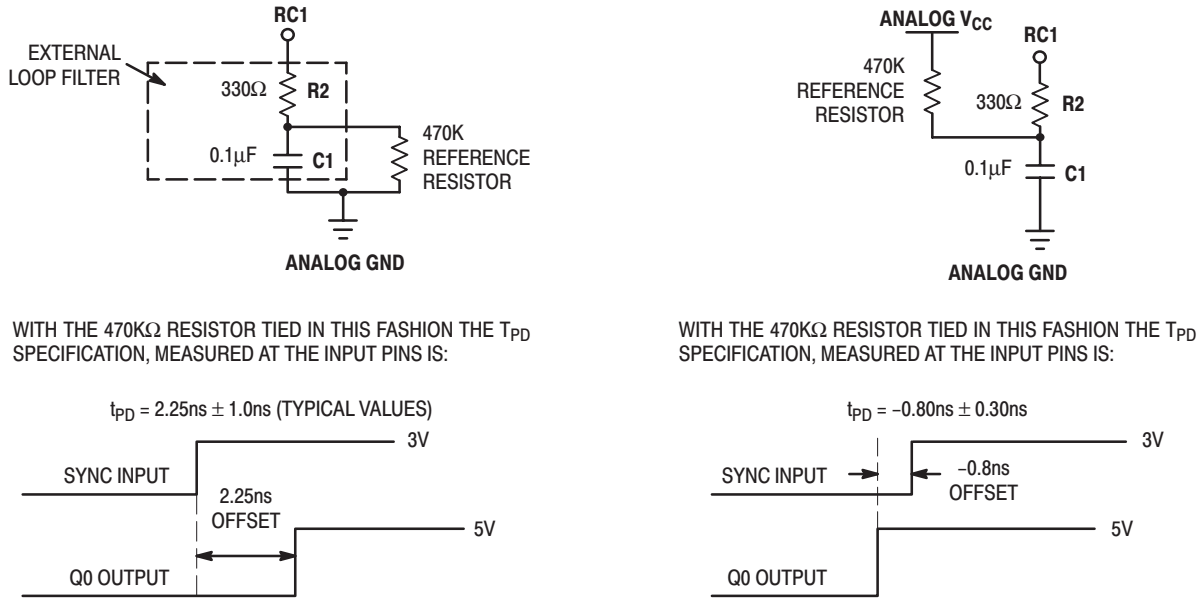



**Figure 1. Depiction of the Fixed SYNC to Q0 Offset ($t_{PD}$) Which Is Present When a 470KΩ Resistor Is Tied to $V_{CC}$ or Ground**

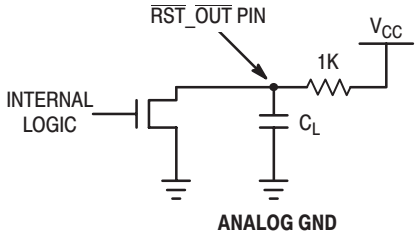



**Figure 2. RST_OUT Test Circuit**



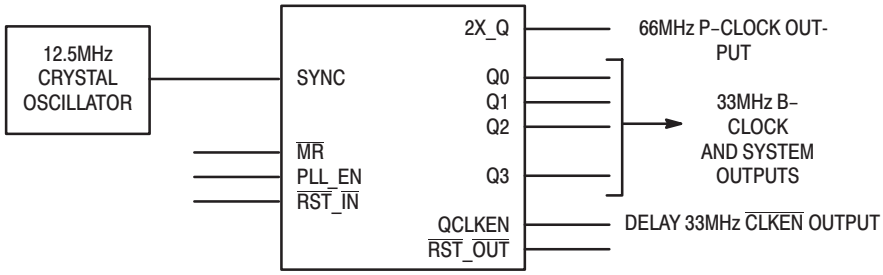



**Figure 3. Logical Representation of the MC88LV926 With Input/Output Frequency Relationships**

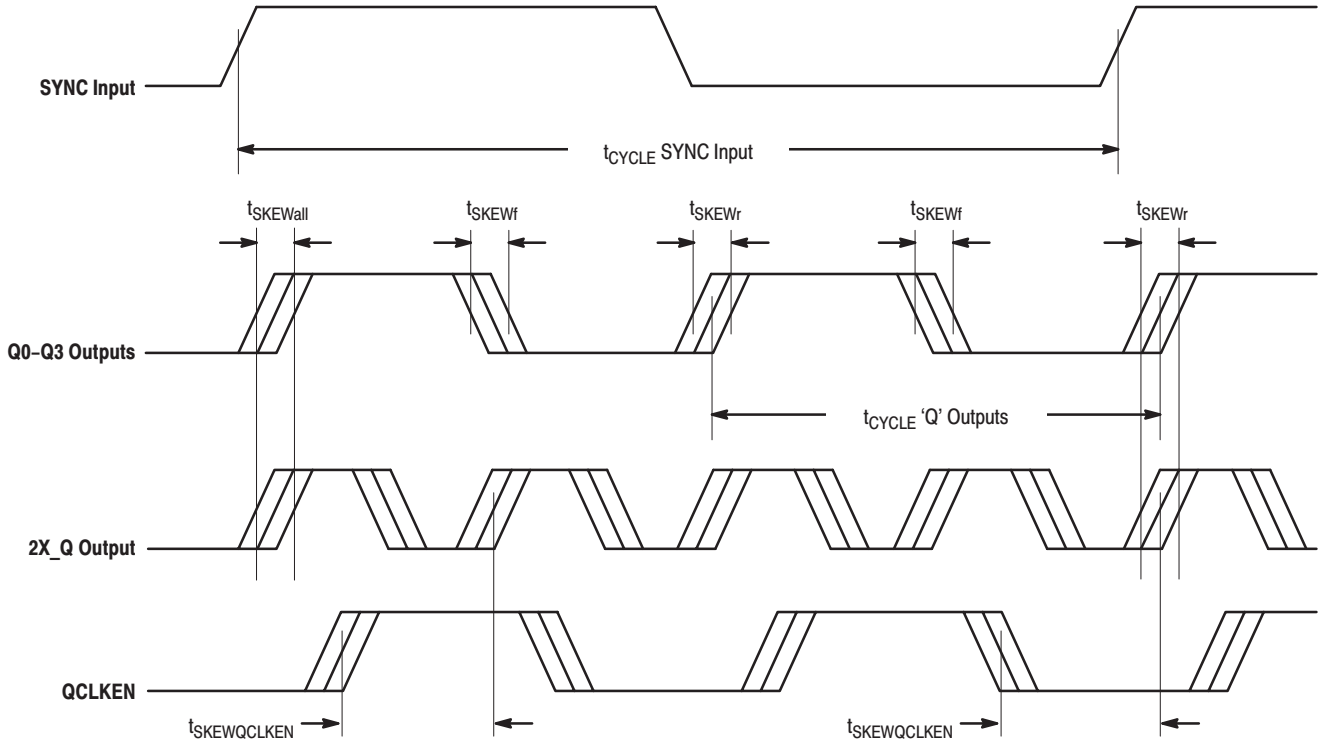



**Figure 4. Output/Input Switching Waveforms and Timing Relationships**

### Timing Notes

1. The MC88LV926 aligns rising edges of the outputs and the SYNC input, therefore the SYNC input does not require a 50% duty cycle.
2. All skew specs are measured between the $V_{CC}/2$ crossing point of the appropriate output edges. All skews are specified as 'windows', not as a ± deviation around a center point.

The $t_{PD}$ spec includes the full temperature range from 0°C to 70°C and the full $V_{CC}$ range from 3.0V to 3.3V. If the $\Delta T$ and $\Delta V_{CC}$ is a given system are less than the specification limits, the $t_{PD}$ spec window will be reduced. The $t_{PD}$ window for a given $\Delta T$ and $\Delta V_{CC}$ is given by the following regression formula:

TBD

**Notes Concerning Loop Filter and Board Layout Issues**

1. Figure 5. shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter–free operation:

1a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the RC1 pin.

1b. The 47Ω resistors, the 10μF low frequency bypass capacitor, and the 0.1μF high frequency bypass capacitor form a wide bandwidth filter that will make the 88LV926 PLL insensitive to voltage transients from the system digital $V_{CC}$ supply and ground planes. This filter will typically ensure that a 100mV step deviation on the digital $V_{CC}$ supply will cause no more than a 100ps phase deviation on the 88LV926 outputs. A 250mV step deviation on $V_{CC}$ using the recommended filter values will cause no more than a 250ps phase deviation; if a 25μF bypass capacitor is used (instead of 10μF) a 250mV $V_{CC}$ step will cause no more than a 100ps phase deviation.

If good bypass techniques are used on a board design near components which may cause digital $V_{CC}$ and ground noise, the above described $V_{CC}$ step deviations should not occur at the 88LV926's digital $V_{CC}$ supply. The purpose of the bypass filtering scheme shown in Figure 5. is to give the 88LV926 additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.

1c. There are no special requirements set forth for the loop filter resistors (470K and 330Ω). The loop filter capacitor (0.1uF) can be a ceramic chip capacitor, the same as a standard bypass capacitor.

1d. The 470K reference resistor injects current into the internal charge pump of the PLL, causing a fixed offset between the outputs and the SYNC input. This also prevents excessive jitter caused by inherent PLL dead–band. If the VCO (2X_Q output) is running above 40MHz, the 470K resistor provides the correct amount of current injection into the charge pump (2–3μA). If the VCO is running below 40MHz, a 1MΩ reference resistor should be used (instead of 470K).

2. In addition to the bypass capacitors used in the analog filter of Figure 5., there should be a 0.1μF bypass capacitor between each of the other (digital) four $V_{CC}$ pins and the board ground plane. This will reduce output switching noise caused by the 88LV926 outputs, in addition to reducing potential for noise in the 'analog' section of the chip. These bypass capacitors should also be tied as close to the 88LV926 package as possible.

5. The $\overline{RST}\_\overline{OUT}$ pin is an open drain N–Channel output. Therefore an external pull–up resistor must be provide to pull up the $\overline{RST}\_\overline{OUT}$ pin when it goes into the high impedance state (after the MC88LV926 is phase–locked to the reference input with $\overline{RST}\_\overline{IN}$ held high or 1024 'Q' cycles after the $\overline{RST}\_\overline{IN}$ pin goes high when the part is locked). In the $t_{PLZ}$ and $t_{PZL}$ specifications, a 1KΩ resistor is used as a pull–up as shown in Figure 2.

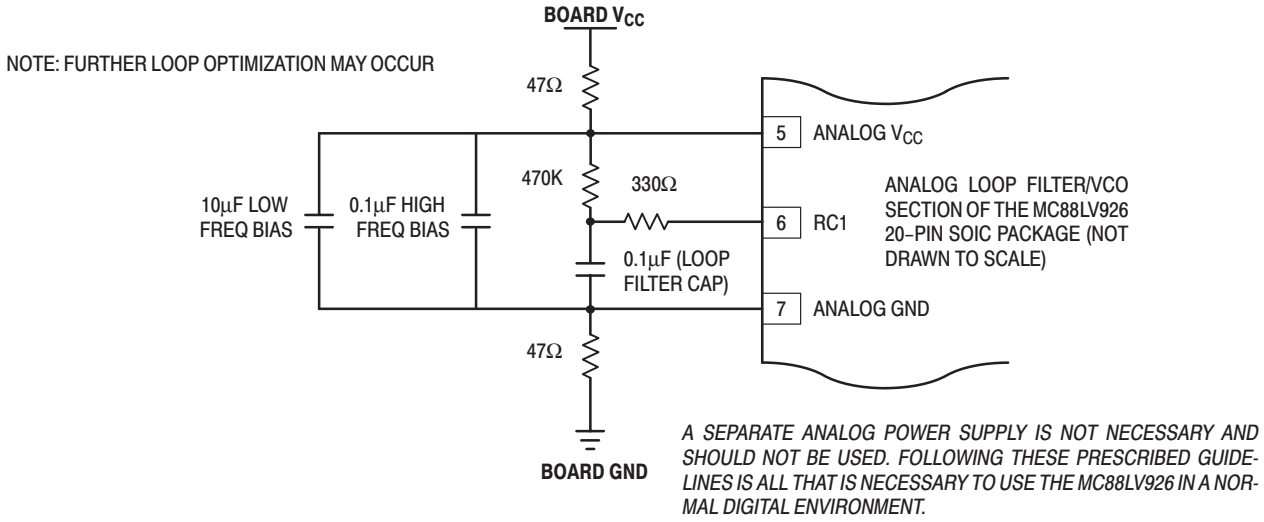



**Figure 5. Recommended Loop Filter and Analog Isolation Scheme for the MC88LV926**

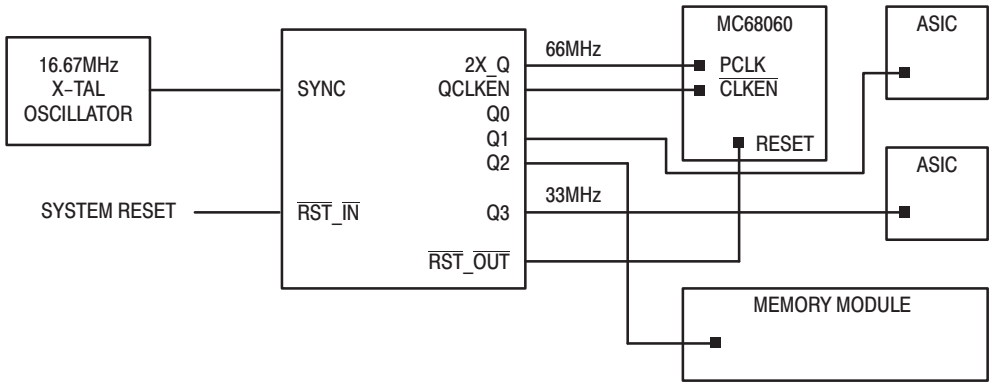



**Figure 6. Typical MC88LV926/MC68060 System Configuration**

# Low Voltage PLL Clock Driver

**MPC930**
**MPC931**

**See Upgrade Products – MPC9330/MPC9331**

2

**LOW VOLTAGE**
**PLL CLOCK DRIVER**

**FA SUFFIX**
32–LEAD TQFP PACKAGE
CASE 873A–02

The MPC930/931 is a 3.3V compatible, PLL based clock driver device targeted for high performance clock applications. With output frequencies of up to 150MHz and output skews of 300ps the MPC930/931 is ideal for the most demanding clock distribution designs. The device employs a fully differential PLL design to minimize cycle to cycle and long term jitter. This parameter is of significant importance when the clock driver is providing the reference clock for PLL's on board todays microprocessors and ASiC's. The device offers 6 low skew outputs, and a choice between internal or external feedback. The feedback option adds to the flexibility of the device, providing numerous input to output frequency relationships.

- On–Board Crystal Oscillator (MPC930)
- Differential LVPECL Reference Input (MPC931)
- Fully Integrated PLL
- Output Shut Down Mode
- Output Frequency up to 150MHz
- Compatible with **PowerPC**™ and Intel Microprocessors
- 32–Lead TQFP Packaging
- Power Down Mode
- ±100ps Typical Cycle–to–Cycle Jitter

The MPC930 and MPC931 are very similar in basic functionality, but there are some minor differences. The MPC931 has been optimized for use as a zero delay buffer. In addition to tighter specification limits on the phase offset of the device, a higher speed VCO has been used on the MPC931. The MPC930, on the other hand, is more optimized for use as a clock generator. When choosing between the 930 and 931, pay special attention to the differences in the AC parameters of each device.

The MPC930/931 offers two power saving features for power conscious portable or "green" designs. The power down pin will seemlessly reduce all of the clock rates by one half so that the system will run at half the potential clock rate to extend battery life. The POWER_DN pin is synchronized internally to the slowest output clock rate. This allows the transition in and out of the power–down mode to be output glitch free. In addition, the shut down control pins will turn off various combinations of clock outputs while leaving a subset active to allow for total processor shut down while maintaining system monitors to "wake up" the system when signaled. During shut down, the PLL will remain locked, if internal feedback is used, so that wake up time will be minimized. The shut down and power down pins can be combined for the ultimate in power savings. The Shut_Dn pins are synchronized to the clock internal to the chip to eliminate the possibility of generating runt pulses.

The MPC930/931 devices offer a great deal of flexibility in what is used as the PLL reference. The MPC930 offers an integrated crystal oscillator that allows for an inexpensive crystal to be used as the frequency reference. For more information on the crystal oscillator please refer to the applications section of this data sheet. In those applications where the 930/931 will be used to regenerate clocks from an existing source or as a zero delay buffer, alternative reference clock inputs are provided. Both devices offer an LVCMOS input that can be used as the PLL reference. In addition the MPC931 replaces the crystal oscillator inputs with a differential PECL reference clock input that allows the device to be used in mixed technology clock distribution trees.

An internal feedback divide by 8 of the VCO frequency is compared with the input reference provided by the on–board crystal oscillator when the internal feedback is selected. The on–board crystal oscillator requires no external components other than a series resonant crystal (see Applications Information section for more on crystals). The internal VCO is running at 8x the input reference clock. The outputs can be configured to run at 4x, 2x, 1.25x or 0.66x the input reference frequency. If the external feedback is selected, one of the MPC931's outputs must be connected to the Ext_FB pin. Using the external feedback, numerous input/output frequency relationships can be developed.

The MPC930/931 is fully 3.3V compatible and requires no external loop filter components. All control inputs accept LVCMOS or LVTTL compatible levels while the outputs provide LVCMOS levels with the capability to drive terminated 50Ω transmission lines. For series terminated applications, each output can drive two 50Ω transmission lines, effectively increasing the fanout to 1:12. The device is packaged in a 32–lead TQFP package to provide the optimum combination of board density and cost.



**Rev 4**

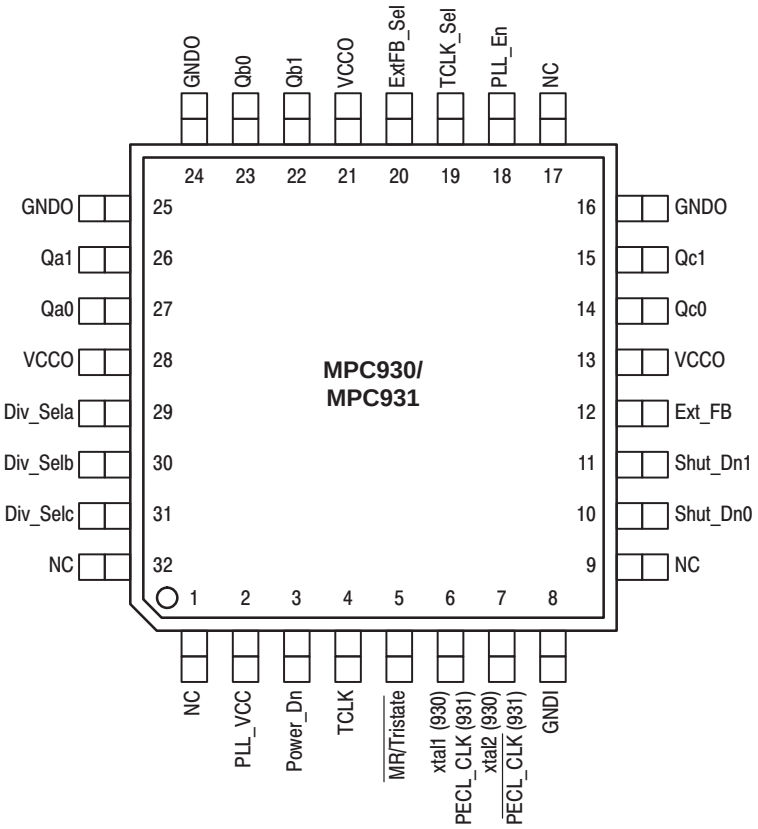



**Figure 1. 32–Lead Pinout** (Top View)

**FUNCTION TABLES**

| TCLK_Sel | Reference |
|---|---|
| 0 | xtal (PECL_CLK) |
| 1 | TCLK |

| PLL_En | PLL Status |
|---|---|
| 0 | Test Mode |
| 1 | PLL Enabled |

| ExtFB_Sel | Reference |
|---|---|
| 0 | Int. ÷8 |
| 1 | Ext_FB |

| Power_Dn | PLL Status |
|---|---|
| 0 | VCO/1 |
| 1 | VCO/2 |

| Div_Sela,b,c | Qa | Qb | Qc |
|---|---|---|---|
| 0 | ÷2 | ÷2 | ÷4 |
| 1 | ÷4 | ÷4 | ÷6 |

| $\overline{\text{MR}}$/Tristate | PLL Status |
|---|---|
| 0 | Disabled |
| 1 | Enabled |

| Shut_Dn1 | Shut_Dn0 | Div_Seln |
|---|---|---|
| 0 | 0 | Qb & Qc Low, Qa Toggle |
| 0 | 1 | Qa & Qb Low, Qc Toggle |
| 1 | 0 | Qb Low, Qa & Qc Toggle |
| 1 | 1 | All Toggle |

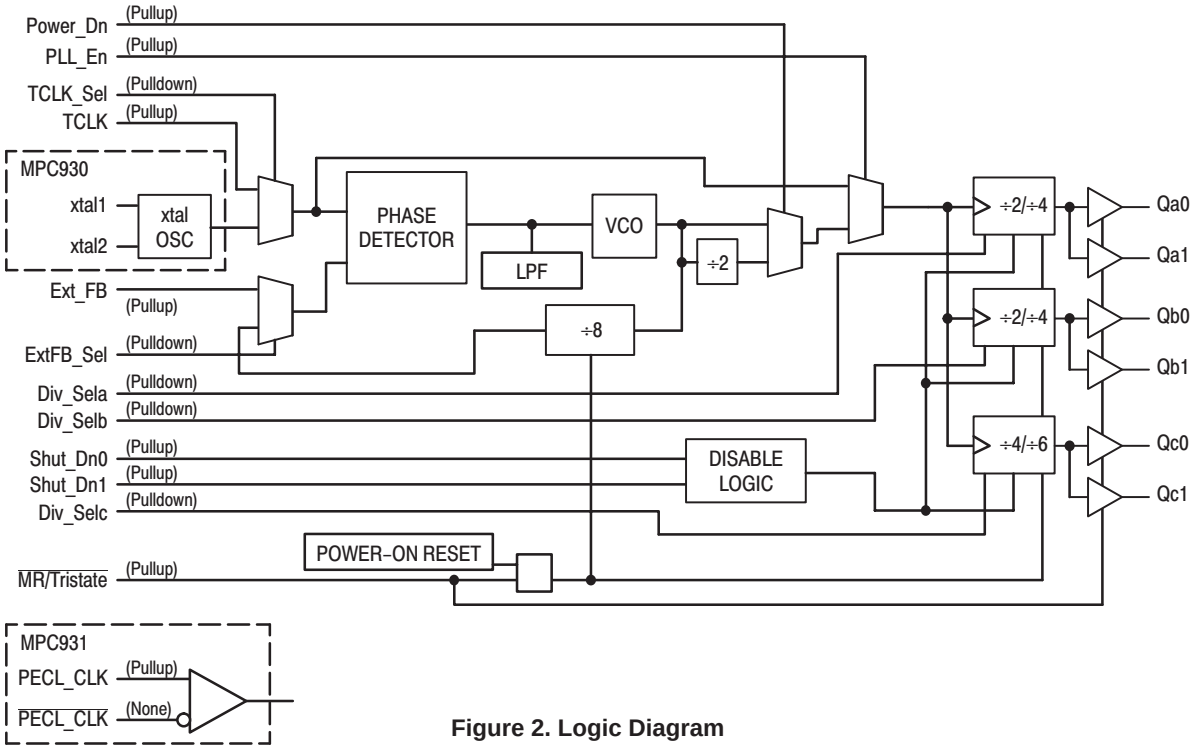



**Figure 2. Logic Diagram**

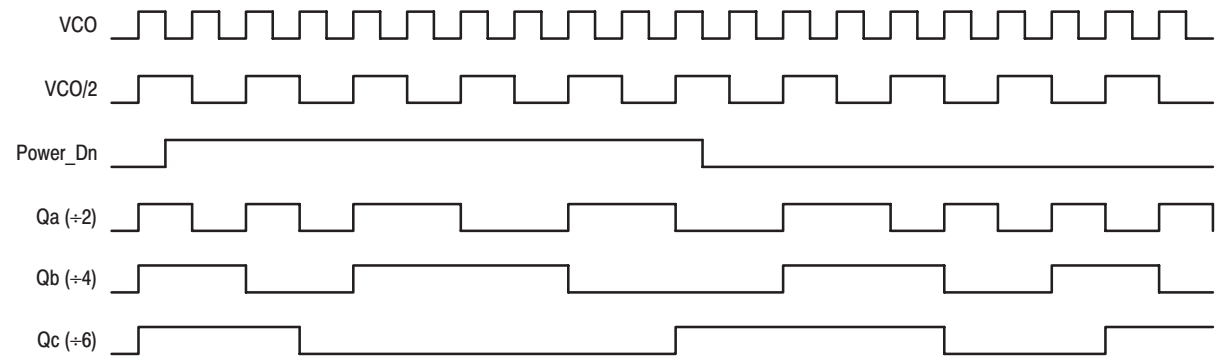



**Figure 3. Power_Dn Timing Diagram**

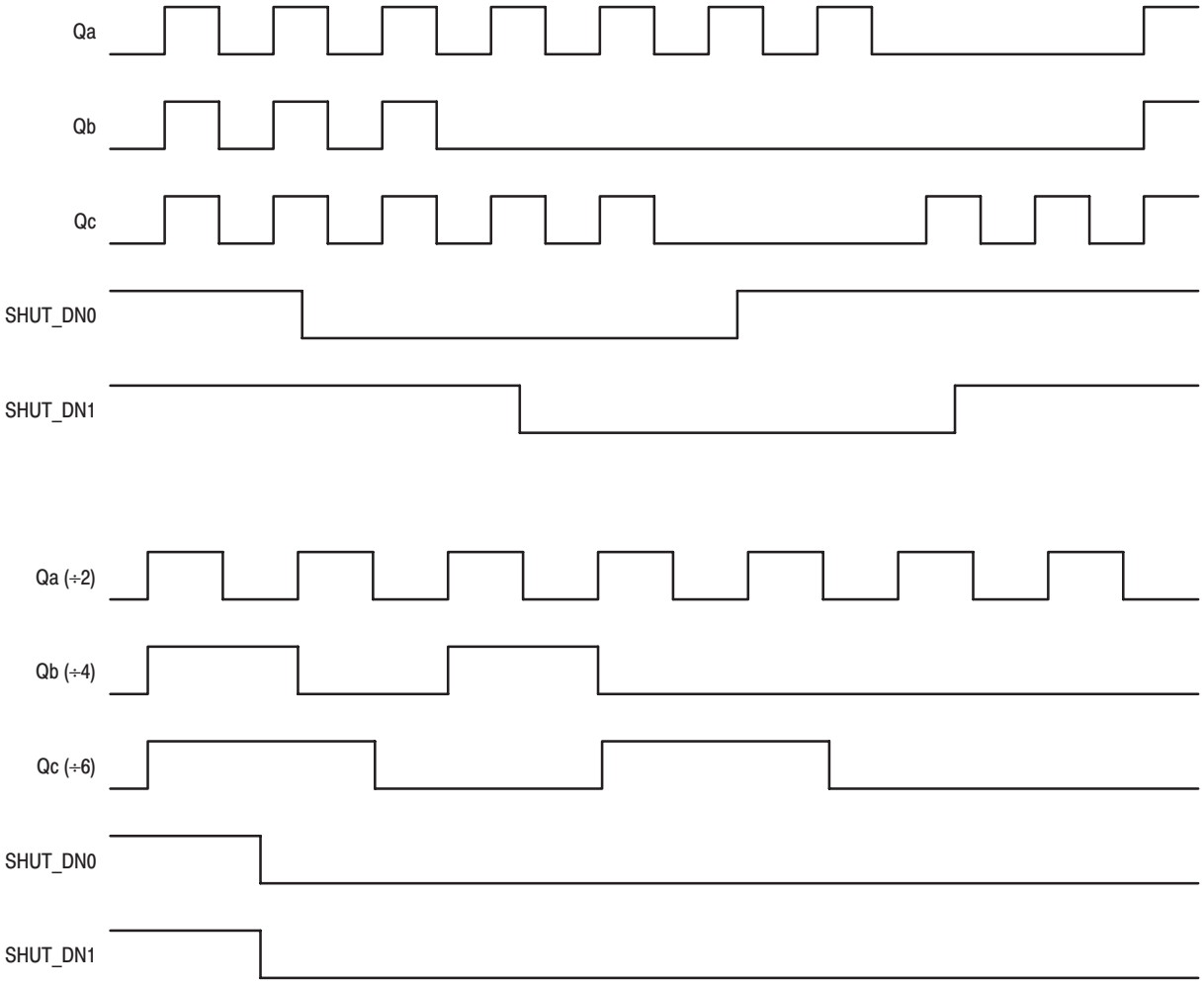



**Figure 4. Shut_Dn Timing Diagram**

**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 4.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_{IN}$ | Input Current | | ±20 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |



* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

**PLL INPUT REFERENCE CHARACTERISTICS** ($T_A$ = 0 to 70°C)

| Symbol | Characteristic | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $t_r$, $t_f$ | TCLK Input Rise/Falls | | 3.0 | ns | |
| $f_{ref}$ | Reference Input Frequency | 10 | Note 1. | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | 25 | 75 | % | |

1. Maximum input reference frequency is limited by the VCO lock range and the feedback divider.

**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | 3.6 | V | |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | $I_{OH}$ = –20mA (Note 2.) |
| $V_{OL}$ | Output LOW Voltage | | | 0.5 | V | $I_{OL}$ = 20mA (Note 2.) |
| $I_{IN}$ | Input Current | | | ±120 | µA | Note 3. |
| $I_{CC}$ | Maximum Core Supply Current | | 65 | 85 | mA | |
| $I_{CCPLL}$ | Maximum PLL Supply Current | | 15 | 20 | mA | |
| $C_{IN}$ | | | | 4 | pF | |
| $C_{pd}$ | | | 25 | | pF | Per Output |

2. The MPC930/931 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}$/2) transmission lines on the incident edge (see Applications Info section).
3. Inputs have pull–up/pull–down resistors which affect input current.

**MPC930 AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $f_{xtal}$ | Crystal Oscillator Frequency Range | 10 | | 20 | MHz | Note 5., Note 7. |
| $f_{ref}$ | Input Reference Frequency | Note 7. | | Note 7. | MHz | Ref = TCLK |
| $t_{os}$ | Output–to–Output Skew Same Frequency<br>(Note 4.) Diff Frequency<br>Same Frequency<br>Diff Frequency | | 200<br>300<br>300<br>450 | 300<br>400<br>400<br>600 | ps | $f_{max} \leq$ 100MHz<br>$f_{max} \leq$ 100MHz<br>$f_{max}$ > 100MHz<br>$f_{max}$ > 100MHz |
| $f_{VCO}$ | VCO Lock Range | 100 | | 280 | MHz | |
| $f_{max}$ | Maximum Output Frequency Qa, Qb (÷2)<br>Qa, Qb, Qc (÷4)<br>Qc (÷6) | | | 140<br>80<br>47 | MHz | Note 4. |
| $t_{pd}$ | TCLK to EXT_FB Delay | –600 | –100 | 400 | ps | $f_{ref}$ = 50MHz, FB = ÷4 |
| $t_{pw}$ | Output Duty Cycle (Note 4.) | $t_{CYCLE}$/2 –750 | $t_{CYCLE}$/2 ±500 | $t_{CYCLE}$/2 +750 | ps | |
| $t_r$, $t_f$ | Output Rise/Fall Time (Note 4.) | 0.1 | | 1.0 | ns | 0.8 to 2.0V |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time | 2.0 | | 8.0 | ns | 50Ω to $V_{CC}$/2 |
| $t_{PZL}$ | Output Enable Time | 2.0 | | 10 | ns | 50Ω to $V_{CC}$/2 |
| $t_{jitter}$ | Cycle–to–Cycle Jitter (Peak–to–Peak) | | ±100 | | ps | Note 6. |
| $t_{lock}$ | Maximum PLL Lock Time | | | 10 | ms | |

4. Measured with 50Ω to $V_{CC}$/2 termination.
5. See Applications Info section for more Crystal specifications.
6. See Applications Info section for more jitter information.
7. Input reference frequency is bounded by VCO lock range and feedback divide selection.

**MPC931 AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Reference Frequency | Note 11. | | Note 11. | MHz | |
| $t_{os}$ | Output–to–Output Skew Same Frequency<br>(Note 8.) Diff Frequency<br>Same Frequency<br>Diff Frequency | | 200<br>300<br>300<br>450 | 300<br>400<br>400<br>600 | ps | $f_{max} \leq$ 100MHz<br>$f_{max} \leq$ 100MHz<br>$f_{max}$ > 100MHz<br>$f_{max}$ > 100MHz |
| $f_{VCO}$ | VCO Lock Range | 200 | | 480 | MHz | |
| $f_{max}$ | Maximum Output Frequency Qa, Qb (÷2)<br>Qa, Qb, Qc (÷4)<br>Qc (÷6) | | | 150<br>120<br>80 | MHz | Note 9. |
| $t_{pd}$ | Reference to EXT_FB Average Delay TCLK<br>PECL_CLK | –150<br>–400 | 0<br>–250 | +150<br>–100 | ps | $f_{ref}$ = 50MHz; FB = ÷8;<br>Note 12. |
| $t_{pw}$ | Output Duty Cycle (Note 8.) | $t_{CYCLE}$/2 –750 | $t_{CYCLE}$/2 ±500 | $t_{CYCLE}$/2 +750 | ps | |
| $t_r$, $t_f$ | Output Rise/Fall Time (Note 8.) | 0.1 | | 1.0 | ns | 0.8 to 2.0V |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time | 2.0 | | 8.0 | ns | 50Ω to $V_{CC}$/2 |
| $t_{PZL}$ | Output Enable Time | 2.0 | | 10 | ns | 50Ω to $V_{CC}$/2 |
| $t_{jitter}$ | Cycle–to–Cycle Jitter (Peak–to–Peak) | | ±100 | | ps | Note 10. |
| $t_{lock}$ | Maximum PLL Lock Time | | | 10 | ms | |

8. Measured with 50Ω to $V_{CC}$/2 termination.
9. $f_{max}$ limited by skew spec. Outputs will generate valid CMOS signals up to 180MHz.
10. See Applications Info section for more jitter information.
11. Input reference frequency is bounded by VCO lock range and feedback divide selection.
12. $t_{pd}$ is specified for 50MHz input reference, the window will shrink/grow proportionally from the minimum limit with shorter/linger reference periods. The $t_{pd}$ does not include jitter.

## APPLICATIONS INFORMATION

### Programming the MPC930/931

The MPC930/931 clock driver outputs can be configured into several frequency relationships, in addition the external feedback option allows for a great deal of flexibility in establishing unique input to output frequency relationships. The output dividers for the three output groups allows the user to configure the outputs into 1:1, 2:1, 3:1, 3:2 and 3:2:1 frequency ratios. The use of even dividers ensures that the output duty cycle is always 50%. Table 1 illustrates the various output configurations, the table describes the outputs using the VCO frequency as a reference. As an example for a 3:2:1 relationship the Qa outputs would be set at VCO/2, the Qb's at VCO/4 and the Qc's at VCO/6. These settings will provide output frequencies with a 3:2:1 relationship.

The division settings establish the output relationship, but one must still ensure that the VCO will be stable given the frequency of the outputs desired. The VCO lock range can be found in the specification tables. The feedback frequency and the Power_Dn pin can be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL is such that for output frequencies between 25 and 180MHz the MPC930/931 can generally be configured into a stable region.

The relationship between the input reference and the output frequency is also very flexible. Table 2 shows the multiplication factors between the inputs and outputs when the internal feedback option is used. For external feedback Table 1 can be used to determine the multiplication factor, there are too many potential combinations to tabularize the external feedback condition. Figure 5 through Figure 10 illustrates several programming possibilities, although not exhaustive it is representative of the potential applications.

**Table 1. Programmable Output Frequency Relationships** (Power_Dn = '0')

| INPUTS | | | OUTPUTS | | |
|---|---|---|---|---|---|
| **Div_Sela** | **Div_Selb** | **Div_Selc** | **Qa** | **Qb** | **Qc** |
| 0 | 0 | 0 | VCO/2 | VCO/2 | VCO/4 |
| 0 | 0 | 1 | VCO/2 | VCO/2 | VCO/6 |
| 0 | 1 | 0 | VCO/2 | VCO/4 | VCO/4 |
| 0 | 1 | 1 | VCO/2 | VCO/4 | VCO/6 |
| 1 | 0 | 0 | VCO/4 | VCO/2 | VCO/4 |
| 1 | 0 | 1 | VCO/4 | VCO/2 | VCO/6 |
| 1 | 1 | 0 | VCO/4 | VCO/4 | VCO/4 |
| 1 | 1 | 1 | VCO/4 | VCO/4 | VCO/6 |

**Table 2. Input Reference/Output Frequency Relationships** (Internal Feedback Only)

| INPUTS | | | OUTPUTS | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | **Qa** | | **Qb** | | **Qc** | |
| **Div_Sela** | **Div_Selb** | **Div_Selc** | **Power_Dn=0** | **Power_Dn=1** | **Power_Dn=0** | **Power_Dn=1** | **Power_Dn=0** | **Power_Dn=1** |
| 0 | 0 | 0 | 4x | 2x | 4x | 2x | 2x | x |
| 0 | 0 | 1 | 4x | 2x | 4x | 2x | 4/3x | 2/3x |
| 0 | 1 | 0 | 4x | 2x | 2x | x | 2x | x |
| 0 | 1 | 1 | 4x | 2x | 2x | x | 4/3x | 2/3x |
| 1 | 0 | 0 | 2x | x | 4x | 2x | 2x | x |
| 1 | 0 | 1 | 2x | x | 4x | 2x | 4/3x | 2/3x |
| 1 | 1 | 0 | 2x | x | 2x | x | 2x | x |
| 1 | 1 | 1 | 2x | x | 2x | x | 4/3x | 2/3x |

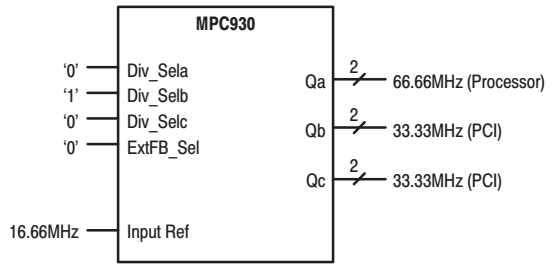



**Figure 5. Dual Frequency Configuration**

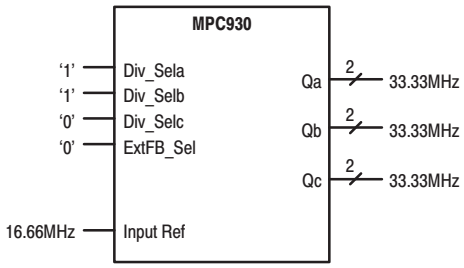



**Figure 6. Single Frequency Configuration**



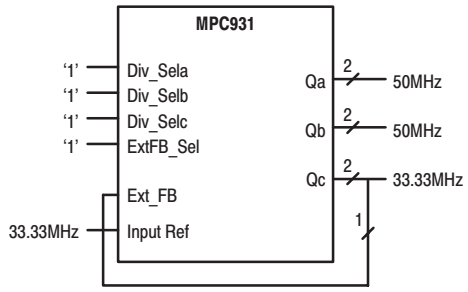



**Figure 7. "Zero" Delay Fractional Multiplier**

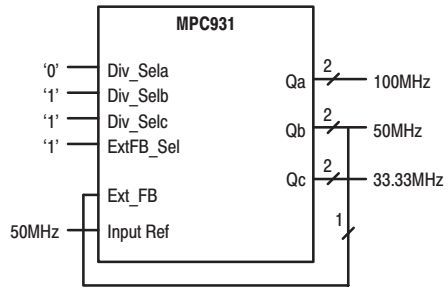



**Figure 8. "Zero" Delay Fractional Divider**

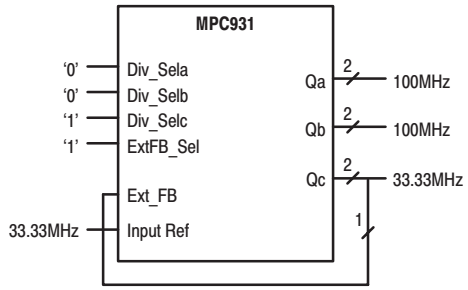



**Figure 9. "Zero" Delay Multiply by 3** (50% Duty Cycle)

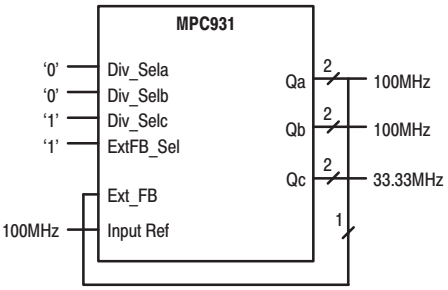



**Figure 10. "Zero" Delay Divide by 3** (50% Duty Cycle)

**Using the MPC930/931 as a Zero Delay Buffer**

The external feedback option of the MPC930/931 clock driver allows for its use as a zero delay buffer. By using one of the outputs as a feedback to the PLL the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The Tpd of the device is specified in the specification tables. For zero delay buffer applications, the MPC931 is recommended over the MPC930. The MPC931 has been optimized and specified specifically for use as a zero delay buffer.

When used as a zero delay buffer the MPC930/931 will likely be in a nested clock tree application. For these applications the MPC931 offers a LVPECL clock input as a PLL reference. This allows the user to use LVPECL as the primary clock distribution device to take advantage of its far superior skew performance. The MPC931 then can lock onto the LVPECL reference and translate with near zero delay to low skew LVCMOS outputs. Clock trees implemented in this fashion will show significantly tighter skews than trees developed from CMOS fanout buffers.

To minimize part–to–part skew the external feedback option again should be used. The PLL in the MPC931 decouples the delay of the device from the propagation delay variations of the internal gates. From the specification table one sees a Tpd variation of only ±150ps, thus for multiple devices under identical configurations the part–to–part skew will be around 850ps (300ps for Tpd variation plus 300ps output–to–output skew plus 250ps jitter). For devices that are configured differently the differences between the nominal delays must also be accounted for.

2

When using the MPC931 as a zero delay buffer there is more information which can help minimize the overall timing uncertainty. To fully minimize the specified uncertainty, it is crucial that the relative position of the outputs be known. It is recommended that if all of the outputs are going to be used that the Qc0 output be used as the feedback reference. The Qc0 output lies in the middle of the other outputs with respect to output skew. Therefore it can be assumed that the output to output skew of the device is ±150ps with respect to output Qc0.

There will be some cases where only a subset of the outputs of the MPC931 are required. There is significantly tighter skew performance between outputs on a common bank (i.e., Qa0 to Qa1). The skews between these common bank outputs are outlined in the table below. In general the skews between outputs on a given bank is about a third of the skew between all banks, reducing the skew to a value of 100ps.

**Table 3. Within–Bank Skews**

| Outputs | Relative Skews |
|---|---|
| Qa0 → Qa1 | +35ps, ±50ps |
| Qb0 → Qb1 | –30ps, ±50ps |
| Qc0 → Qc1 | 20ps, ±50ps |

**Jitter Performance of the MPC930/931**

With the clock rates of today's digital systems continuing to increase more emphasis is being placed on clock distribution design and management. Among the issues being addressed is system clock jitter and how that affects the overall system timing budget. The MPC930/931 was designed to minimize clock jitter by employing a differential bipolar PLL as well as incorporating numerous power and ground pins in the design. The following few paragraphs will outline the jitter performance of the MPC930/931, illustrate the measurement limitations and provide guidelines to minimize the jitter of the device.

The most commonly specified jitter parameter is cycle–to–cycle jitter. Unfortunately with today's high performance measurement equipment there is no way to measure this parameter for jitter performance in the class demonstrated by the MPC930/931. As a result different methods are used which approximate cycle–to–cycle jitter. The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak–to–peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. If this is not the case the measurement inaccuracy will add significantly to the measured jitter. The oscilloscope cannot collect adjacent pulses, rather it collects data from a very large sample of pulses. It is safe to assume that collecting pulse information in this mode will produce jitter values somewhat larger than if consecutive cycles were measured, therefore, this measurement will represent an upper bound of cycle–to–cycle jitter. Most likely, this is a conservative estimate of the cycle–to–cycle jitter.

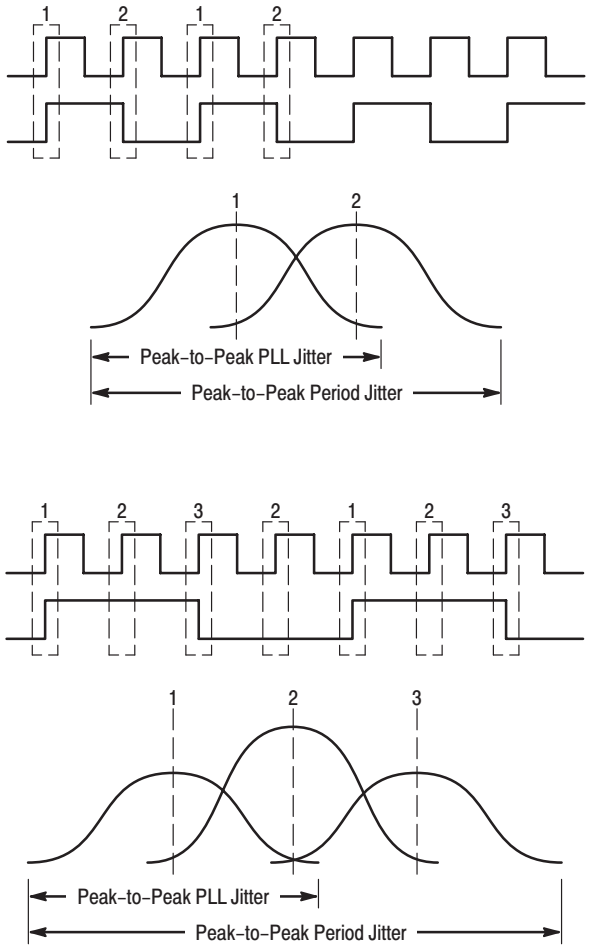
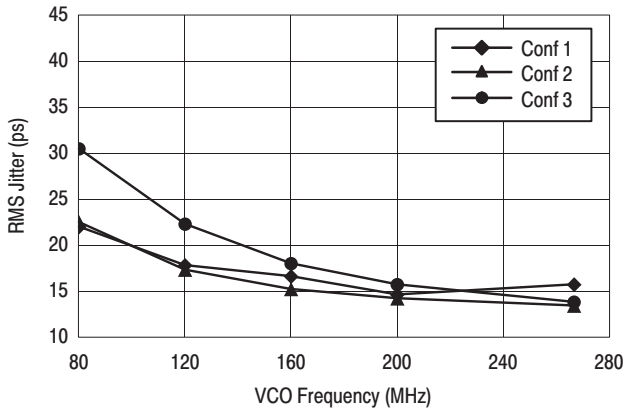



**Figure 11. PLL Jitter and Edge Displacement**

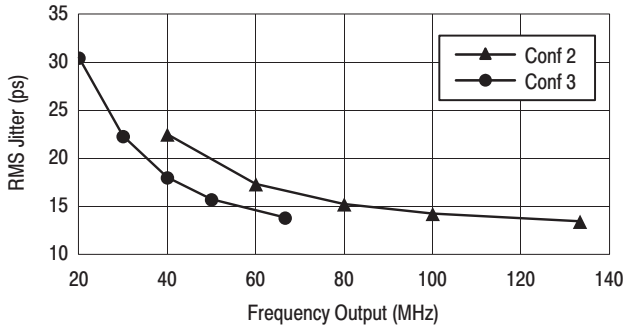
There are two sources of jitter in a PLL based clock driver, the commonly known random jitter of the PLL and the less intuitive jitter caused by synchronous, different frequency outputs switching. For the case where all of the outputs are switching at the same frequency the total jitter is exactly equal to the PLL jitter. In a device, like the MPC930/931, where a number of the outputs can be switching synchronously but at different frequencies a "multi–modal" jitter distribution can be seen on the highest frequency outputs. Because the output being monitored is affected by the activity on the other outputs it is important to consider what is happening on those other outputs. From Figure 11, one can see for each rising edge on the higher frequency signal the activity on the lower frequency signal is not constant. The activity on the other outputs tends to alter the internal thresholds of the device such that the placement of the edge being monitored is displaced in time. Because the signals are synchronous the relationship is periodic and the resulting jitter is a compilation of the PLL jitter superimposed on the displaced edges. When histograms are plotted the jitter looks like a "multi–modal" distribution as pictured in Figure 11 on page 54. Depending on the size of the PLL jitter and the relative displacement of the edges the "multi–modal" distribution will appear truly "multi–modal" or simply like a "fat" Gaussian distribution. Again note that in the case where all the outputs are switching at the same frequency there is no edge displacement and the jitter is reduced to that of the PLL.

Figure 12 graphically represents the PLL jitter of the MPC930/931. The data was taken for several different output configurations. Because of the relatively few outputs on the MPC930/931, the multimodal distribution is of a second order affect on the 930/931 and can be ignored. As one can see in the figure the PLL jitter is much less dependent on output configuration than on internal VCO frequency. However, for a given VCO frequency, a lower output frequency produces more jitter.




Conf 1 = Qa=÷2, Qb=Qc=÷4
Conf 2 = Qa=÷2, Qb=Qc=Shut Down
Conf 3 = Qa=÷4, Qb=Qc=Shut Down

**Figure 12. RMS Jitter versus VCO Frequency**
(Qa0 Output)




Conf 2 = Qa=÷2, Qb=Qc=Shut Down
Conf 3 = Qa=÷4, Qb=Qc=Shut Down

**Figure 13. RMS Jitter versus Output Frequency**
(Qa0 Output)

Finally from the data there are some general guidelines that, if followed, will minimize the output jitter of the device. First and foremost always configure the device such that the VCO runs as fast as possible. This is by far the most critical parameter in minimizing jitter. Second keep the reference frequency as high as possible. More frequent updates at the phase detector will help to reduce jitter. Note that if there is a tradeoff between higher reference frequencies and higher VCO frequency always chose the higher VCO frequency to minimize jitter. The third guideline is to try to shut down outputs that are unused. Minimizing the number of switching outputs will minimize output jitter.

**Power Supply Filtering**

The MPC930/931 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC930/931 provides separate power supplies for the output buffers ($V_{CCO}$) and the internal PLL (PLL_VCC) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the PLL_VCC pin for the MPC930/931.

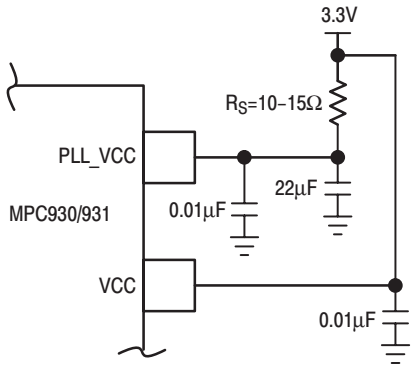



**Figure 14. Power Supply Filter**

Figure 14 illustrates a typical power supply filter scheme. The MPC930/931 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the PLL_VCC pin of the MPC930/931. From the data sheet the $I_{PLL\_VCC}$ current (the current sourced through the PLL_VCC pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the PLL_VCC pin very little DC voltage drop can be tolerated when a 3.3V $V_{CC}$ supply is used. The resistor shown in Figure 14 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

Although the MPC930/931 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Using the Power Management Features of the MPC930/931**

The MPC930/931 clock driver offers two different features that designers can take advantage of for managing power dissipation in their designs. The first feature allows the user to turn off outputs which drive portions of the system which may go idle in a sleep mode. The Shut_Dn pins allow for three different combinations of output shut down schemes. The schemes are summarized in the function tables in the data sheet. The MPC930/931 synchronizes the shut down signals internal to the chip and applies them in a manner which eliminates the possibility of creating runt pulse on the outputs. The device waits for the output to go into the “LOW” state prior to disabling. When the outputs are re–enabled the device waits and re–enables the output such that the transition is synchronous and in the proper phase relationship to the outputs which remained active.

The Power_Dn pin offers another means of implementing power management schemes into a design. To use this feature the device must be set up in its normal operating mode with the Power_Dn pin “LOW”, in addition the user must use the internal feedback option. If the external feedback option were used the output frequency reduction would change the feedback frequency and the PLL will lose lock. When the Power_Dn pin is driven “HIGH” the MPC930/931 synchronizes the signal to the internal clock and then seemlessly reduces the frequency of the outputs by one half. The Power_Dn signal is synchronized to the slowest internal VCO clock. It waits until both VCO clocks are in the “LOW” state and then switches from the nominal speed VCO clock to the half speed VCO clock. This will in turn cause the current output pulse to stretch to reflect the reduction in output frequency. When the Power_Dn pin is brought back “LOW” the device will again wait until both of the VCO clocks are “LOW” and then switch to the nominal VCO clock. This will cause the current output pulses, and all successive pulses, to shrink to match the higher output frequency. Both the power up and power down features are illustrated in the timing diagrams of in this data sheet.

Timing diagrams for both of the power management features are shown in Figure 3 and Figure 4 on page 49**.**

**Using the On–Board Crystal Oscillator**

The MPC930 features an on–board crystal oscillator to allow for seed clock generation as well as final distribution. The on–board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC930/931 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required.

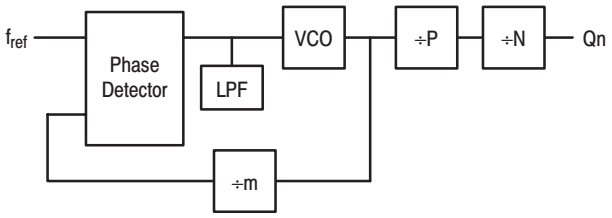
The oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on–board capacitors. Because the design is a series resonant design for the optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most off the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC930 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implement– ations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

**Table 4. Crystal Specifications**

| Parameter | Value |
|---|---|
| Crystal Cut | Fundamental AT Cut |
| Resonance | Series Resonance* |
| Frequency Tolerance | ±75ppm at 25°C |
| Frequency/Temperature Stability | ±150pm 0 to 70°C |
| Operating Range | 0 to 70°C |
| Shunt Capacitance | 5–7pF |
| Equivalent Series Resistance (ESR) | 50 to 80Ω Max |
| Correlation Drive Level | 100μW |
| Aging | 5ppm/Yr (First 3 Years) |

* See accompanying text for series versus parallel resonant discussion.

The MPC930 is a clock driver which was designed to generate outputs with programmable frequency relationships and not a synthesizer with a fixed input frequency. As a result the crystal input frequency is a function of the desired output frequency. For a design which utilizes the external feedback to the PLL the selection of the crystal frequency is straight forward; simply chose a crystal which is equal in frequency to the fed back signal. To determine the crystal required to produce the desired output frequency for an application which utilizes internal feedback the block diagram of Figure 15 should be used. The P and the M values for the MPC930/931 are also included in Figure 15. The M values can be found in the configuration tables included in this applications section.




$$f_{ref} = \frac{f_{VCO}}{m}, \quad f_{VCO} = fQn \cdot N \cdot P$$

$$\therefore f_{ref} = \frac{fQn \cdot N \cdot P}{m}$$

m = 8
P = 1 (Power_Dn=‘0’), 2 (Power_Dn=‘1’)

**Figure 15. PLL Block Diagram**

For the MPC930 clock driver, the following will provide an example of how to determine the crystal frequency required for a given design.

Given:

Qa = 66.6MHz
Qb = 33.3MHz
Qc = 22.2MHz
Power_Dn = '0'

$$f_{ref} = \frac{fQn \cdot N \cdot P}{m}$$

From Table 4

fQc = VCO/6 then N = 6

From Figure 15

m = 8 and P = 1

$$f_{ref} = \frac{22.22 \cdot 6 \cdot 1}{8} = 16.66MHz$$

**Driving Transmission Lines**

The MPC930/931 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}$/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC930/931 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 16 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC930/931 clock driver is effectively doubled due to its capability to drive multiple lines.

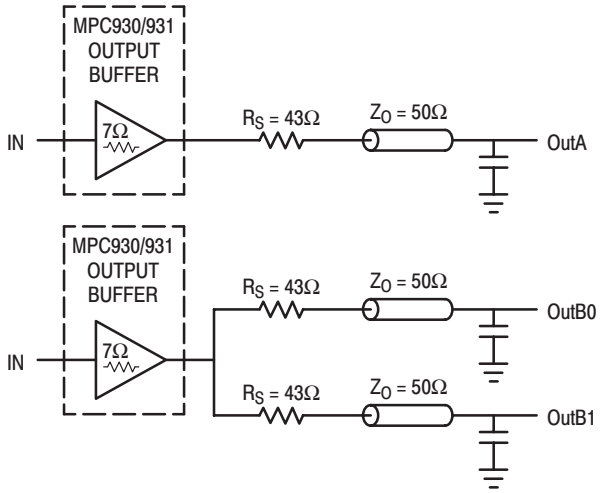



**Figure 16. Single versus Dual Transmission Lines**

The waveform plots of Figure 17 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC930/931 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC930/931. The output waveform in Figure 17 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

VL = VS ( Zo / (Rs + Ro +Zo))

Zo = 50Ω || 50Ω
Rs = 43Ω || 43Ω
Ro = 7Ω

VL = 3.0 (25 / (21.5 + 7 + 25) = 3.0 (25 / 53.5)
= 1.40V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

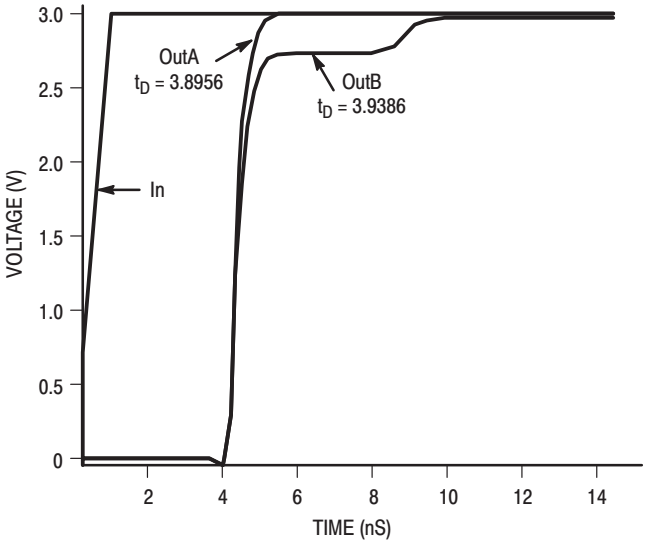
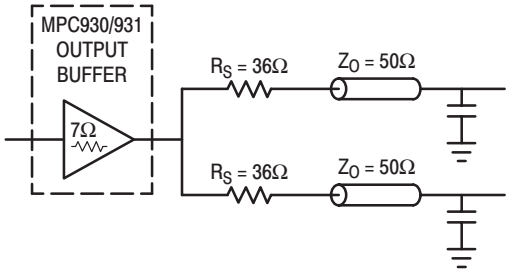



**Figure 17. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 18 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




$7\Omega + 36\Omega \parallel 36\Omega = 50\Omega \parallel 50\Omega$
$25\Omega = 25\Omega$

**Figure 18. Optimized Dual Line Termination**

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

# 2.5V and 3.3V CMOS PLL Clock Generator and Driver

**MPC9315**

**LOW VOLTAGE 2.5V AND 3.3V PLL CLOCK GENERATOR**



The MPC9315 is a 2.5V and 3.3V compatible, PLL based clock generator designed for low-skew clock distribution in low-voltage mid-range to high-performance telecom, networking and computing applications. The MPC9315 offers 8 low-skew outputs and 2 selectable inputs for clock redundancy. The outputs are configurable and support 1:1, 2:1, 4:1, 1:2 and 1:4 output to input frequency ratios. In addition, a selectable output 180° phase control supports advanced clocking schemes with inverted clock signals. The MPC9315 is specified for the extended temperature range of –40 to +85°C.

**Features**

- Configurable 8 outputs LVCMOS PLL clock generator
- Compatible to various microprocessor such as PowerQuicc I and II
- Wide range output clock frequency of 18.75 to 160 MHz
- 2.5V and 3.3V CMOS compatible
- Designed for mid-range to high-performance telecom, networking and computer applications
- Fully integrated PLL supports spread spectrum clocking
- Supports applications requiring clock redundancy
- Max. output skew of 120 ps (80 ps within one bank)
- Selectable output configurations (1:1, 2:1, 4:1, 1:2, 1:4 frequency ratios)
- 2 selectable LVCMOS clock inputs
- External PLL feedback path and selectable feedback configuration
- Tristable outputs
- 32 ld LQFP package
- Ambient operating temperature range of –40 to +85°C

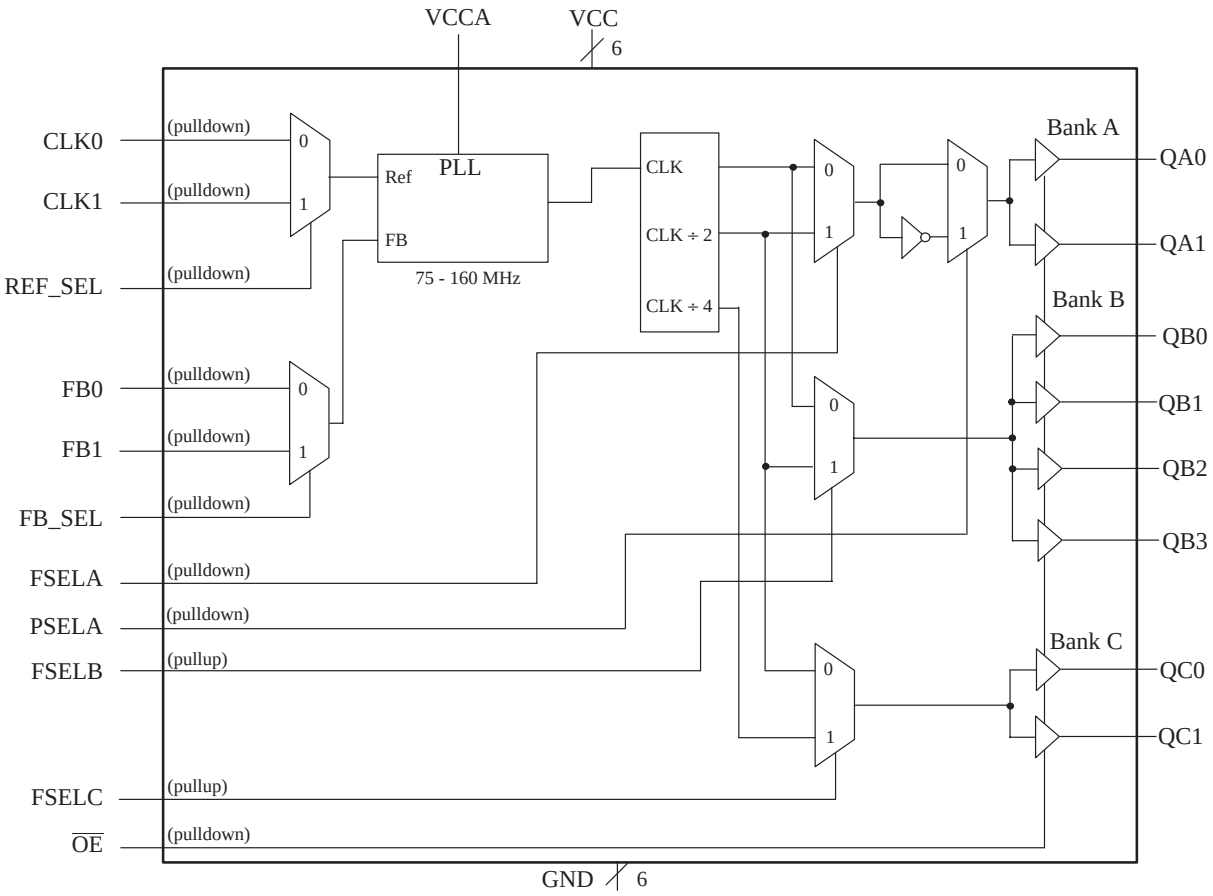
**FA SUFFIX**
LQFP PACKAGE
CASE 873A–02

**Functional Description**

The MPC9315 utilizes PLL technology to frequency and phase lock its outputs onto an input reference clock. Normal operation requires a connection of one of the device outputs to the selected feedback (FB0 or FB1) input to close the PLL feedback path. The reference clock frequency and the output divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. With available output dividers of divide-by-1, divide-by-2 and divide-by-4 the internal VCO of the MPC9315 is running at either 1x, 2x or 4x of the reference clock frequency. The frequency of the QA, QB, QC output groups is either the equal, one half or one fourth of the selected VCO frequency and can be configured for each output bank using the FSELA, FSELB and FSELC pins, respectively. The available output to input frequency ratios are 4:1, 2:1, 1:1, 1:2 and 1:4. The REF_SEL pin selects one of the two available LVCMOS compatible reference input (CLK0 and CLK1) supporting clock redundant applications. The selectable feedback input pin allows the user to select different feedback configurations and input to output frequency ratios. The MPC9315 also provides a static test mode when the PLL supply pin ($V_{CCA}$) is pulled to logic low state (GND). In test mode, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The test mode is intended for system diagnostics, test and debug purpose. This test mode is fully static and the minimum clock frequency specification does not apply. The outputs can be disabled by deasserting the $\overline{OE}$ pin (logic high state). In PLL mode, deasserting $\overline{OE}$ causes the PLL to lose lock due to no feedback signal presence at FB0 or FB1. Asserting $\overline{OE}$ will enable the outputs and close the phase locked loop, also enabling the PLL to recover to normal operation. The MPC9315 is fully 2.5V and 3.3V compatible and requires no external loop filter components. All inputs accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9315 outputs can drive one or two traces giving the devices an effective fanout of 1:18. The device is packaged in a 7x7 $mm^2$ 32-lead LQFP package.

The fully integrated PLL of the MPC9315 allows the low skew outputs to lock onto a clock input and distribute it with essentially zero propagation delay to multiple components on the board. In zero-delay buffer mode, the PLL minimizes phase offset between the outputs and the reference signal.

**Rev 1**




The MPC9315 requires an external RC filter for the analog power supply pin VCCA. Please see application section for details.

**Figure 1. MPC9315 Logic Diagram**

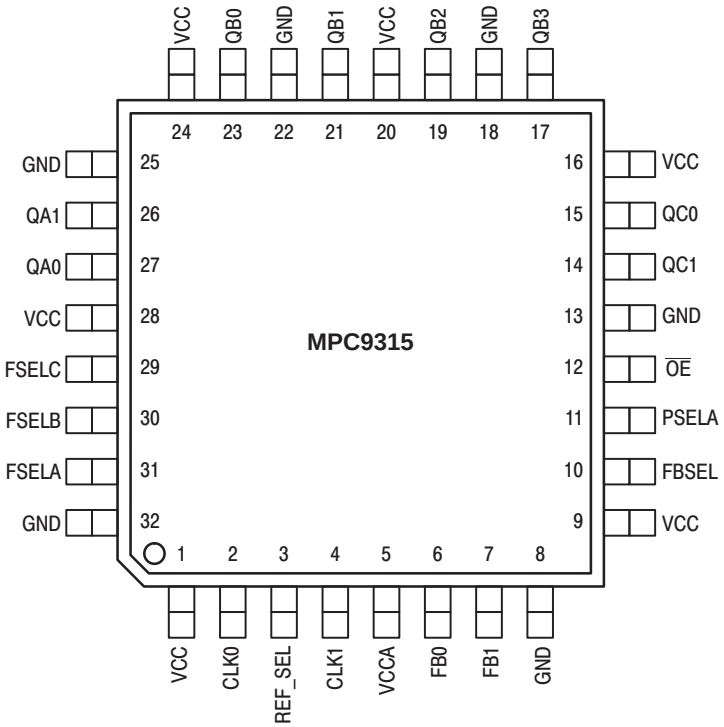



**Figure 2. Pinout: 32–Lead Package Pinout** (Top View)

### PIN CONFIGURATION

| Pin | I/O | Type | Function |
|---|---|---|---|
| CLK0 | Input | LVCMOS | Reference clock input |
| CLK1 | Input | LVCMOS | Alternative clock input |
| FB0 | Input | LVCMOS | PLL feedback input |
| FB1 | Input | LVCMOS | Alternative feedback input |
| REF_SEL | Input | LVCMOS | Selects clock input reference clock input, default low (pull-down) |
| FB_SEL | Input | LVCMOS | Selects PLL feedback clock input, default low (pull-down) |
| FSELA | Input | LVCMOS | Selects divider ratio of bank A outputs, default low (pull-down) |
| FSELB | Input | LVCMOS | Selects divider ratio of bank B outputs, default low (pull-up) |
| FSELC | Input | LVCMOS | Selects divider ratio of bank C outputs, default low (pull-up) |
| PSELA | Input | LVCMOS | Selects phase of bank A outputs |
| QA0, QA1 | Output | LVCMOS | Bank A outputs |
| QB0 to QB3 | Output | LVCMOS | Bank B outputs |
| QC0, QC1 | Output | LVCMOS | Bank C outputs |
| $\overline{OE}$ | Input | LVCMOS | Output tristate |
| VCCA | | Supply | Analog (PLL) positive supply voltage. Requires external RC filter |
| VCC | | Supply | Digital positive supply voltage |
| GND | | Ground | Digital negative supply voltage (ground) |

### FUNCTION TABLE

| Control | Default | 0 | 1 |
|---|---|---|---|
| REF_SEL | 0 | CLK0 | CLK1 |
| FB_SEL | 0 | FB0 | FB1 |
| FSELA | 0 | QAx = VCO clock frequency | QA0, QA1 = VCO clock frequency ÷ 2 |
| FSELB | 1 | QBx = VCO clock frequency | QB0 - QB3 = VCO clock frequency ÷ 2 |
| FSELC | 1 | QCx = VCO clock frequency ÷ 2 | QC0, QC1 = VCO clock frequency ÷ 4 |
| PSELA | 0 | 0° (QA0, QA1 non-inverted) | 180° (QA0, QA1 inverted) |
| VCCA | none | VCCA = GND, PLL off and bypassed for static test and diagnosis | VCCA = 3.3 or 2.5V, PLL enabled |
| MR | 0 | Normal operation | Reset (VCO clamped to min. range) |
| $\overline{OE}$ | 0 | Outputs enabled | Outputs disabled (tristate), open PLL loop |

### ABSOLUTE MAXIMUM RATINGS[a]

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 4.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -55 | 125 | °C | |

a. Absolute maximum continuos ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

### GENERAL SPECIFICATIONS

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output Termination Voltage | | $V_{CC}$ ÷ 2 | | V | |
| MM | ESD (Machine Model) | 200 | | | V | |
| HBM | ESD (Human Body Model) | 2000 | | | V | |
| LU | Latch–Up | 200 | | | mA | |
| $C_{PD}$ | Power Dissipation Capacitance | | 10 | | pF | Per output |
| $C_{IN}$ | | | 4.0 | | pF | Inputs |

**DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40° to 85°C)

| Sym-bol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | | | 0.8 | V | LVCMOS |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$=-24 mA[a] |
| $V_{OL}$ | Output Low Voltage | | | 0.55<br>0.30 | V<br>V | $I_{OL}$= 24mA[a]<br>$I_{OL}$= 12mA |
| $Z_{OUT}$ | Output Impedance | | 14 - 17 | | Ω | |
| $I_{IN}$ | Input Current[b] | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CCA}$ | Maximum PLL Supply Current | | 3.5 | 7.0 | mA | $V_{CCA}$ Pin |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a. The MPC9315 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.
b. Inputs have pull–up or pull–down resistors affecting the input current.

**AC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40° to 85°C)[a]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency | ÷1 feedback<br>÷2 feedback<br>÷4 feedback<br><br>PLL bypass mode | 100[c]<br>37.50<br>18.75<br><br>0 | | 160<br>80<br>40<br><br>TBD | MHz<br>MHz<br>MHz<br><br>MHz | PLL locked<br>PLL locked<br>PLL locked<br><br>$V_{CCA}$ = GND |
| $f_{VCO}$ | VCO Lock Range | | 75[c] | | 160 | MHz | |
| $f_{MAX}$ | Maximum Output Frequency | ÷1 output<br>÷2 output<br>÷4 output | 75<br>37.50<br>18.75 | | 160<br>80<br>40 | MHz<br>MHz<br>MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 25 | | 75 | % | |
| $t_r$, $t_f$ | CLK0, CLK1 Input Rise/Fall Time | | | | 1.0 | ns | 0.8 to 2.0V |
| $t_{(∅)}$ | Propagation Delay (Static Phase Offset) | CLK0 or CLK1 to FB | –150 | | +150 | ps | PLL locked |
| $t_{SK(∅)}$ | Output-to-Output Skew | Within one bank<br>Any output | | | 80<br>120 | ps<br>ps | |
| DC | Output Duty Cycle | | 45 | 50 | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.55 to 2.4V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 10 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 10 | ns | |
| BW | PLL closed loop bandwidth | ÷1 feedback<br>÷2 feedback<br>÷4 feedback | | TBD<br>2.0 – 20<br>0.6 – 6.0 | | MHz<br>MHz<br>MHz | |
| $t_{JIT(CC)}$ | Cycle-to-Cycle Jitter | (1σ) | | 10 | 22 | ps | RMS value |
| $t_{JIT(PER)}$ | Period Jitter | (1σ) | | 8.0 | 15 | ps | RMS value |
| $t_{JIT(∅)}$ | I/O Phase Jitter | (1σ) | | 8.0 – 25[b] | TBD | ps | RMS value |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | | 1.0 | ms | |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
b. I/O jitter depends on VCO frequency. Please see application section for I/O jitter versus VCO frequency characteristics.
c. The VCO range in ÷1 feedback configuration (e.g. QAx connected to FBx and FSELA = 0) is limited to 100 ≤ $f_{VCO}$ ≤ 160 MHz. Please see next revision of the MPC9315 for improved VCO frequency range.

**DC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40° to 85°C)

| Sym-bol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | | | 0.7 | V | LVCMOS |
| $V_{OH}$ | Output High Voltage | 1.8 | | | V | $I_{OH}$=-15 mA[a] |
| $V_{OL}$ | Output Low Voltage | | | 0.6 | V | $I_{OL}$= 15 mA |
| $Z_{OUT}$ | Output Impedance | | 17 - 20 | | Ω | |
| $I_{IN}$ | Input Current[b] | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CCA}$ | Maximum PLL Supply Current | | 2.0 | 5.0 | mA | $V_{CCA}$ Pin |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a. The MPC9315 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.
b. Inputs have pull–up or pull–down resistors affecting the input current.

**AC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40° to 85°C)[a]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency | ÷1 feedback | 110[c] | | 160[c] | MHz | PLL locked |
| | | ÷2 feedback | 37.50 | | 80 | MHz | PLL locked |
| | | ÷4 feedback | 18.75 | | 40 | MHz | PLL locked |
| | | PLL bypass mode | 0 | | TBD | MHz | $V_{CCA}$ = GND |
| $f_{VCO}$ | VCO Lock Range | | 75[c] | | 160[c] | MHz | |
| $f_{MAX}$ | Maximum Output Frequency | ÷1 output | 75 | | 160[c] | MHz | |
| | | ÷2 output | 37.50 | | 80 | MHz | |
| | | ÷4 output | 18.75 | | 50 | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 25 | | 75 | % | |
| $t_r$, $t_f$ | CLK0, CLK1 Input Rise/Fall Time | | | | 1.0 | ns | 0.7 to 1.7V |
| $t_{(\varnothing)}$ | Propagation Delay (Static Phase Offset) | CLK0 or CLK1 to FB | –150 | | +150 | ps | PLL locked |
| $t_{SK(\varnothing)}$ | Output-to-Output Skew | Within one bank | | | 80 | ps | |
| | | Any output | | | 120 | ps | |
| DC | Output Duty Cycle | | 45 | 50 | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.55 to 2.4V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 12 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 12 | ns | |
| BW | PLL closed loop bandwidth | ÷1 feedback | | 2.0 – 20 | | MHz | |
| | | ÷2 feedback | | 1.0 – 10 | | MHz | |
| | | ÷4 feedback | | 0.4 – 3.0 | | MHz | |
| $t_{JIT(CC)}$ | Cycle-to-Cycle Jitter | (1σ) | | 10 | 22 | ps | RMS value |
| $t_{JIT(PER)}$ | Period Jitter | (1σ) | | 8.0 | 15 | ps | RMS value |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | (1σ) | | 10 – 25[b] | TBD | ps | RMS value |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | | 1.0 | ms | |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
b. I/O jitter depends on VCO frequency. Please see application section for I/O jitter versus VCO frequency characteristics.
c. The VCO range in ÷1 feedback configuration (e.g. QAx connected to FBx and FSELA = 0) is limited to 110 ≤ $f_{VCO}$ ≤ 160 MHz. Please see next revision of the MPC9315 for improved VCO frequency range.

## APPLICATIONS INFORMATION

### Programming the MPC9315

The PLL of the MPC9315 supports output clock frequencies from 18.75 to 160 MHz. Different feedback and output divider configurations can be used to achieve the desired input to output frequency relationship. The feedback frequency and divider should be used to situate the VCO in the frequency range between 75 and 160 MHz for stable and optimal operation. The FSELA, FSELB, FSELC pins select the desired output clock frequencies. Possible frequency ratios of the reference clock input to the outputs are 1:1, 1:2, 1:4 as well as 2:1 and 4:1, Table 1, Table 2 and Table 3 illustrate the various output configurations and frequency ratios supported by the MPC9315. PSELA controls the output phase of the QA0 and QA1 outputs, allowing the user to generate inverted clock signals synchronous to non-inverted clock signals. See also “Example Configurations for the MPC9315” on page 8 for further reference.



**Table 1: Output Frequency Relationship for QA0 connected to FB0[a]**

| Inputs | | | Outputs | | |
|---|---|---|---|---|---|
| FSELA | FSELB | FSELC | QA0, QA1 | QB0-QB3 | QC0, QC1 |
| 0 | 0 | 0 | CLK | CLK | CLK ÷ 2 |
| 0 | 0 | 1 | CLK | CLK | CLK ÷ 4 |
| 0 | 1 | 0 | CLK | CLK ÷ 2 | CLK ÷ 2 |
| 0 | 1 | 1 | CLK | CLK ÷ 2 | CLK ÷ 4 |
| 1 | 0 | 0 | CLK | 2 * CLK | CLK |
| 1 | 0 | 1 | CLK | 2 * CLK | CLK ÷ 2 |
| 1 | 1 | 0 | CLK | CLK | CLK |
| 1 | 1 | 1 | CLK | CLK | CLK ÷ 2 |

a. Output frequency relationship with respect to input reference frequency CLK.

**Table 2: Output Frequency Relationship for QB0 connected to FB0[a]**

| Inputs | | | Outputs | | |
|---|---|---|---|---|---|
| FSELA | FSELB | FSELC | QA0, QA1 | QB0-QB3 | QC0, QC1 |
| 0 | 0 | 0 | CLK | CLK | CLK ÷ 2 |
| 0 | 0 | 1 | CLK | CLK | CLK ÷ 4 |
| 0 | 1 | 0 | 2 * CLK | CLK | CLK |
| 0 | 1 | 1 | 2 * CLK | CLK | CLK ÷ 2 |
| 1 | 0 | 0 | CLK ÷ 2 | CLK | CLK ÷ 2 |
| 1 | 0 | 1 | CLK ÷ 2 | CLK | CLK ÷ 4 |
| 1 | 1 | 0 | CLK | CLK | CLK |
| 1 | 1 | 1 | CLK | CLK | CLK ÷ 2 |

a. Output frequency relationship with respect to input reference frequency CLK.

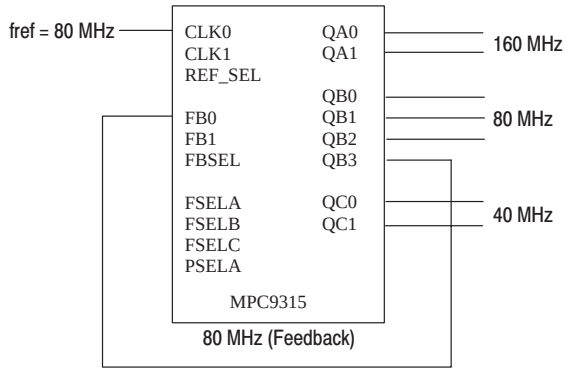
**Table 3: Output Frequency Relationship for QC0 connected to FB0[a]**

| Inputs | | | Outputs | | |
|---|---|---|---|---|---|
| FSELA | FSELB | FSELC | QA0, QA1 | QB0-QB3 | QC0, QC1 |
| 0 | 0 | 0 | 2 * CLK | 2 * CLK | CLK |
| 0 | 0 | 1 | 4 * CLK | 4 * CLK | CLK |
| 0 | 1 | 0 | 2 * CLK | CLK | CLK |
| 0 | 1 | 1 | 4 * CLK | 2 * CLK | CLK |
| 1 | 0 | 0 | CLK | 2 * CLK | CLK |
| 1 | 0 | 1 | 2 * CLK | 4 * CLK | CLK |
| 1 | 1 | 0 | CLK | CLK | CLK |
| 1 | 1 | 1 | 2 * CLK | 2 * CLK | CLK |

a. Output frequency relationship with respect to input reference frequency CLK.

## Example Configurations for the MPC9315

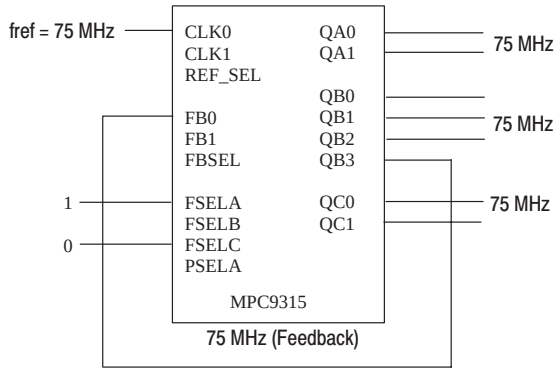
### Figure 3. MPC9315 Default Configuration




MPC9315 default configuration (feedback of QB3 = 100 MHz). All control pins are left open.

| Frequency range | Min | Max |
|---|---|---|
| Input | 37.50 MHz | 80 MHz |
| QA outputs | 75.00 MHz | 160 MHz |
| QB outputs | 37.50 MHz | 80 MHz |
| QC outputs | 18.75 MHz | 40 MHz |

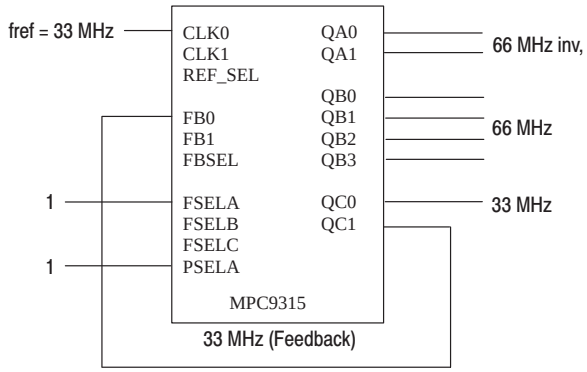
### Figure 4. MPC9315 Zero Delay Buffer Configuration




MPC9315 1:1 frequency configuration (feedback of QB3 = 75 MHz). FSELA = H, FSELC = L. All other control pins are left open.

| Frequency range | Min | Max |
|---|---|---|
| Input | 37.50 MHz | 80 MHz |
| QA outputs | 37.50 MHz | 80 MHz |
| QB outputs | 37.50 MHz | 80 MHz |
| QC outputs | 37.50 MHz | 80 MHz |

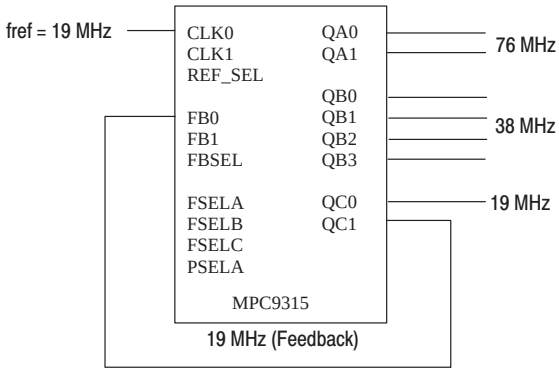
### Figure 5. MPC9315 180° Phase Inversion Configuration




MPC9315 1:1 frequency configuration (feedback of QC1 = 33 MHz). FSELA = PSELA = H. All other control pins are left open.

| Frequency range | Min | Max |
|---|---|---|
| Input | 18.75 MHz | 40 MHz |
| QA outputs | 37.50 MHz | 80 MHz |
| QB outputs | 37.50 MHz | 80 MHz |
| QC outputs | 18.75 MHz | 40 MHz |

### Figure 6. MPC9315 x4 Multiplier Configuration




MPC9315 4x, 2x, 1x frequency configuration (feedback of QC1 = 19 MHz). All control pins are left open.

| Frequency range | Min | Max |
|---|---|---|
| Input | 18.75 MHz | 40 MHz |
| QA outputs | 75.00 MHz | 160 MHz |
| QB outputs | 37.50 MHz | 80 MHz |
| QC outputs | 18.75 MHz | 40 MHz |

2

### Using the MPC9315 in zero–delay applications

The external feedback option of the MPC9315 PLL allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge and virtually eliminates the propagation delay through the device.

The remaining insertion delay (skew error) of the MPC9315 in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset (SPO or $t_{(\varnothing)}$), I/O jitter ($t_{JIT(\varnothing)}$, phase or long-term jitter), feedback path delay and the output-to-output skew ($t_{SK(O)}$ relative to the feedback output.

### Calculation of part-to-part skew

The MPC9315 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs (TCLK or PCLK) of two or more MPC9315 are connected together, the maximum overall timing uncertainty from the common TCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consists of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

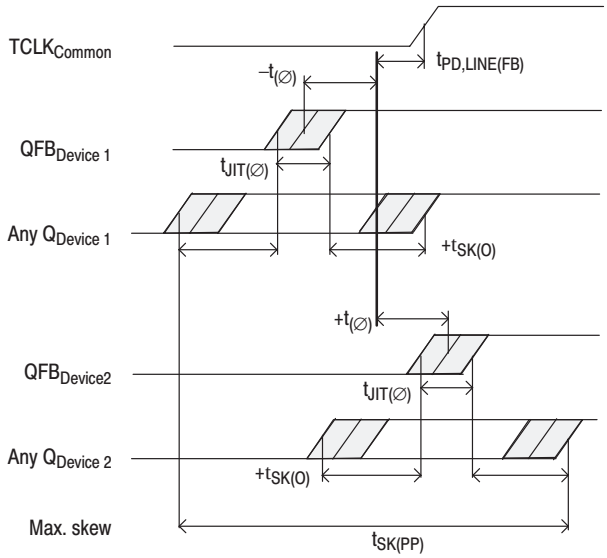



**Figure 7. MPC9315 max. device-to-device skew**

Due to the statistical nature of I/O jitter, a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

**Table 8: Confidence Facter CF**

| CF | Probability of clock edge within the distribution |
|---|---|
| ± 1σ | 0.68268948 |
| ± 2σ | 0.95449988 |
| ± 3σ | 0.99730007 |
| ± 4σ | 0.99993663 |
| ± 5σ | 0.99999943 |
| ± 6σ | 0.99999999 |

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of -300 ps to +300 ps relative to TCLK ($V_{CC}$=3.3V and $f_{VCO}$ = 160 MHz):

$$t_{SK(PP)} = [–150ps...150ps] + [–150ps...150ps] + [(10ps \cdot –3)...(10ps \cdot 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [–300ps...300ps] + t_{PD,\ LINE(FB)}$$

Above equation uses the maximum I/O jitter number shown in the AC characteristic table for $V_{CC}$=3.3V (10 ps RMS). I/O jitter is frequency dependant with a maximum at the lowest VCO frequency (160 MHz for the MPC9315). Applications using a higher VCO frequency exhibit less I/O jitter than the AC characteristic limit. The I/O jitter characteristics in Figure 8 and Figure 9 can be used to derive a smaller I/O jitter number at the specific VCO frequency, resulting in tighter timing limits in zero-delay mode and for part-to-part skew $t_{SK(PP)}$.

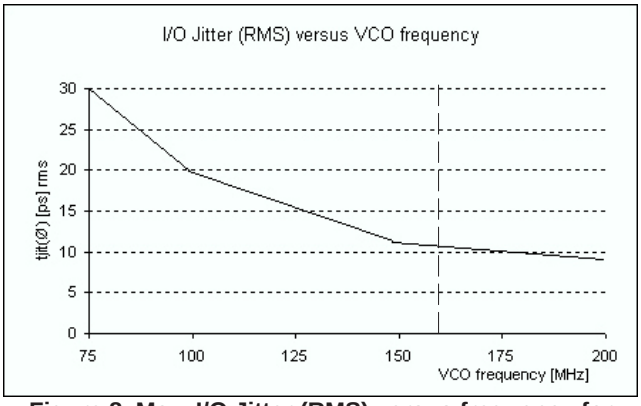



**Figure 8. Max. I/O Jitter (RMS) versus frequency for $V_{CC}$=2.5V**

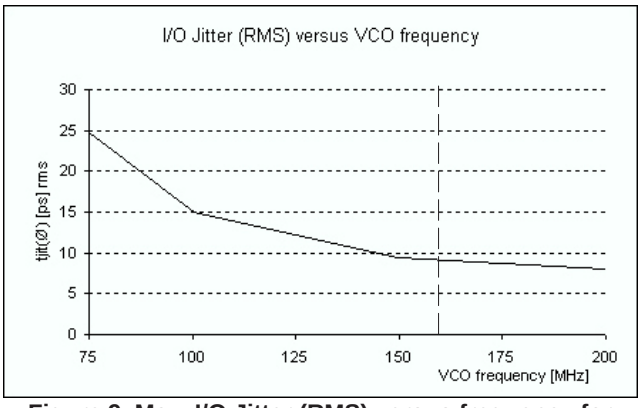



**Figure 9. Max. I/O Jitter (RMS) versus frequency for $V_{CC}$=3.3V**

### Power Supply Filtering

The MPC9315 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Noise on the $V_{CCA}$ (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC9315 provides separate power supplies for the output buffers ($V_{CC}$) and the phase-locked loop ($V_{CCA}$) of the device.The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize

noise on the power supplies, a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the $V_{CCA}$ pin for the MPC9315. Figure 10 illustrates a typical power supply filter scheme. The MPC9315 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor $R_F$. From the data sheet the $I_{CCA}$ current (the current sourced through the $V_{CCA}$ pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V ($V_{CC}$=3.3V or $V_{CC}$=2.5V) must be maintained on the $V_{CCA}$ pin. The resistor $R_F$ shown in Figure 10 "$V_{CCA}$ Power Supply Filter" must have a resistance of 270Ω ($V_{CC}$=3.3V) or 9-10Ω ($V_{CC}$=2.5V) to meet the voltage drop criteria.

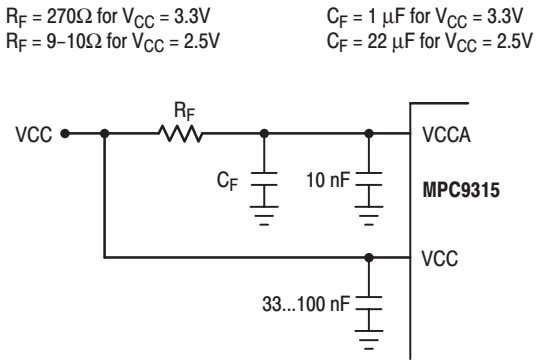



**Figure 10. $V_{CCA}$ Power Supply Filter**

The minimum values for $R_F$ and the filter capacitor $C_F$ are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 10 "$V_{CCA}$ Power Supply Filter", the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9315 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Driving Transmission Lines**

The MPC9315 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}$÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9315 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 11 "Single versus Dual Transmission Lines" illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9315 clock driver is effectively doubled due to its capability to drive multiple lines.

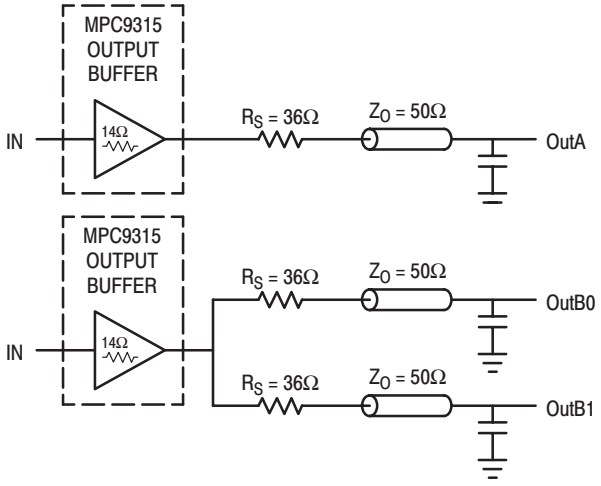



**Figure 11. Single versus Dual Transmission Lines**

The waveform plots in Figure 12 "Single versus Dual Line Termination Waveforms" show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9315 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9315. The output waveform in Figure 12 "Single versus Dual Line Termination Waveforms" shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S ( Z_0 \div (R_S+R_0+Z_0))$$
$$Z_0 = 50\Omega \parallel 50\Omega$$
$$R_S = 36\Omega \parallel 36\Omega$$
$$R_0 = 14\Omega$$
$$V_L = 3.0 ( 25 \div (18+17+25)$$
$$= 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

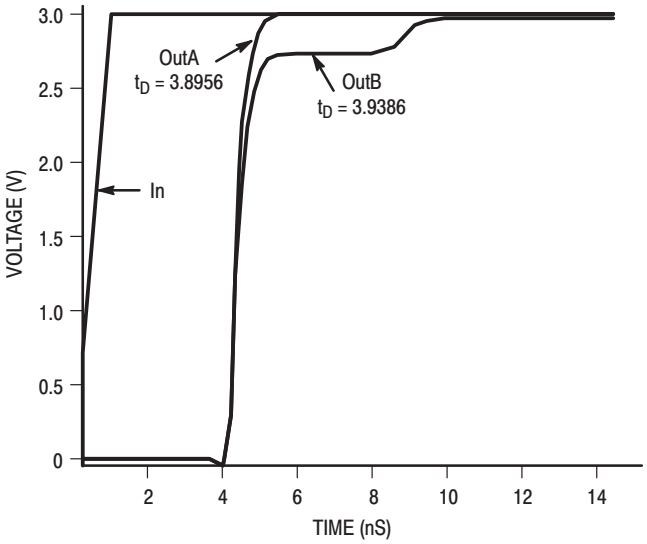
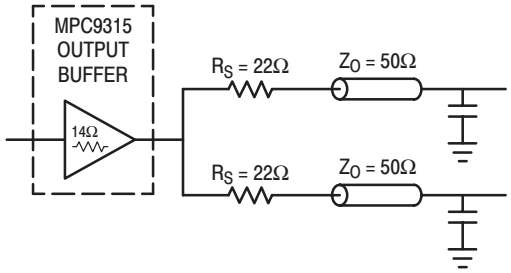



**Figure 12. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 13 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




$14\Omega + 22\Omega \parallel 22\Omega = 50\Omega \parallel 50\Omega$
$25\Omega = 25\Omega$

**Figure 13. Optimized Dual Line Termination**

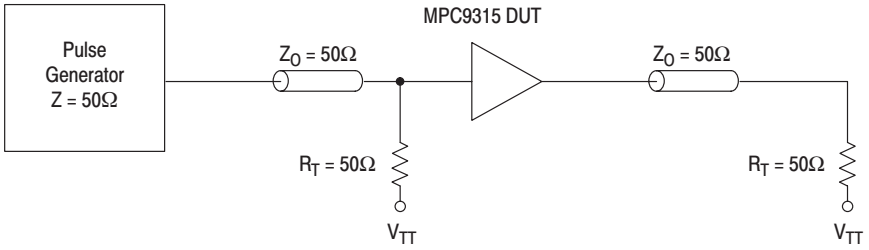



**Figure 14. CLK0, CLK1 MPC9315 AC test reference**

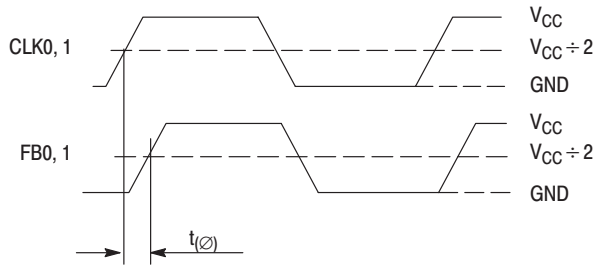
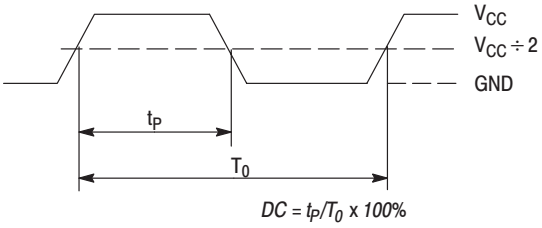


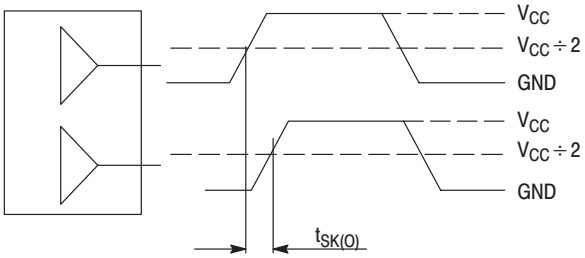

**Figure 15. Propagation delay ($t_{(\varnothing)}$, SPO) test reference**





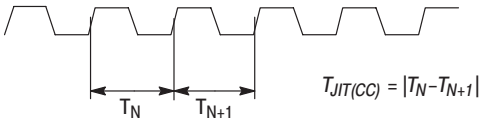

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 16. Output Duty Cycle (DC)**



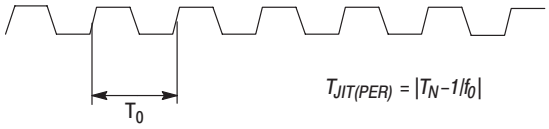

The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 17. Output–to–output Skew $t_{SK(O)}$**



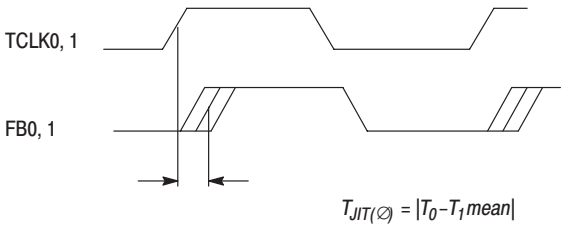

The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

**Figure 18. Cycle–to–cycle Jitter**




The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

**Figure 19. Period Jitter**




The deviation in $t_0$ for a controlled edge with respect to a $t_0$ mean in a random sample of cycles

**Figure 20. I/O Jitter**

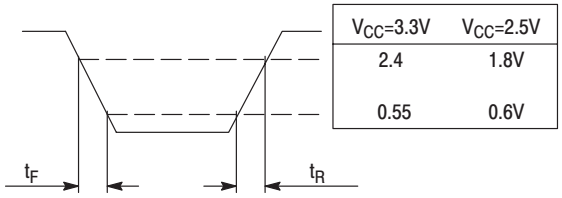



**Figure 21. Output Transition Time Test Reference**

# Low Voltage PLL Clock Driver

**MPC932**

**LOW VOLTAGE PLL CLOCK DRIVER**



**FA SUFFIX**
TQFP PACKAGE
CASE 873A-02

2

The MPC932 is a 3.3 V compatible PLL based clock driver device targetted for zero delay applications. The device provides 6 outputs for driving clock loads plus a single dedicated PLL feedback clock output. The dedicated feedback output gives the user six choices of input multiplication factors: x1, x1.25, x1.5, x2, x2.5 and x3.

- 6 Low Skew Clock Outputs
- 1 Dedicated PLL Feedback Output
- Individual Output Enable Control
- Fully Integrated PLL
- Output Frequency Up to 120MHz
- 32–Lead TQFP Packaging
- 3.3V VCC
- ±100ps Cycle–to–Cycle Jitter

The MPC932 provides individual output enable control. The enables are synchronized to the internal clock such that upon assertion the shut down signals will hold the clocks LOW without generating a runt pulse on the outputs. The shut down pins provide a means of powering down certain portions of a system or a means of disabling outputs when the full compliment is not required for a specific design. The shut down pins will disable the outputs when driven LOW. A common shut down pin is provided to disable all of the outputs (except the feedback output) with a single control signal.

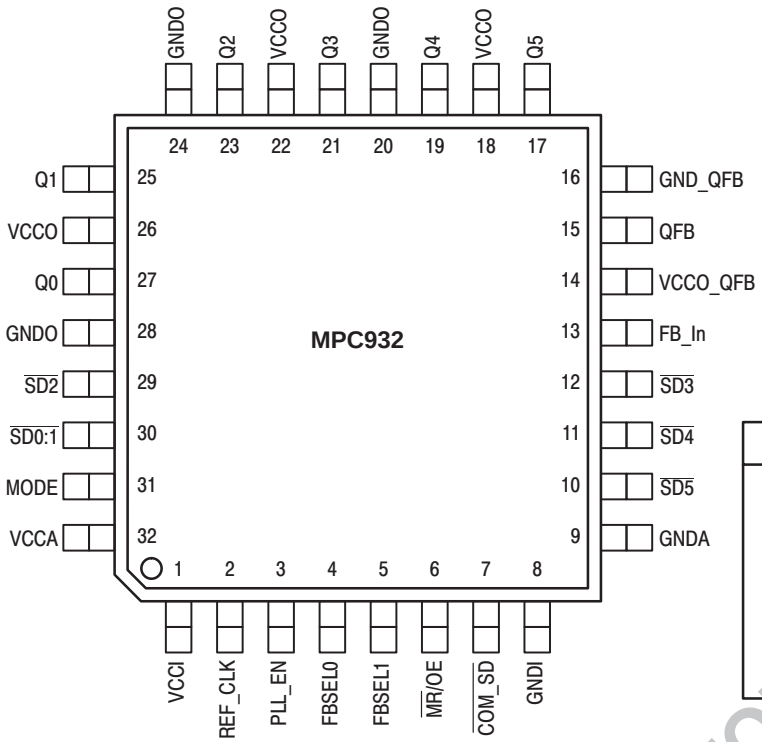
Two feedback select pins are provided to select the multiplication factor of the PLL. The MPC932 provides six multiplication factors: x1, x1.25, x1.5, x2, x2.5 and x3. In the x1.25 and x2.5 modes, the QFB output will not provide a 50% duty cycle. The phase detector of the MPC932 only monitors rising edges of its feedback signals, thus for this function a 50% duty cycle is not required. As the QFB signal can also be used to drive other clocks in a system it is important the user understand that the duty cycle will not be 50%. In the x1 and x1.5 modes the QFB output will produce 50% duty cycle signals.

The MPC932 provides two pins for use in system test and debug operations. The $\overline{MR}$/OE input will force all of the outputs into a high impedance state to allow for back driving the outputs during system test. In addition the PLL_EN pin allows the user to bypass the PLL and drive the outputs directly through the Ref_CLK input. Note the Ref_CLK signal will be routed through the dividers so that it will take several transitions on the Ref_CLK input to create a transition on the outputs.

The MPC932 is fully 3.3 V compatible and requires no external loop filter components. All of the inputs are LVCMOS/LVTTL compatible and the outputs produce rail–to–rail 3.3V swings. For series terminated applications each output can drive two series terminated 50 Ω transmission lines. For parallel terminated lines the device can drive terminations of 50 Ω into VCC/2. The device is packaged in a 32–lead TQFP package to provide the optimum combination of performance, board density and cost.

**Rev 1**

**Pinout: 32-Lead TQFP Package** (Top View)




**FUNCTION TABLES**

| $\overline{SDn}$, $\overline{COM\_SD}$ | Qn |
|---|---|
| 0 | Held LOW |
| 1 | Enabled |

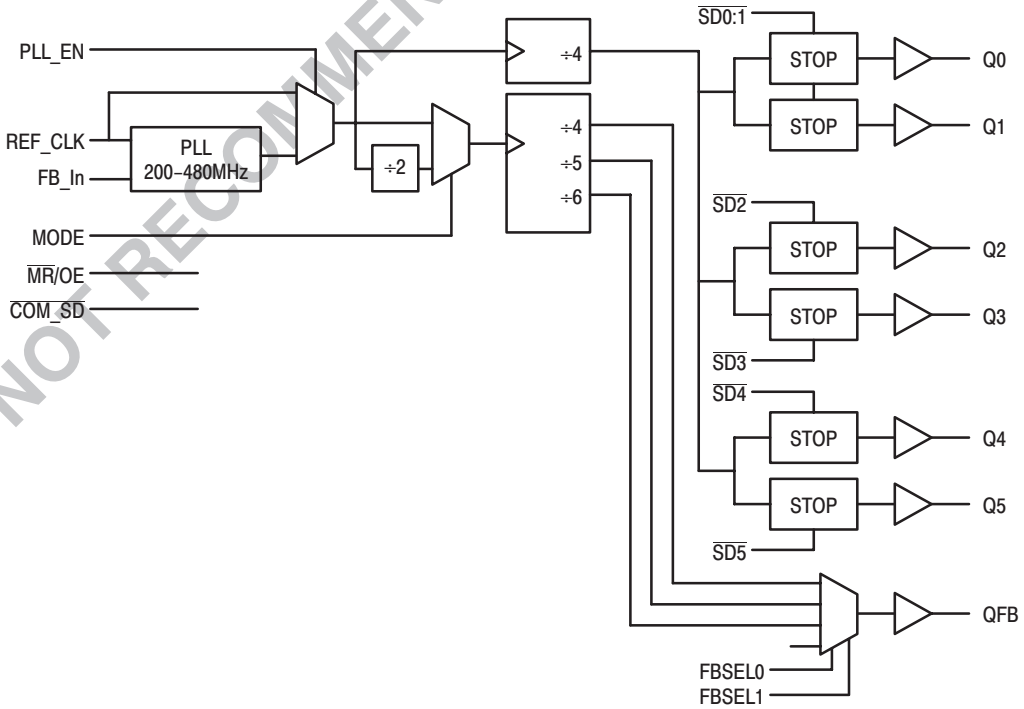
| PLL_En | PLL Status |
|---|---|
| 0 | Test Mode |
| 1 | PLL Enabled |

| $\overline{MR}$/OE | PLL Status |
|---|---|
| 0 | Disabled |
| 1 | Enabled |

| MODE | FBSEL1 | FBSEL0 | Qn | QFB |
|---|---|---|---|---|
| 0 | 0 | 0 | VCO/4 | VCO/8 |
| 0 | 0 | 1 | VCO/4 | VCO/10 |
| 0 | 1 | 0 | VCO/4 | VCO/12 |
| 0 | 1 | 1 | NA | NA |
| 1 | 0 | 0 | VCO/4 | VCO/4 |
| 1 | 0 | 1 | VCO/4 | VCO/5 |
| 1 | 1 | 0 | VCO/4 | VCO/6 |
| 1 | 1 | 1 | NA | NA |



**LOGIC DIAGRAM**



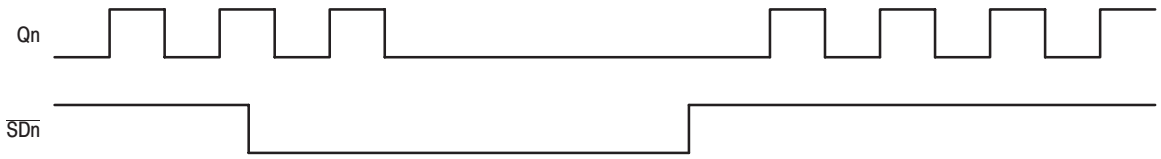



**Figure 1. Timing Diagram**

2

**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 4.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_{IN}$ | Input Current | | ±20 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

**PLL INPUT REFERENCE CHARACTERISTICS** ($T_A$ = 0 to 70°C)

| Symbol | Characteristic | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $t_r$, $t_f$ | TCLK Input Rise/Falls | | 3.0 | ns | |
| $f_{ref}$ | Reference Input Frequency | Note 1. | Note 1. | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | 25 | 75 | % | |

1. Maximum and minimum input reference frequency is limited by the VCO lock range and the feedback divider.

**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | 3.6 | V | |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | $I_{OH}$ = –20mA (Note 2.) |
| $V_{OL}$ | Output LOW Voltage | | | 0.5 | V | $I_{OL}$ = 20mA (Note 2.) |
| $I_{IN}$ | Input Current | | | ±120 | µA | Note 3. |
| $I_{CC}$ | Maximum Core Supply Current | | | 130 | mA | |
| $I_{CCPLL}$ | Maximum PLL Supply Current | | 15 | 20 | mA | |
| $C_{IN}$ | | | | 4 | pF | |
| $C_{pd}$ | | | 25 | | pF | Per Output |

2. The MPC932 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}$/2) transmission lines on the incident edge (see Applications Info section).
3. Inputs have pull–up/pull–down resistors which affect input current.

**MPC932 AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Reference Frequency | Note 6. | | Note 6. | MHz | |
| $t_{os}$ | Output-to-Output Skew | | 250 | 600 | ps | Note 4. |
| $f_{VCO}$ | VCO Lock Range | 200 | | 480 | MHz | |
| $f_{max}$ | Maximum Output Frequency (÷4)<br>(÷5)<br>(÷6) | | | 120<br>96<br>80 | MHz | |
| $t_{pd}$ | Reference to EXT_FB Average Delay TCLK<br>PECL_CLK | –200 | 0 | 200 | ps | $f_{ref}$ = 50MHz; Note 7. |
| $t_{pw}$ | Output Duty Cycle (Note 4.) | $t_{CYCLE}/2$ –750 | $t_{CYCLE}/2$ ±500 | $t_{CYCLE}/2$ +750 | ps | |
| $t_r$, $t_f$ | Output Rise/Fall Time (Note 4.) | 0.1 | | 1.0 | ns | 0.8 to 2.0V |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time | 2.0 | | 8.0 | ns | 50 Ω to $V_{CC}/2$ |
| $t_{PZL}$ | Output Enable Time | 2.0 | | 10 | ns | 50 Ω to $V_{CC}/2$ |
| $t_{jitter}$ | Cycle–to–Cycle Jitter (Peak–to–Peak) | | ±100 | | ps | Note 5. |
| $t_{lock}$ | Maximum PLL Lock Time | | | 10 | ms | |

4. Measured with 50Ω to $V_{CC}/2$ termination.
5. See Applications Info section for more jitter information.
6. Input reference frequency is bounded by VCO lock range and feedback divide selection.
7. $t_{pd}$ measurement uses the averaging feature of the oscilloscope to remove the jitter component.



## APPLICATIONS INFORMATION

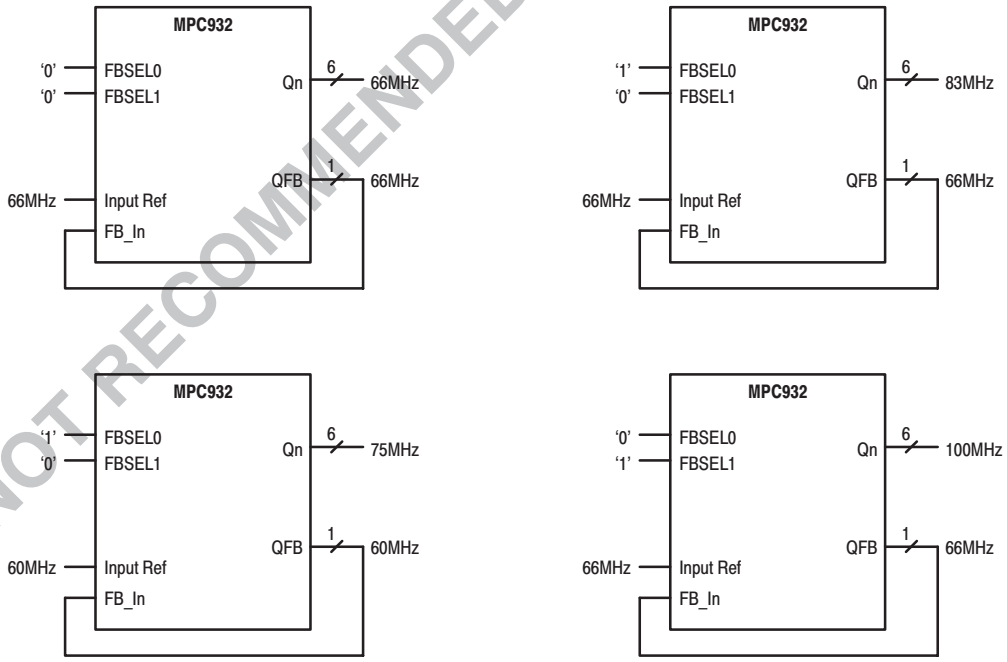



**Figure 2. MPC932 Potential Configurations**
(Mode = 1)

2

**Power Supply Filtering**

The MPC932 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC932 provides separate power supplies for the output buffers ($V_{CCO}$) and the internal PLL (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC932.

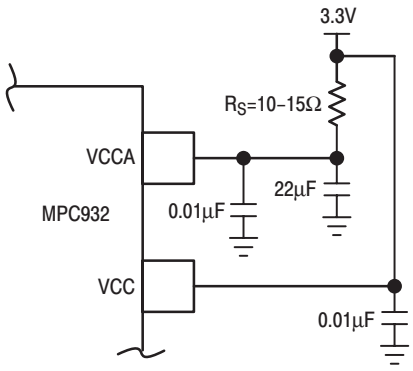



**Figure 3. Power Supply Filter**

Figure 3 illustrates a typical power supply filter scheme. The MPC932 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the VCCA pin of the MPC932. From the data sheet the $I_{VCCA}$ current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V $V_{CC}$ supply is used. The resistor shown in Figure 3 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

Although the MPC932 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Driving Transmission Lines**

The MPC932 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}$/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC932 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC932 clock driver is effectively doubled due to its capability to drive multiple lines.

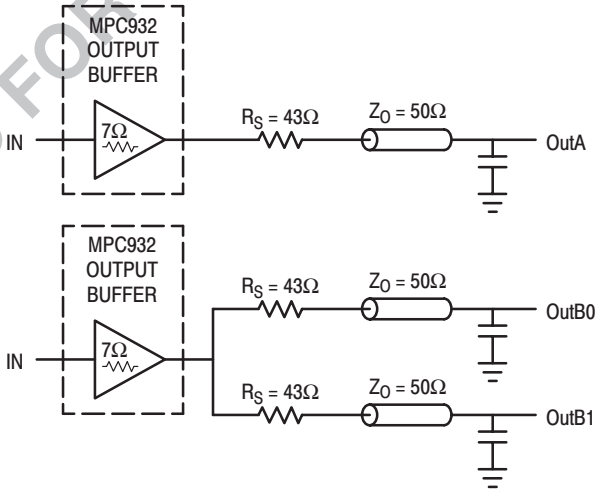



**Figure 4. Single versus Dual Transmission Lines**

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC932 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC932. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS ( Zo / (Rs + Ro + Zo))$$

Zo = 50Ω || 50Ω
Rs = 43Ω || 43Ω

Ro = 7Ω

VL = 3.0 (25 / (21.5 + 7 + 25) = 3.0 (25 / 53.5)
= 1.40V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

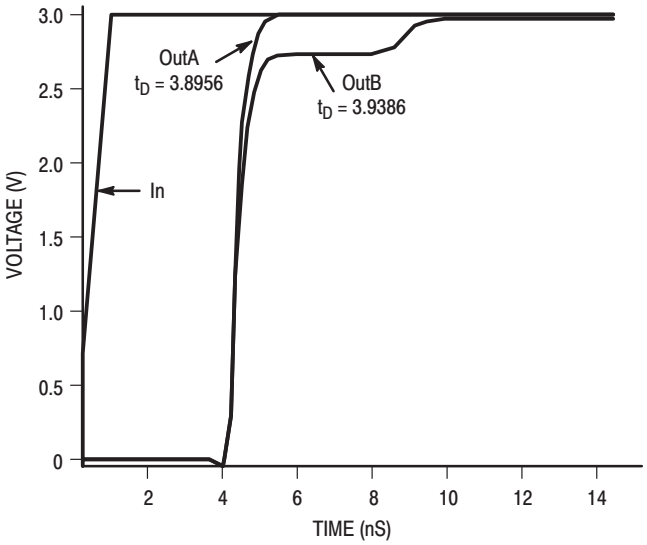
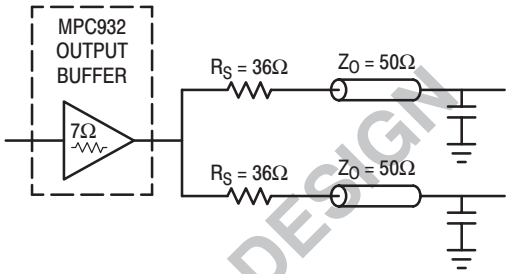



**Figure 5. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




7Ω + 36Ω || 36Ω = 50Ω || 50Ω
25Ω = 25Ω

**Figure 6. Optimized Dual Line Termination**

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

**Order Number: MPC9330/D**
**Rev 0, 11/2001**

2

*Product Preview*

# 3.3V/2.5V 1:6 LVCMOS PLL Clock Generator

**MPC9330**

**3.3V/2.5V 1:6 LVCMOS PLL CLOCK GENERATOR**

**FA SUFFIX**
32 LEAD LQFP PACKAGE
CASE 873A

The MPC9330 is a 3.3V or 2.5V compatible, 1:6 PLL based clock generator targeted for high performance low-skew clock distribution in mid-range to high-performance telecomm, networking and computing applications. With output frequencies up to 200 MHz and output skews less than 150 ps[1] the device meets the needs of the most demanding clock applications. The MPC9330 is specified for the extended temperature range of –40°C to +85°C.

**Features**

- 1:6 PLL based low-voltage clock generator
- 2.5V or 3.3V power supply
- Generates clock signals up to 200 MHz
- Maximum output skew of 150 ps[1]
- On-chip crystal oscillator clock reference
- Alternative LVCMOS PLL reference clock input
- Internal and external PLL feedback
- PLL multiplies the reference clock by 4x, 3x, 2x, 1x, 4/3x, 3/2x, 2/3x, x/2, x/3 or x/4
- Supports zero-delay operation in external feedback mode
- Synchronous output clock stop in logic low eliminates output runt pulses
- Power_down feature reduces output clock frequency
- Drives up to 12 clock lines
- 32 lead LQFP packaging
- Ambient temperature range –40°C to +85°C
- Pin and function compatible to the MPC930

**Functional Description**

The MPC9330 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9330 requires either the selection of internal PLL feedback or the connection of one of the device outputs to the feedback input to close the PLL feedback path in external feedback mode. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. In external PLL feedback configuration and with the available post-PLL dividers (divide-by-2, divide-by-4 and divide-by-6), the internal VCO of the MPC9330 is running at either 4x, 8x, 12x, 16x or 24x of the reference clock frequency. In internal feedback configuration (divide-by-16) the internal VCO is running 16x of the reference frequency. The frequency of the QA, QB, QC output banks is a division of the VCO frequency and can be configured independently for each output bank using the FSELA, FSELB and FSELC pins, respectively. The available output to input frequency ratios are 4x, 3x, 2x, 1x, 4/3x, 3/2x, 2/3x, x/2, x/3 or x/4.

The REF_SEL pin selects the internal crystal oscillator or the LVCMOS compatible input as the reference clock signal. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply.

The outputs can be disabled (high-impedance) by deasserting the OE pin. In the PLL configuration with external feedback selected, deasserting OE causes the PLL to loose lock due to missing feedback signal presence at FB_IN. Asserting OE will enable the outputs and close the phase locked loop, enabling the PLL to recover to normal operation. The MPC9330 output clock stop control allows the outputs to start and stop synchronously in the logic low state, without the potential generation of runt pulses.

The MPC9330 is fully 2.5V and 3.3V compatible and requires no external loop filter components. All inputs (except XTAL) accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9330 outputs can drive one or two traces giving the devices an effective fanout of 1:12. The device is packaged in a 7x7 mm$^2$ 32-lead LQFP package.

1. Design target, pending final characterization.



**Rev 0**

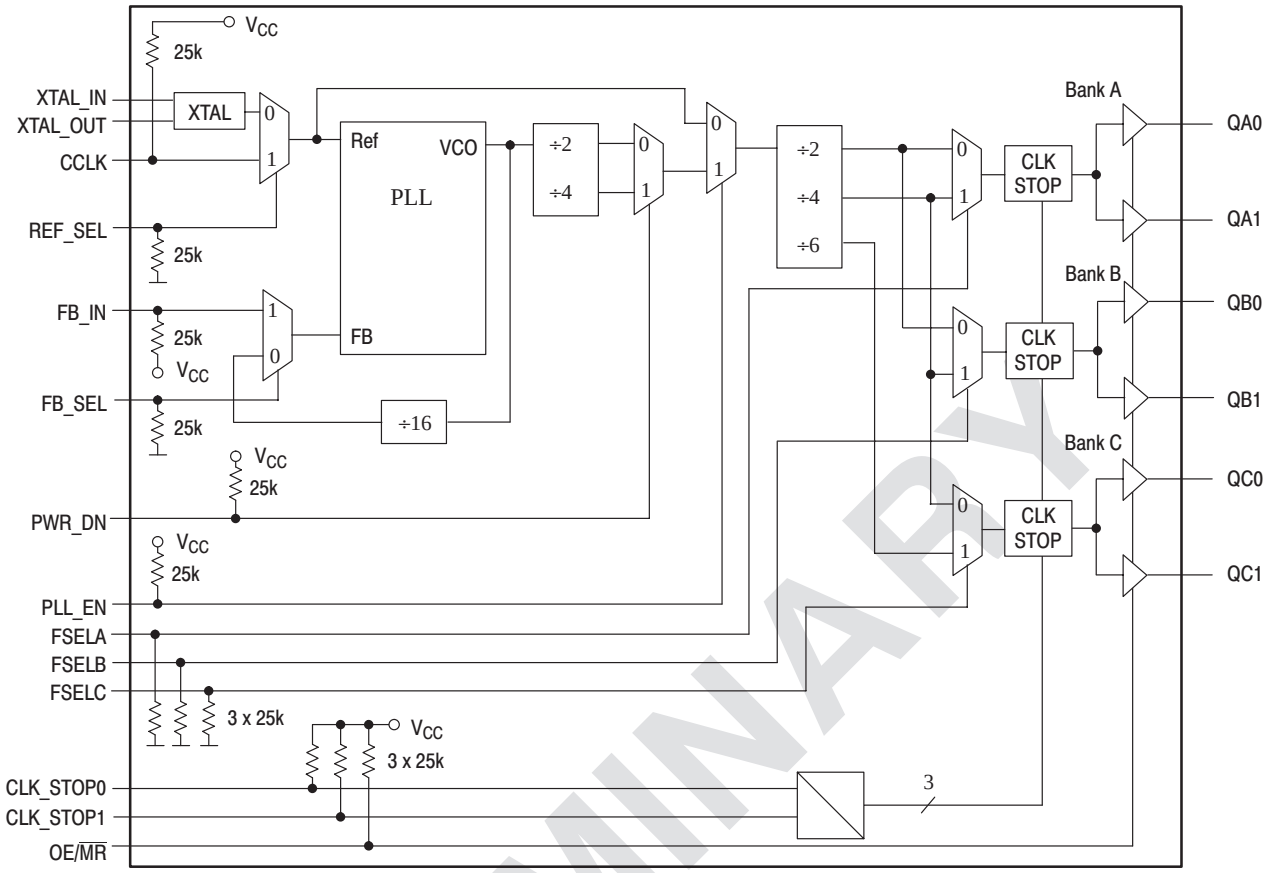
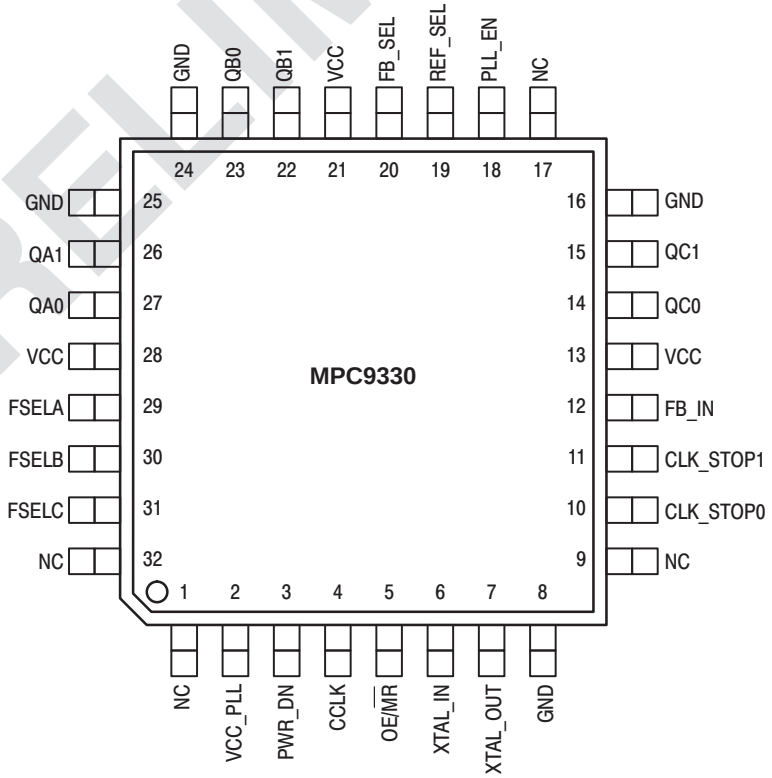



**Figure 1. MPC9330 Logic Diagram**




The MPC9330 requires an external RC filter for the analog power supply pin VCC_PLL. Please see application section for details.

**Figure 2. MPC9330 32–Lead Package Pinout** (Top View)

**Table 1: PIN CONFIGURATION**

| Pin | I/O | Type | Function |
|---|---|---|---|
| CCLK | Input | LVCMOS | PLL reference clock signal |
| XTAL_IN, XTAL_OUT | Input | Analog | Crystal oscillator interface |
| FB_IN | Input | LVCMOS | PLL feedback signal input, connect to an output |
| FB_SEL | Input | LVCMOS | Feedback select |
| REF_SEL | Input | LVCMOS | Reference clock select |
| PWR_DN | Input | LVCMOS | Output frequency and power down select |
| FSELA | Input | LVCMOS | Frequency divider select for bank A outputs |
| FSELB | Input | LVCMOS | Frequency divider select for bank B outputs |
| FSELC | Input | LVCMOS | Frequency divider select for bank C outputs |
| PLL_EN | Input | LVCMOS | PLL enable/disable |
| CLK_STOP0-1 | Input | LVCMOS | Clock output enable/disable |
| OE/$\overline{MR}$ | Input | LVCMOS | Output enable/disable (high-impedance tristate) and device reset |
| QA0-1, QB0-1, QC0-1 | Output | LVCMOS | Clock outputs |
| GND | Supply | Ground | Negative power supply |
| VCC_PLL | Supply | VCC | PLL positive power supply (analog power supply). The MPC9330 requires an external RC filter for the analog power supply pin $V_{CC\_PLL}$. Please see applications section for details. |
| VCC | Supply | VCC | Positive power supply for I/O and core. All VCC pins must be connected to the positive power supply for correct operation |

**Table 2: FUNCTION TABLE**

| Control | Default | 0 | 1 |
|---|---|---|---|
| REF_SEL | 0 | The crystal oscillator output is the PLL reference clock | CCLK is the PLL reference clock |
| FB_SEL | 0 | Internal PLL feedback of 16. $f_{VCO} = 16 * f_{ref}$ | External feedback. Zero-delay operation enabled for CCLK as reference clock |
| PLL_EN | 1 | Test mode with PLL disabled. The reference clock is substituted for the internal VCO output. MPC9330 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable. | Normal operation mode with PLL enabled. |
| PWR_DN | 1 | VCO ÷ 2 (High output frequency range) | VCO ÷ 4 (Low output frequency range) |
| FSELA | 0 | Output divider ÷ 2 | Output divider ÷ 4 |
| FSELB | 0 | Output divider ÷ 2 | Output divider ÷ 4 |
| FSELC | 0 | Output divider ÷ 4 | Output divider ÷ 6 |
| CLK_STOP[0:1] | 11 | See Table 3 | |
| OE/$\overline{MR}$ | 1 | Outputs disabled (high-impedance state) and reset of the device. During reset in external feedback configuration, the PLL feedback loop is open. The VCO is tied to its lowest frequency. The MPC9330 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLK). Reset does not affect PLL lock in internal feedback configuration. | Outputs enabled (active) |
| PWR_DN, FSELA, FSELB and FSELC control the operating PLL frequency range and input/output frequency ratios. See Table 1 to Table 3 for supported frequency ranges and output to input frequency ratios. | | | |

**Table 3: CLOCK OUTPUT SYNCHRONOUS DISABLE (CLK_STOP) FUNCTION TABLE[a]**

| CLK_STOP0 | CLK_STOP1 | QA[0:1] | QB[0:1] | QC[0:1] |
|---|---|---|---|---|
| 0 | 0 | Active | Stopped in logic L state | Stopped in logic L state |
| 0 | 1 | Active | Stopped in logic L state | Active |
| 1 | 0 | Stopped in logic L state | Stopped in logic L state | Active |
| 1 | 1 | Active | Active | Active |

a. Output operation for OE/$\overline{MR}$=1 (outputs enabled). OE/$\overline{MR}$=1=0 will high-impedance tristate all outputs independend on CLK_STOP[0:1]



**Table 4: GENERAL SPECIFICATIONS**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output Termination Voltage | | $V_{CC}$ ÷ 2 | | V | |
| MM | ESD Protection (Machine Model) | 200 | | | V | |
| HBM | ESD Protection (Human Body Model) | 2000 | | | V | |
| LU | Latch–Up Immunity | 200 | | | mA | |
| $C_{PD}$ | Power Dissipation Capacitance | | 10 | | pF | Per output |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | Inputs |

**Table 5: ABSOLUTE MAXIMUM RATINGS[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage Temperature | -65 | 125 | °C | |

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 6: DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40°C to 85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | | | 0.8 | V | LVCMOS |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$=-24 mA[a] |
| $V_{OL}$ | Output Low Voltage | | | 0.55<br>0.30 | V<br>V | $I_{OL}$= 24 mA<br>$I_{OL}$= 12 mA |
| $Z_{OUT}$ | Output Impedance | | 14 - 17 | | Ω | |
| $I_{IN}$ | Input Current[b] | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CC\_PLL}$ | Maximum PLL Supply Current | | 3.0 | 5.0 | mA | $V_{CC\_PLL}$ Pin |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a. The MPC9330 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

b. Inputs have pull–down resistors affecting the input current.

**Table 7: AC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40°C to 85°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Reference Frequency[c] | ÷ 4 feedback[d] | 40 | | 100 | MHz | PLL locked |
| | PLL mode, external feedback | ÷ 8 feedback | 20 | | 50 | MHz | |
| | | ÷ 12 feedback | 13.3 | | 33.3 | MHz | |
| | | ÷ 16 feedback | 10 | | 25 | MHz | |
| | | ÷ 24 feedback | 6.66 | | 16.67 | MHz | |
| | PLL mode, internal feedback | ⟨÷ 16 feedback) | 10 | | 25 | MHz | |
| | Input Reference Frequency in PLL bypass mode[e] | | | | TBD | MHz | |
| $f_{VCO}$ | VCO Lock Frequency Range[f] | | 160 | | 400 | MHz | |
| $f_{XTAL}$ | Crystal Interface Frequency Range[g] | | 10 | | 25 | MHz | |
| $f_{MAX}$ | Output Frequency | ÷ 4 output | 40 | | 100 | MHz | PLL locked |
| | | ÷ 8 output | 20 | | 50 | MHz | |
| | | ÷ 12 output | 13.3 | | 33.3 | MHz | |
| | | ÷ 16 output | 10 | | 25 | MHz | |
| | | ÷ 24 output | 6.66 | | 16.67 | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | | 60 | % | |
| $t_r$, $t_f$ | CCLK Input Rise/Fall Time | | | | 1.0 | ns | 0.8 to 2.0V |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) | CCLK or PCLK to FB_IN | | ±100 | | ps | FB_SEL=1 & PLL locked |
| $t_{sk(o)}$ | Output-to-Output Skew[h] | | | | 150 | ps | |
| DC | Output Duty Cycle | | 45 | 50 | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.55 to 2.4V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 10 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 10 | ns | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1σ)[i] | | TBD | | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1σ) | | TBD | | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1σ) | | TBD | | ps | |
| BW | PLL closed loop bandwidth[j] | ÷ 4 feedback | | | TBD | kHz | |
| | PLL mode, external feedback | ÷ 8 feedback | | | TBD | kHz | |
| | | ÷ 12 feedback | | | TBD | kHz | |
| | | ÷ 16 feedback | | | TBD | kHz | |
| | | ÷ 24 feedback | | | TBD | kHz | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 10 | | ms | |

a. All AC characteristics are design targets and subject to change upon device characterization.
b. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
c. PLL mode requires PLL_EN = 0 to enable the PLL.
d. ÷4 feedback (FB) can be accomplished by setting PWR_DN = 0 and the connection of one ÷2 output to FB_IN. See Table 1 to Table 3 for other feedback configurations.
e. In bypass mode, the MPC9330 divides the input reference clock.
f. The input frequency $f_{ref}$ on CCLK must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$.
g. The usable crystal frequency range depends on the VCO lock frequency and the PLL feedback ratio.
h. See application section for part–to–part skew calculation.
i. See application section for a jitter calculation for other confidence factors than 1 σ.
j. –3 dB point of PLL transfer characteristics.

**Table 8: DC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40°C to 85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | –0.3 | | 0.7 | V | LVCMOS |
| $V_{OH}$ | Output High Voltage | 1.8 | | | V | $I_{OH}$=-15 mA[a] |
| $V_{OL}$ | Output Low Voltage | | | 0.6 | V | $I_{OL}$= 15 mA |
| $Z_{OUT}$ | Output Impedance | | 17 - 20 | | Ω | |
| $I_{IN}$ | Input Current | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CC\_PLL}$ | Maximum PLL Supply Current | | 2.0 | 5.0 | mA | $V_{CCA}$ Pin |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a. The MPC9330 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.

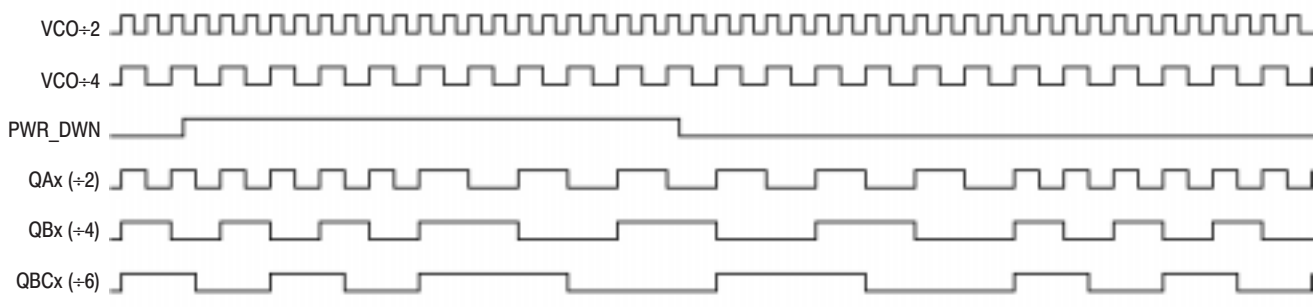
**Table 9: AC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40°C to 85°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Reference Frequency[c] | ÷ 4 feedback[d] | 40 | | 100 | MHz | PLL locked |
| | PLL mode, external feedback | ÷ 8 feedback | 20 | | 50 | MHz | |
| | | ÷ 12 feedback | 13.3 | | 33.3 | MHz | |
| | | ÷ 16 feedback | 10 | | 25 | MHz | |
| | | ÷ 24 feedback | 6.66 | | 16.67 | MHz | |
| | PLL mode, internal feedback | ⟨÷ 16 feedback) | 10 | | 25 | MHz | |
| | Input Reference Frequency in PLL bypass mode[e] | | | | TBD | | |
| $f_{VCO}$ | VCO Lock Frequency Range[f] | | 160 | | 400 | MHz | |
| $f_{XTAL}$ | Crystal Interface Frequency Range[g] | | 10 | | 25 | MHz | |
| $f_{MAX}$ | Output Frequency | ÷ 4 output[g] | 40 | | 100 | MHz | PLL locked |
| | | ÷ 8 output | 20 | | 50 | MHz | |
| | | ÷ 12 output | 13.3 | | 33.3 | MHz | |
| | | ÷ 16 output | 10 | | 25 | MHz | |
| | | ÷ 24 output | 6.66 | | 16.67 | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | | 60 | % | |
| $t_r$, $t_f$ | CCLK Input Rise/Fall Time | | | | 1.0 | ns | 0.7 to 1.7V |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) | CCLK or PCLK to FB_IN | | ±100 | | ps | FB_SEL=1 & PLL locked |
| $t_{sk(o)}$ | Output-to-Output Skew[h] | | | | 150 | ps | |
| DC | Output Duty Cycle | | 45 | 50 | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.6 to 1.8V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 10 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 10 | ns | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1σ)[i] | | TBD | | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1σ) | | TBD | | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1σ) | | TBD | | ps | |
| BW | PLL closed loop bandwidth[j] | ÷ 4 feedback | | | TBD | kHz | |
| | | ÷ 8 feedback | | | TBD | kHz | |
| | | ÷ 12 feedback | | | TBD | kHz | |
| | | ÷ 16 feedback | | | TBD | kHz | |
| | | ÷ 24 feedback | | | TBD | kHz | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 10 | | ms | |

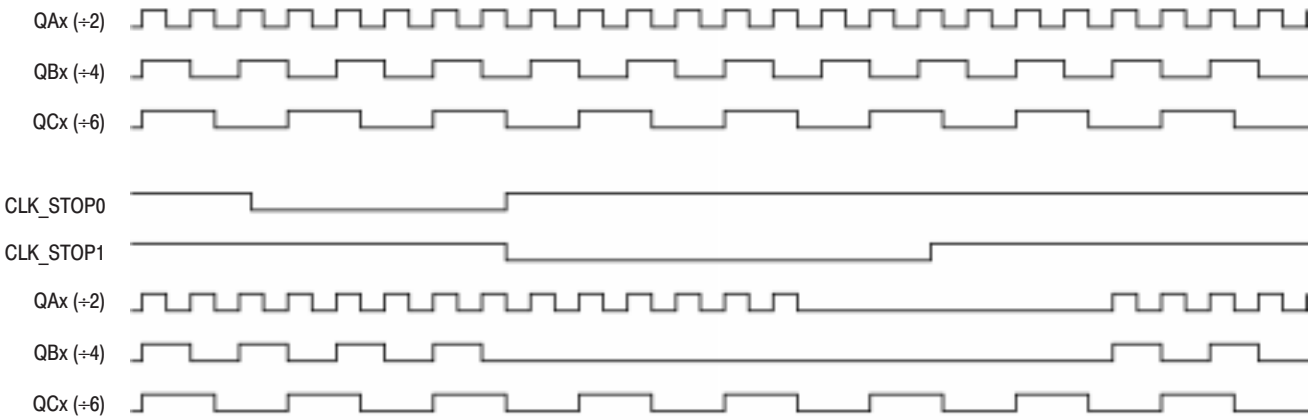
a. All AC characteristics are design targets and subject to change upon device characterization.
b. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
c. PLL mode requires PLL_EN = 0 to enable the PLL.
d. ÷4 feedback (FB) can be accomplished by setting PWR_DN = 0 and the connection of one ÷2 output to FB_IN. See Table 1 to Table 3 for other feedback configurations.
e. In bypass mode, the MPC9330 divides the input reference clock.
f. The input frequency $f_{ref}$ on CCLK must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$.
g. The usable crystal frequency range depends on the VCO lock frequency and the PLL feedback ratio.
h. See application section for part–to–part skew calculation.
i. See application section for a jitter calculation for other confidence factors than 1 σ.
j. –3 dB point of PLL transfer characteristics.

## APPLICATIONS INFORMATION

### Output power down (PWR_DN) timing diagram




### Output clock stop (CLK_STOP) timing diagram




### Programming the MPC9330

The MPC9330 supports output clock frequencies from 6.67 to 200 MHz. Different feedback and output divider configurations can be used to achieve the desired input to output frequency relationship. The feedback frequency and divider should be used to situate the VCO in the frequency lock range between 200 and 400 MHz for stable and optimal operation. The FSELA, FSELB, FSELC and PWR_DN pins select the desired output clock frequencies. Possible frequency ratios of the reference clock input to the outputs are 1:4, 1:3, 1:2, 1:1, 2:3, 4:3 and 3:2. Tables 10 through 12 illustrate the various output configurations and frequency ratios supported by the MPC9330.

**Table 10: MPC9330 Example Configurations (Internal Feedback: FB_SEL = 0)**

| fref[a] [MHz] | PWR_DN | FSELA | FSELB | FSELC | QA[0:1]:fref ratio | QB[0:1]:fref ratio | QC[0:1]:fref ratio |
|---|---|---|---|---|---|---|---|
| 10.0-25.0 | 0 | 0 | 0 | 0 | fref · 4 (40-100 MHz) | fref · 4 (40-100 MHz) | fref · 2 (20-50 MHz) |
| | 0 | 0 | 0 | 1 | fref · 4 (40-100 MHz) | fref · 4 (40-100 MHz) | fref ·4÷3 (13.3-33.3 MHz) |
| | 0 | 0 | 1 | 0 | fref · 4 (40-100 MHz) | fref · 2 (20-50 MHz) | fref · 2 (20-50 MHz) |
| | 0 | 0 | 1 | 1 | fref · 4 (40-100 MHz) | fref · 2 (20-50 MHz) | fref ·4÷3 (13.3-33.3 MHz) |
| | 0 | 1 | 0 | 0 | fref · 2 (20-50 MHz) | fref · 4 (40-100 MHz) | fref · 2 (20-50 MHz) |
| | 0 | 1 | 0 | 1 | fref · 2 (20-50 MHz) | fref · 4 (40-100 MHz) | fref ·4÷3 (13.3-33.3 MHz) |
| | 0 | 1 | 1 | 0 | fref · 2 (20-50 MHz) | fref · 2 (20-50 MHz) | fref · 2 (20-50 MHz) |
| | 0 | 1 | 1 | 1 | fref · 2 (20-50 MHz) | fref · 2 (20-50 MHz) | fref ·4÷3 (13.3-33.3 MHz) |
| | 1 | 0 | 0 | 0 | fref · 2 (20-50 MHz) | fref · 2 (20-50 MHz) | fref (10-25 MHz) |
| | 1 | 0 | 0 | 1 | fref · 2 (20-50 MHz) | fref · 2 (20-50 MHz) | fref ·2÷3 (6.67-16.67 MHz) |
| | 1 | 0 | 1 | 0 | fref · 2 (20-50 MHz) | fref (10-25 MHz) | fref (10-25 MHz) |
| | 1 | 0 | 1 | 1 | fref · 2 (20-50 MHz) | fref (10-25 MHz) | fref ·2÷3 (6.67-16.67 MHz) |
| | 1 | 1 | 0 | 0 | fref (10-25 MHz) | fref · 2 (20-50 MHz) | fref (10-25 MHz) |
| | 1 | 1 | 0 | 1 | fref (10-25 MHz) | fref · 2 (20-50 MHz) | fref ·2÷3 (6.67-16.67 MHz) |
| | 1 | 1 | 1 | 0 | fref (10-25 MHz) | fref (10-25 MHz) | fref (10-25 MHz) |
| | 1 | 1 | 1 | 1 | fref (10-25 MHz) | fref (10-25 MHz) | fref ·2÷3 (6.67-16.67 MHz) |

a. fref is the input clock reference frequency (CCLK or XTAL)

**Table 11: MPC9330 Example Configurations (External Feedback and PWR_DN = 0)**

| PLL Feedback | fref[a] [MHz] | FSELA | FSELB | FSELC | QA[0:1]:fref ratio | QB[0:1]:fref ratio | QC[0:1]:fref ratio |
|---|---|---|---|---|---|---|---|
| VCO ÷ 4[b] | 40-100 | 0 | 0 | 0 | fref (40-100 MHz) | fref (40-100 MHz) | fref÷2 (20-50 MHz) |
| | | 0 | 0 | 1 | fref (40-100 MHz) | fref (40-100 MHz) | fref÷3 (13.3-33.3MHz) |
| | | 0 | 1 | 0 | fref (40-100 MHz) | fref÷2 (20-50 MHz) | fref÷2 (20-50 MHz) |
| | | 0 | 1 | 1 | fref (40-100 MHz) | fref÷2 (20-50 MHz) | fref÷3 (13.3-33.3MHz) |
| VCO ÷ 8[c] | 20-50 | 1 | 0 | 0 | fref (20-50 MHz) | fref ·2 (40-100 MHz) | fref (20-50 MHz) |
| | | 1 | 0 | 1 | fref (20-50 MHz) | fref ·2 (40-100 MHz) | fref ·2÷3 (13.3-33.3 MHz) |
| | | 1 | 1 | 0 | fref (20-50 MHz) | fref (20-50 MHz) | fref (20-50 MHz) |
| | | 1 | 1 | 1 | fref (20-50 MHz) | fref (20-50 MHz) | fref ·2÷3 (13.3-33.3 MHz) |
| VCO ÷ 12[d] | 13.3-33.3 | 0 | 0 | 0 | fref ·3 (40-100 MHz) | fref ·3 (40-100 MHz) | fref (13.3-33.3 MHz) |
| | | 0 | 1 | 0 | fref ·3 (40-100 MHz) | fref ·3÷2 (20-50 MHz) | fref (13.3-33.3 MHz) |
| | | 1 | 0 | 0 | fref ·3÷2 (20-50 MHz) | fref ·3 (40-100 MHz) | fref (13.3-33.3 MHz) |
| | | 1 | 1 | 0 | fref ·3÷2 (20-50 MHz) | fref ·3÷2 (20-50 MHz) | fref (13.3-33.3 MHz) |

a. fref is the input clock reference frequency (CCLK or XTAL)
b. QAx connected to FB_IN and FSELA=0, PWR_DN=0
c. QAx connected to FB_IN and FSELA=1, PWR_DN=0
d. QCx connected to FB_IN and FSELC=1, PWR_DN=0

**Table 12: MPC9330 Example Configurations (External Feedback and PWR_DN = 1)**

| PLL Feedback | fref[a] [MHz] | FSELA | FSELB | FSELC | QA[0:1]:fref ratio | QB[0:1]:fref ratio | QC[0:1]:fref ratio |
|---|---|---|---|---|---|---|---|
| VCO ÷ 16[b] | 10-25 | 1 | 0 | 0 | fref (10-25 MHz) | fref ·2 (20-50 MHz) | fref (10-25 MHz) |
| | | 1 | 0 | 1 | fref (10-25 MHz) | fref ·2 (20-50 MHz) | fref ·2÷3 (6.6-16.6 MHz) |
| | | 1 | 1 | 0 | fref (10-25 MHz) | fref (10-25 MHz) | fref (10-25 MHz) |
| | | 1 | 1 | 1 | fref (10-25 MHz) | fref (10-25 MHz) | fref ·2÷3 (6.6-16.6 MHz) |
| VCO ÷ 24[c] | 6.67-16.67 | 0 | 0 | 1 | fref ·3 (20-50 MHz) | fref ·3 (20-50 MHz) | fref (6.67-16.67 MHz) |
| | | 0 | 1 | 1 | fref ·3 (20-50 MHz) | fref ·3÷2 (10-25 MHz) | fref (6.67-16.67 MHz) |
| | | 1 | 0 | 1 | fref ·3÷2 (10-25 MHz) | fref ·3 (20-50 MHz) | fref (6.67-16.67 MHz) |
| | | 1 | 1 | 1 | fref ·3÷2 (10-25 MHz) | fref ·3÷2 (10-25 MHz) | fref (6.67-16.67 MHz) |

a. fref is the input clock reference frequency (CCLK or XTAL)
b. QAx connected to FB_IN and FSELA=1, PWR_DN=1
c. QCx connected to FB_IN and FSELC=1, PWR_DN=1

## APPLICATIONS INFORMATION

### Power Supply Filtering

The MPC9330 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the $V_{CCA\_PLL}$ power supply impacts the device characteristics, for instance I/O jitter. The MPC9330 provides separate power supplies for the output buffers ($V_{CC}$) and the phase-locked loop ($V_{CCA}$) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the $V_{CC\_PLL}$ pin for the MPC9330. Figure 3 illustrates a typical power supply filter scheme. The MPC9330 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor $R_F$. From the data sheet the $I_{CCA}$ current (the current sourced through the $V_{CC\_PLL}$ pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V ($V_{CC}$=3.3V or $V_{CC}$=2.5V) must be maintained on the $V_{CC\_PLL}$ pin. The resistor $R_F$ shown in Figure 3 "$V_{CC\_PLL}$ Power Supply Filter" must have a resistance of 270Ω ($V_{CC}$=3.3V) or 9-10Ω ($V_{CC}$=2.5V) to meet the voltage drop criteria.

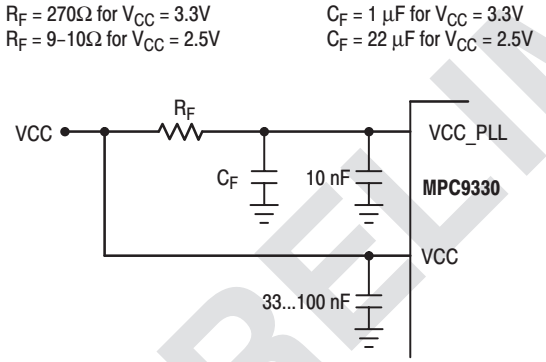



**Figure 3. $V_{CC\_PLL}$ Power Supply Filter**

The minimum values for $R_F$ and the filter capacitor $C_F$ are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3 "$V_{CC\_PLL}$ Power Supply Filter", the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9330 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

### Driving Transmission Lines

The MPC9330 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}$÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9330 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 "Single versus Dual Transmission Lines" illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9330 clock driver is effectively doubled due to its capability to drive multiple lines.

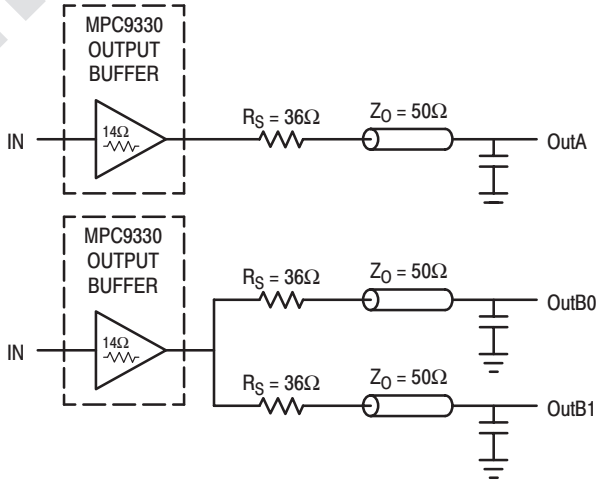



**Figure 4. Single versus Dual Transmission Lines**

The waveform plots in Figure 5 "Single versus Dual Line Termination Waveforms" show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9330 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9330. The output waveform in Figure 5 "Single versus Dual Line Termination Waveforms" shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the

parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S ( Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\Omega \parallel 50\Omega$$
$$R_S = 36\Omega \parallel 36\Omega$$
$$R_0 = 14\Omega$$
$$V_L = 3.0 ( 25 \div (18+17+25)$$
$$= 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

1. Final skew data pending specification.

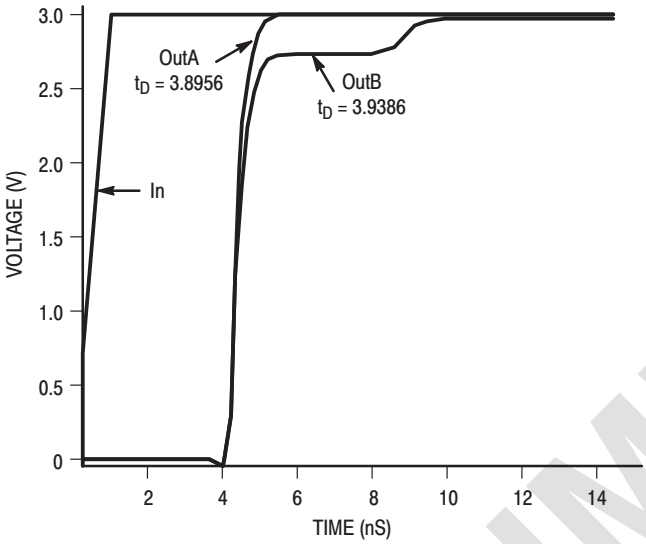



**Figure 5. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

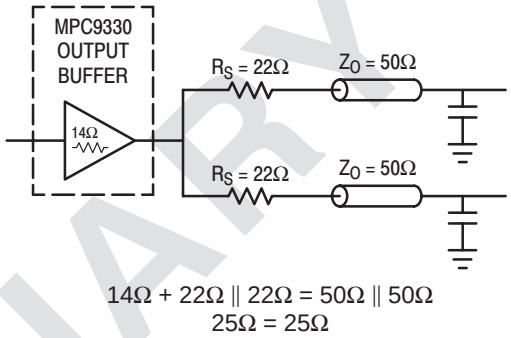



**Figure 6. Optimized Dual Line Termination**

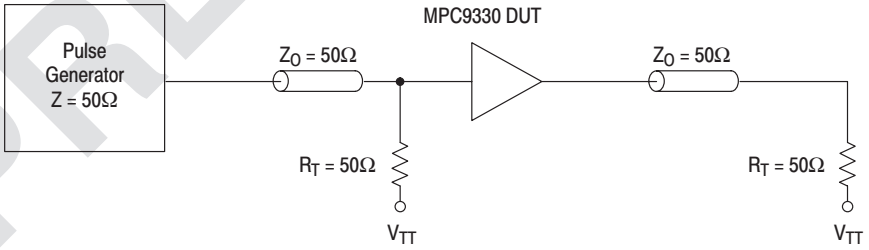
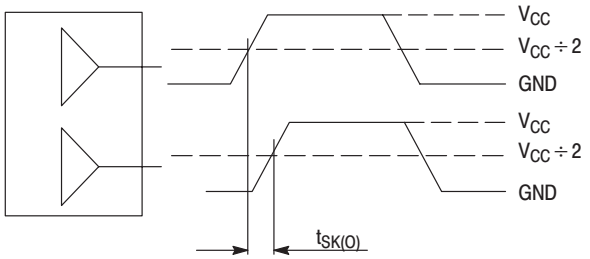



**Figure 7. CCLK MPC9330 AC test reference for $V_{cc}$ = 3.3V and $V_{cc}$ = 2.5V**




The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 8. Output–to–output Skew $t_{SK(O)}$**

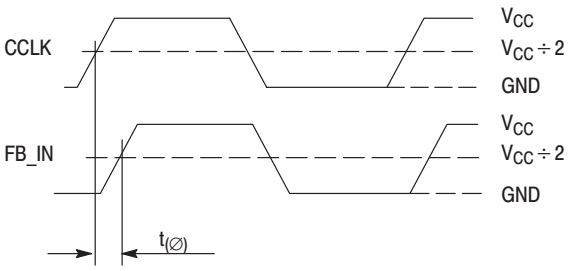
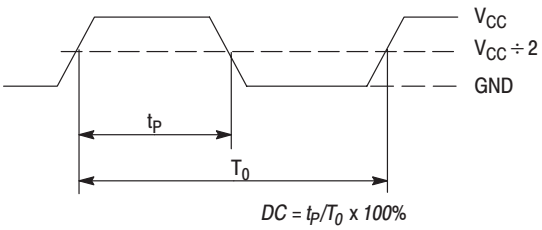
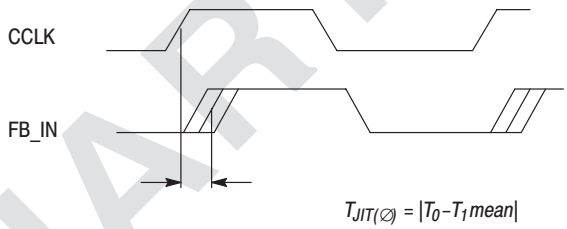



**Figure 9. Propagation delay ($t_{(\varnothing)}$, static phase offset) test reference**



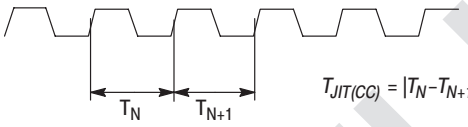

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 10. Output Duty Cycle (DC)**



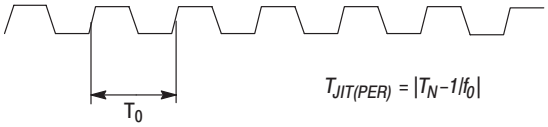

The deviation in $t_0$ for a controlled edge with respect to a $t_0$ mean in a random sample of cycles

**Figure 11. I/O Jitter**




The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

**Figure 12. Cycle–to–cycle Jitter**




The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

**Figure 13. Period Jitter**

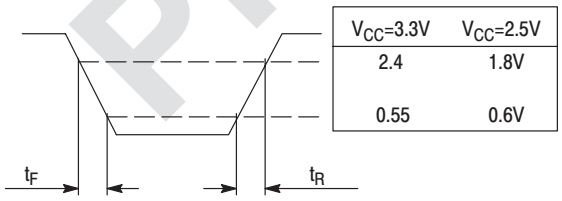



**Figure 14. Output Transition Time Test Reference**

**Order Number: MPC9331/D**
**Rev 0, 11/2001**

*Preliminary Information*

# 3.3V/2.5V 1:6 LVCMOS PLL Clock Generator

**MPC9331**

**LOW VOLTAGE 3.3V/2.5V LVCMOS 1:6 CLOCK GENERATOR**

**FA SUFFIX**
32 LEAD LQFP PACKAGE
CASE 873A

2

The MPC9331 is a 3.3V or 2.5V compatible, 1:6 PLL based clock generator targeted for high performance low-skew clock distribution in mid-range to high-performance telecom, networking, and computing applications. With output frequencies up to 200 MHz and output skews less than 150 ps[1], the device meets the needs of most the demanding clock applications. The MPC9331 is specified for the extended temperature range of –40 to +85°C.

**Features**

- 1:6 PLL based low-voltage clock generator
- 2.5V or 3.3V power supply
- Generates clock signals up to 200 MHz
- Maximum output skew of 150 ps[1]
- Differential LVPECL reference clock input
- Alternative LVCMOS PLL reference clock input
- Internal and external PLL feedback
- Supports zero-delay operation in external feedback mode
- PLL multiplies the reference clock by 4x, 3x, 2x, 1x, 4/3x, 3/2x, 2/3x, x/2, x/3 or x/4
- Synchronous output clock stop in logic low eliminates output runt pulses
- Power_down feature reduces output clock frequency
- Drives up to 12 clock lines
- 32 lead LQFP packaging
- Ambient temperature range –40°C to +85°C
- Pin and function compatible to the MPC931

**Functional Description**

The MPC9331 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9331 requires either the selection of internal PLL feedback or the connection of one of the device outputs to the feedback input to close the PLL feedback path in external feedback mode. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. In external PLL feedback configuration and with the available post-PLL dividers (divide-by-2, divide-by-4, and divide-by-6), the internal VCO of the MPC9331 is running at either 2x, 4x, 6x, 8x, or 12x of the reference clock frequency. In internal feedback configuration (divide-by-8) the internal VCO is running 8x of the reference frequency. The frequency of the QA, QB, QC output banks is a division of the VCO frequency and can be configured independently for each output bank using the FSELA, FSELB, and FSELC pins, respectively. The available output to input frequency ratios are 4x, 3x, 2x, 1x, 4/3x, 3/2x, 2/3x, x/2, x/3, or x/4.

The REF_SEL pin selects the differential LVPECL or the LVCMOS compatible input as the reference clock signal. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply. The outputs can be disabled (high-impedance) by deasserting the OE pin. In the PLL configuration with external feedback selected, deasserting OE causes the PLL to loose lock due to missing feedback signal presence at FB_IN. Asserting OE will enable the outputs and close the phase locked loop, enabling the PLL to recover to normal operation. The MPC9331 output clock stop control allows the outputs to start and stop synchronously in logic low state, without the potential generation of runt pulses.

The MPC9331 is fully 2.5V and 3.3V compatible and requires no external loop filter components. The inputs (except PCLK) accept LVCMOS except signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9331 outputs can drive one or two traces giving the devices an effective fanout of 1:12. The device is packaged in a 7x7 mm$^2$ 32-lead LQFP package.

1. Final specification of this parameter is pending characterization



**Rev 0**

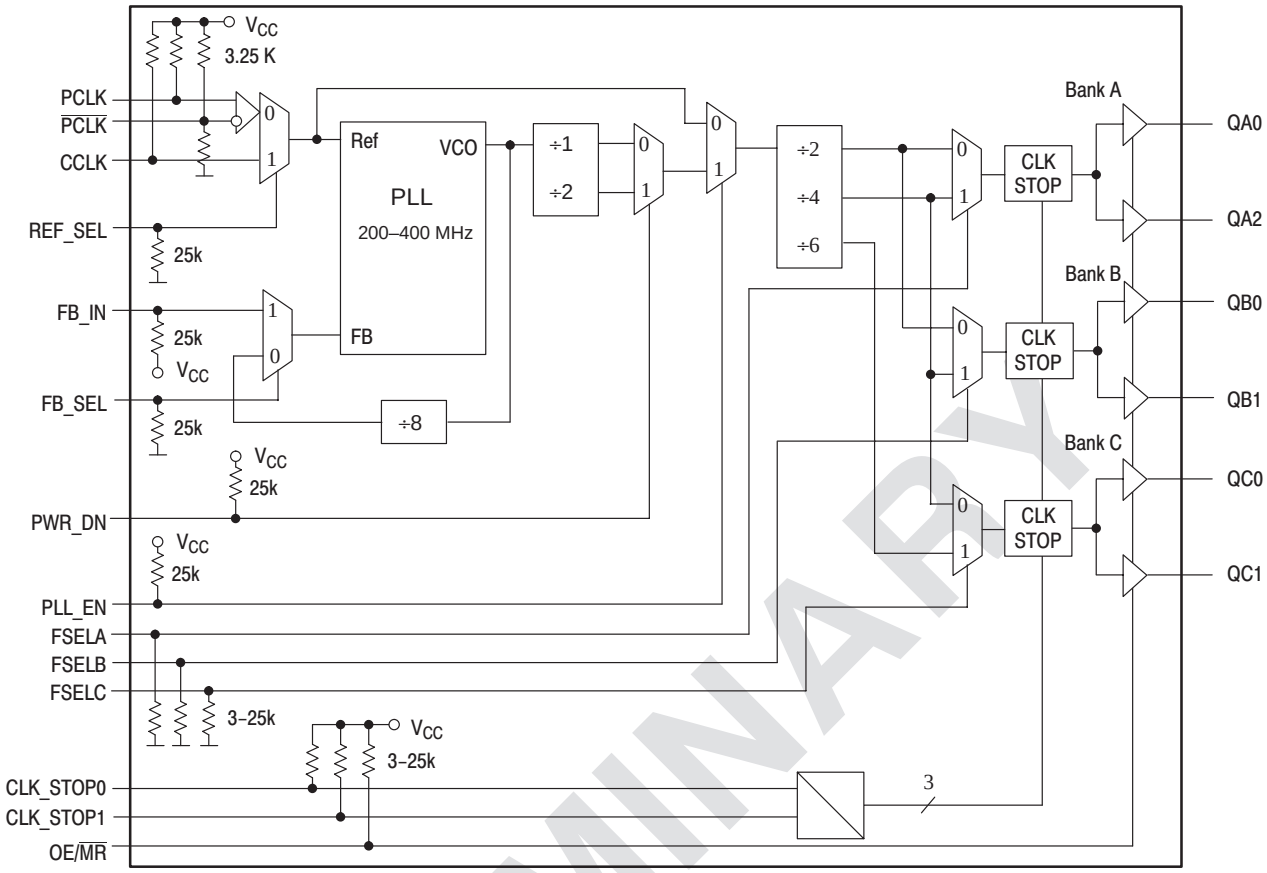
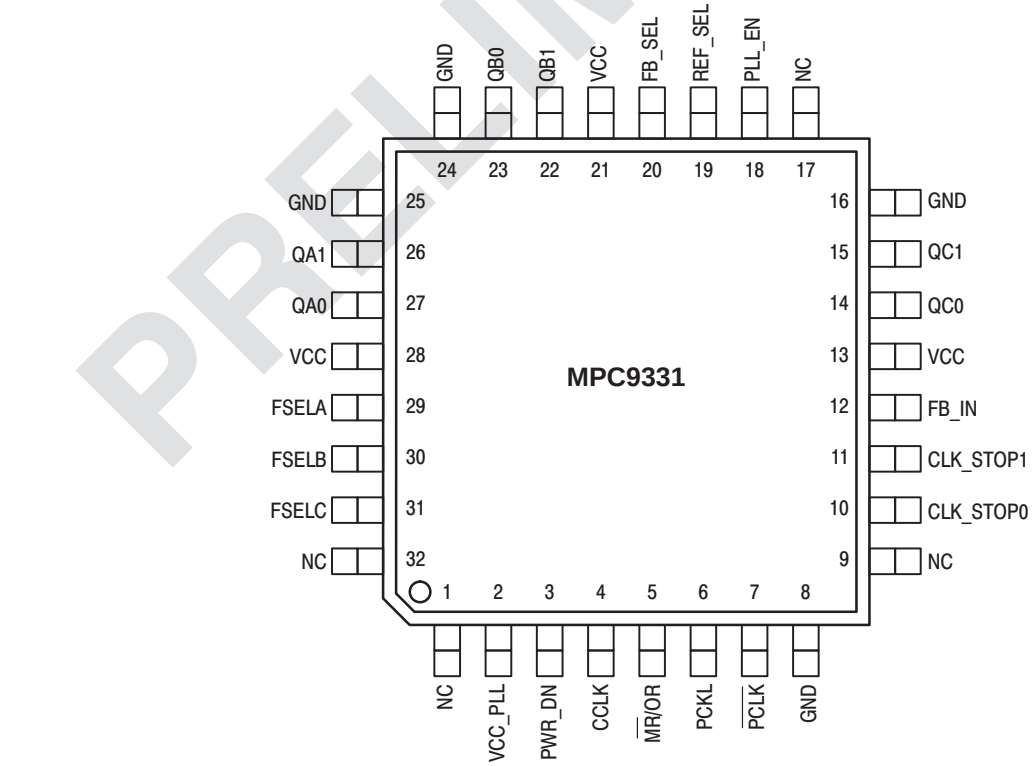



**Figure 1. MPC9331 Logic Diagram**




The MPC9331 requires an external RC filter for the analog VCC_PLL power supply pin. Please see application section for details.

**Figure 2. MPC9331 32–Lead Package Pinout** (Top View)

**Table 1. Pin Configuration**

| Pin | I/O | Type | Function |
|---|---|---|---|
| CCLK | Input | LVCMOS | PLL reference clock signal |
| PCLK, $\overline{\text{PCLK}}$ | Input | LVPECL | Differential PECL reference clock signal |
| FB_IN | Input | LVCMOS | PLL feedback signal input, connect to an output |
| FB_SEL | Input | LVCMOS | Feedback select |
| REF_SEL | Input | LVCMOS | Reference clock select |
| PWR_DN | Input | LVCMOS | Output frequency and power down select |
| FSELA | Input | LVCMOS | Frequency divider select for bank A outputs |
| FSELB | Input | LVCMOS | Frequency divider select for bank B outputs |
| FSELC | Input | LVCMOS | Frequency divider select for bank C outputs |
| PLL_EN | Input | LVCMOS | PLL enable/disable |
| CLK_STOP0-1 | Input | LVCMOS | Clock output enable/disable |
| $\overline{\text{MR}}$/OE | Input | LVCMOS | Output enable/disable (high-impedance tristate) and device reset |
| QA0-1, QB0-1, QC0-1 | Output | LVCMOS | Clock outputs |
| GND | Supply | Ground | Negative power supply (GND) |
| $V_{CC\_PLL}$ | Supply | $V_{CC}$ | PLL positive power supply (analog power supply). The MPC9331 requires an external RC filter for the analog power supply pin $V_{CC\_PLL}$. Please see applications section for details. |
| $V_{CC}$ | Supply | $V_{CC}$ | Positive power supply for I/O and core. All $V_{CC}$ pins must be connected to the positive power supply for correct operation |

**Table 2. Function Table**

| Control | Default | 0 | 1 |
|---|---|---|---|
| REF_SEL | 0 | PCLK is the PLL reference clock | CCLK is the PLL reference clock |
| FB_SEL | 1 | Internal PLL feedback of 8. $f_{VCO} = 8 * f_{ref}$ | External feedback. Zero-delay operation enabled for CCLK or PCLK as reference clock |
| PLL_EN | 1 | Test mode with PLL disabled. The reference clock is substituted for the internal VCO output. MPC9331 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable. | Normal operation mode with PLL enabled. |
| PWR_DN | 1 | VCO ÷ 1 (High output frequency range) | VCO ÷ 2 (Low output frequency range) |
| FSELA | 0 | Output divider ÷ 2 | Output divider ÷ 4 |
| FSELB | 0 | Output divider ÷ 2 | Output divider ÷ 4 |
| FSELC | 0 | Output divider ÷ 4 | Output divider ÷ 6 |
| $\overline{\text{MR}}$/OE | 1 | Outputs disabled (high-impedance state) and reset of the device. During reset in external feedback configuration, the PLL feedback loop is open. The VCO is tied to its lowest frequency. The MPC9331 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLK or PCLK). Reset does not affect PLL lock in internal feedback configuration. | Outputs enabled (active) |
| CLK_STOP[0:1] | 11 | See Table 3 | |
| PWR_DN, FSELA, FSELB and FSELC control the operating PLL frequency range and input/output frequency ratios. See Table 1 – 3 for supported frequency ranges and output to input frequency ratios. | | | |

**Table 3. Clock Output Synchronous Disable (CLK_STOP) Function Table [a]**

| CLK_STOP0 | CLK_STOP1 | QA[0:1] | QB[0:1] | QC[0:1] |
|---|---|---|---|---|
| 0 | 0 | Active | Stopped in logic L state | Stopped in logic L state |
| 0 | 1 | Active | Stopped in logic L state | Active |
| 1 | 0 | Stopped in logic L state | Stopped in logic L state | Active |
| 1 | 1 | Active | Active | Active |

a. Output operation for OE/$\overline{MR}$=1 (outputs enabled). OE/$\overline{MR}$=1=0 will high-impedance tristate all outputs independend on CLK_STOP[0:1]

2

**Table 4. General Specifications**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output termination voltage | | $V_{CC} \div 2$ | | V | |
| MM | ESD protection (Machine model) | 200 | | | V | |
| HBM | ESD protection (Human body model) | 2000 | | | V | |
| LU | Latch-up immunity | 200 | | | mA | |
| $C_{PD}$ | Power dissipation capacitance | | 10 | | pF | Per output |
| $C_{IN}$ | Input capacitance | | 4.0 | | pF | Inputs |

**Table 5. Absolute Maximum Ratings[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -65 | 125 | °C | |

a Absolute maximum continuos ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 6. DC Characteristics** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40°C to +85°C)

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | | | | 0.8 | V | LVCMOS |
| $V_{PP}$ | Peak-to-peak input voltage | PCLK, $\overline{PCLK}$ | 250 | | | mV | LVPECL |
| $V_{CMR}$[a] | Common Mode Range | PCLK, $\overline{PCLK}$ | 1.0 | | $V_{CC}$ - 0.6 | V | LVPECL |
| $V_{OH}$ | Output High Voltage | | 2.4 | | | V | $I_{OH}$ = -24 mA[b] |
| $V_{OL}$ | Output Low Voltage | | | | 0.55<br>0.30 | V<br>V | $I_{OL}$ = 24 mA<br>$I_{OL}$ = 12 mA |
| $Z_{OUT}$ | Output impedance | | | 14 - 17 | | Ω | |
| $I_{IN}$ | Input Current[c] | | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CC\_PLL}$ | Maximum PLL Supply Current | | | 3.0 | 5.0 | mA | $V_{CC\_PLL}$ Pin |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | | 1.0 | mA | All $V_{CC}$ Pins |

a $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (DC) specification

b The MPC9331 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

c Inputs have pull-down resistors affecting the input current.

**Table 7. AC Characteristics** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40°C to +85°C)[a] [b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input reference frequency[c] | ÷2 feedback[d] | 100.0 | | 200.0 | MHz | PLL locked |
| | PLL mode, external feedback | ÷4 feedback | 50.0 | | 100.0 | MHz | |
| | | ÷6 feedback | 33.3 | | 66.6 | MHz | |
| | | ÷8 feedback | 25.0 | | 50.0 | MHz | |
| | | ÷12 feedback | 16.67 | | 33.33 | MHz | |
| | PLL mode, internal feedback | (÷8 feedback) | 25.0 | | 50.0 | MHz | |
| | Input reference frequency in PLL bypass mode[e] | | | | TBD | MHz | |
| $f_{VCO}$ | VCO lock frequency range[f] | | 200 | | 400 | MHz | |
| $f_{MAX}$ | Output Frequency | ÷2 output | 100.0 | | 200.0 | MHz | PLL locked |
| | | ÷4 output | 50.0 | | 100.0 | MHz | |
| | | ÷6 output | 33.3 | | 66.6 | MHz | |
| | | ÷8 output | 25.0 | | 50.0 | MHz | |
| | | ÷12 output | 16.67 | | 33.33 | MHz | |
| $V_{PP}$ | Peak-to-peak input voltage PCLK, $\overline{PCLK}$ | | 500 | | 1000 | mV | LVPECL |
| $V_{CMR}$[g] | Common Mode Range PCLK, $\overline{PCLK}$ | | 1.2 | | $V_{CC}$ - 0.9 | V | LVPECL |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | | 60 | % | |
| tr, tf | CCLK Input Rise/Fall Time | | | | 1.0 | ns | 0.8 to 2.0V |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) CCLK or PCLK to FB_IN) | | | ±100 | | ps | FB_SEL = 1 and PLL locked |
| $t_{sk(O)}$ | Output-to-output Skew[h] | | | | 150 | ps | |
| DC | Output duty cycle | | 45 | 50 | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.55 to 2.4V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 10 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 10 | ns | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ)[i] | | TBD | | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | TBD | | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1 σ) | | TBD | | ps | |
| BW | PLL closed loop bandwidth[j] | ÷ 2 feedback | | | TBD | kHz | |
| | PLL mode, external feedback | ÷ 4 feedback | | | TBD | kHz | |
| | | ÷ 6 feedback | | | TBD | kHz | |
| | | ÷ 8 feedback | | | TBD | kHz | |
| | | ÷12 feedback | | | TBD | kHz | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 10 | | ms | |

NOTES:
a All AC characteristics are design targets and subject to change upon device characterization
b AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$
c PLL mode requires PLL_EN = 1 to enable the PLL
d ÷2 feedback (FB) can be accomplished by setting PWR_DN = 0 and the connection of one ÷2 output to FB_IN. See Table 1 to Table 3 for other feedback configurations
e In bypass mode, the MPC9331 divides the input reference clock.
f The input frequency $f_{ref}$ must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$
g $V_{CMR}$ (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ or $V_{PP}$ impacts static phase offset $t_{(\varnothing)}$
h See application section for part-to-part skew calculation
i See application section for a jitter calculation for other confidence factors than 1 σ
j -3 dB point of PLL transfer characteristics

**Table 8. DC Characteristics** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40°C to +85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | -0.3 | | 0.7 | V | LVCMOS |
| $V_{PP}$ | Peak-to-peak input voltage<br>PCLK, $\overline{PCLK}$ | 250 | | | mV | LVPECL |
| $V_{CMR}$[a] | Common Mode Range<br>PCLK, $\overline{PCLK}$ | 1.0 | | $V_{CC}$ - 0.6 | V | LVPECL |
| $V_{OH}$ | Output High Voltage | 1.8 | | | V | $I_{OH}$ = -15 mA[b] |
| $V_{OL}$ | Output Low Voltage | | | 0.6 | V | $I_{OL}$ = 15 mA |
| $Z_{OUT}$ | Output impedance | | 17 - 20 | | Ω | |
| $I_{IN}$ | Input Current | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CC\_PLL}$ | Maximum PLL Supply Current | | 2.0 | 5.0 | mA | $V_{CCA}$ Pin |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

NOTES:

a $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (DC) specification

b The MPC9331 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.

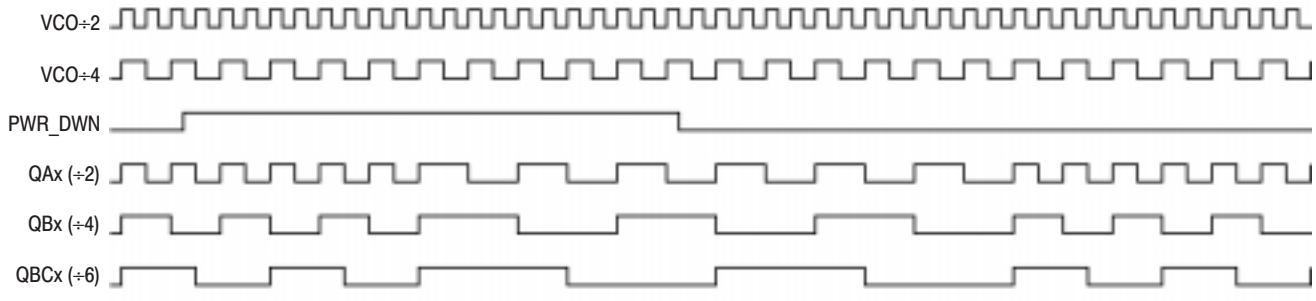
**Table 9. AC Characteristics** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40°C to +85°C)[a] [b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input reference frequency[c] | ÷2 feedback[d] | 100.0 | | 200.0 | MHz | PLL locked |
| | PLL mode, external feedback | ÷4 feedback | 50.0 | | 100.0 | MHz | |
| | | ÷6 feedback | 33.3 | | 66.6 | MHz | |
| | | ÷8 feedback | 25.0 | | 50.0 | MHz | |
| | | ÷12 feedback | 16.67 | | 33.33 | MHz | |
| | PLL mode, internal feedback | (÷8 feedback) | 25.0 | | 50.0 | MHz | |
| | Input reference frequency in PLL bypass mode[e] | | | | TBD | MHz | |
| $f_{VCO}$ | VCO lock frequency range[f] | | 200 | | 400 | MHz | |
| $f_{MAX}$ | Output Frequency | ÷2 output | 100.0 | | 200.0 | MHz | PLL locked |
| | | ÷4 output | 50.0 | | 100.0 | MHz | |
| | | ÷6 output | 33.3 | | 66.6 | MHz | |
| | | ÷8 output | 25.0 | | 50.0 | MHz | |
| | | ÷12 output | 16.67 | | 33.33 | MHz | |
| $V_{PP}$ | Peak-to-peak input voltage PCLK, $\overline{PCLK}$ | | 500 | | 1000 | mV | LVPECL |
| $V_{CMR}$[g] | Common Mode Range PCLK, $\overline{PCLK}$ | | 1.2 | | $V_{CC}$ - 0.6 | V | LVPECL |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | | 60 | % | |
| tr, tf | CCLK Input Rise/Fall Time | | | | 1 | ns | 0.7 to 1.7V |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) CCLK or PCLK to FB_IN) | | | ±100 | | ps | FB_SEL = 1 and PLL locked |
| $t_{sk(O)}$ | Output-to-output Skew[h] | | | | 150 | ps | |
| DC | Output duty cycle | | 45 | 50 | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.6 to 1.8V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 10 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 10 | ns | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ)[i] | | TBD | | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | TBD | | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1 σ) | | TBD | | ps | |
| BW | PLL closed loop bandwidth[j] | ÷2 feedback | | | TBD | kHz | |
| | | ÷4 feedback | | | TBD | kHz | |
| | | ÷6 feedback | | | TBD | kHz | |
| | | ÷8 feedback | | | TBD | kHz | |
| | | ÷12 feedback | | | TBD | kHz | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 10 | | ms | |

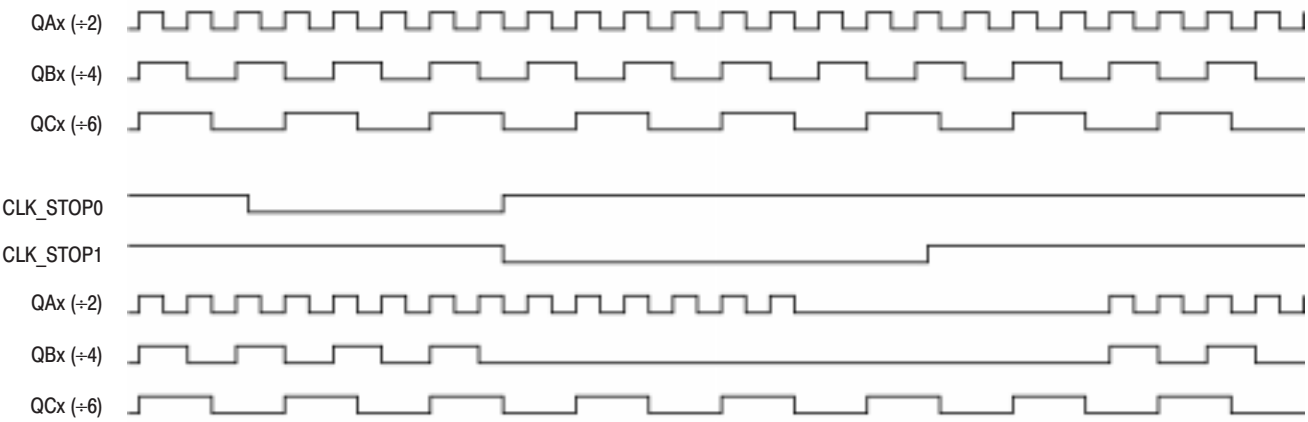
NOTES:
a All AC characteristics are design targets and subject to change upon device characterization
b AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$
c PLL mode requires PLL_EN=1 to enable the PLL
d ÷2 feedback (FB) can be accomplished by setting PWR_DN=0 and the connection of one ÷2 output to FB_IN. See Table 1 to Table 3 for other feedback configurations
e In bypass mode, the MPC9331 divides the input reference clock.
f The input frequency $f_{ref}$ on CCLK must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$
g $V_{CMR}$ (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ or $V_{PP}$ impacts static phase offset $t_{(\varnothing)}$
h See application section for part-to-part skew calculation
i See application section for a jitter calculation for other confidence factors than 1 σ
j -3 dB point of PLL transfer characteristics

## APPLICATIONS INFORMATION

### Output power down (PWR_DN) timing diagram




### Output clock stop (CLK_STOP) timing diagram




### Programming the MPC9331

The MPC9331 supports output clock frequencies from 16.67 to 200 MHz. Different feedback and output divider configurations can be used to achieve the desired input to output frequency relationship. The feedback frequency and divider should be used to situate the VCO in the frequency lock range between 200 and 400 MHz for stable and optimal operation. The FSELA, FSELB, FSELC and PWR_DN pins select the desired output clock frequencies. Possible frequency ratios of the reference clock input to the outputs are 4:1, 3:1, 2:1, 1:1, 1:2, 2:3 and 3:2. Table 10 illustrates the various output configurations and frequency ratios supported by the MPC9331. See also Table 10 and 11 for further reference.

**Table 10. MPC9331 Example Configurations** (Internal Feedback and FB_SEL = 0)

| fref[a] [MHz] | PWR_DN | FSELA | FSELB | FSELC | QA[0:1]:fref ratio | QB[0:1]:fref ratio | QC[0:1]:fref ratio |
|---|---|---|---|---|---|---|---|
| 25.0 - 50.0 | 0 | 0 | 0 | 0 | fref · 4 (100-200 MHz) | fref · 4 (100-200 MHz) | fref · 2 (50-100 MHz) |
| | 0 | 0 | 0 | 1 | fref · 4 (100-200 MHz) | fref · 4 (100-200 MHz) | fref ·4÷3 (33.3-66.6 MHz) |
| | 0 | 0 | 1 | 0 | fref · 4 (100-200 MHz) | fref · 2 (50-100 MHz) | fref · 2 (50-100 MHz) |
| | 0 | 0 | 1 | 1 | fref · 4 (100-200 MHz) | fref · 2 (50-100 MHz) | fref ·4÷3 (33.3-66.6 MHz) |
| | 0 | 1 | 0 | 0 | fref · 2 (50-100 MHz) | fref · 4 (100-200 MHz) | fref · 2 (50-100 MHz) |
| | 0 | 1 | 0 | 1 | fref · 2 (50-100 MHz) | fref · 4 (100-200 MHz) | fref ·4÷3 (33.3-66.6 MHz) |
| | 0 | 1 | 1 | 0 | fref · 2 (50-100 MHz) | fref · 2 (50-100 MHz) | fref · 2 (50-100 MHz) |
| | 0 | 1 | 1 | 1 | fref · 2 (50-100 MHz) | fref · 2 (50-100 MHz) | fref ·4÷3 (33.3-66.6 MHz) |
| | 1 | 0 | 0 | 0 | fref · 2 (50-100 MHz) | fref · 2 (50-100 MHz) | fref (25.0-50 MHz) |
| | 1 | 0 | 0 | 1 | fref · 2 (50-100 MHz) | fref · 2 (50-100 MHz) | fref ·2÷3 (16.67-33.3 MHz) |
| | 1 | 0 | 1 | 0 | fref · 2 (50-100 MHz) | fref (25.0-50 MHz) | fref (25.0-50 MHz) |
| | 1 | 0 | 1 | 1 | fref · 2 (50-100 MHz) | fref (25.0-50 MHz) | fref ·2÷3 (16.67-33.3 MHz) |
| | 1 | 1 | 0 | 0 | fref (25.0-50 MHz) | fref · 2 (50-100 MHz) | fref (25.0-50 MHz) |
| | 1 | 1 | 0 | 1 | fref (25.0-50 MHz) | fref · 2 (50-100 MHz) | fref ·2÷3 (16.67-33.3 MHz) |
| | 1 | 1 | 1 | 0 | fref (25.0-50 MHz) | fref (25.0-50 MHz) | fref (25.0-50 MHz) |
| | 1 | 1 | 1 | 1 | fref (25.0-50 MHz) | fref (25.0-50 MHz) | fref ·2÷3 (16.67-33.3 MHz) |

a. fref is the input clock reference frequency (CCLK or PCLK)

**Table 11. MPC9331 Example Configurations** (External Feedback and PWR_DN = 0)

| PLL Feedback | fref[a] [MHz] | FSELA | FSELB | FSELC | QA[0:1]:fref ratio | QB[0:1]:fref ratio | QC[0:1]:fref ratio |
|---|---|---|---|---|---|---|---|
| VCO ÷ 2[b] | 100 - 200 | 0 | 0 | 0 | fref (100-200 MHz) | fref (100-200 MHz) | fref ÷ 2 (50-100 MHz) |
| | | 0 | 0 | 1 | fref (100-200 MHz) | fref (100-200 MHz) | fref ÷ 3 (33.3-66.6 MHz) |
| | | 0 | 1 | 0 | fref (100-200 MHz) | fref ÷ 2 (50-100 MHz) | fref ÷ 2 (50-100 MHz) |
| | | 0 | 1 | 1 | fref (100-200 MHz) | fref ÷ 2 (50-100 MHz) | fref ÷ 3 (33.3-66.6 MHz) |
| VCO ÷ 4[c] | 50 - 100 | 1 | 0 | 0 | fref (50-100 MHz) | fref ·2 (100-200 MHz) | fref (50-100 MHz) |
| | | 1 | 0 | 1 | fref (50-100 MHz) | fref ·2 (100-200 MHz) | fref ·2÷3 (33.3-66.6 MHz) |
| | | 1 | 1 | 0 | fref (50-100 MHz) | fref (100-200 MHz) | fref (50-100 MHz) |
| | | 1 | 1 | 1 | fref (50-100 MHz) | fref (100-200 MHz) | fref ·2 ÷ 3 (33.3-66.6 MHz) |
| VCO ÷ 6[d] | 33.3-66.67 | 0 | 0 | 0 | fref ·3 (100-200 MHz) | fref ·3 (100-200 MHz) | fref (33.3-66.6 MHz) |
| | | 0 | 1 | 0 | fref ·3 (100-200 MHz) | fref ·3 ÷ 2 (50-100 MHz) | fref (33.3-66.6 MHz) |
| | | 1 | 0 | 0 | fref ·3 ÷ 2 (50-100 MHz) | fref ·3 (100-200 MHz) | fref (33.3-66.6 MHz) |
| | | 1 | 1 | 0 | fref ·3 ÷ 2 (50-100 MHz) | fref ·3 ÷ 2 (50-100 MHz) | fref (33.3-66.6 MHz) |

a. fref is the input clock reference frequency (CCLK or PCLK)
b. QAx connected to FB_IN and FSELA = 0, PWR_DN = 0
c. QAx connected to FB_IN and FSELA = 1, PWR_DN = 0
d. QCx connected to FB_IN and FSELC = 1, PWR_DN = 0

**Table 12. MPC9331 Example Configurations** (External Feedback and PWR_DN = 1)

| PLL Feedback | fref[a] [MHz] | FSELA | FSELB | FSELC | QA[0:1]:fref ratio | QB[0:1]:fref ratio | QC[0:1]:fref ratio |
|---|---|---|---|---|---|---|---|
| VCO ÷ 8[b] | 25.0 - 50.0 | 1 | 0 | 0 | fref (25-50 MHz) | fref ·2 (50-100 MHz) | fref (2.25-50 MHz) |
| | | 1 | 0 | 1 | fref (25-50 MHz) | fref ·2 (50-100 MHz) | fref ·2÷3 (16.6-33.3 MHz) |
| | | 1 | 1 | 0 | fref (25-50 MHz) | fref (25-50 MHz) | fref (25-50 MHz) |
| | | 1 | 1 | 1 | fref (25-50 MHz) | fref (25-50 MHz) | fref ·2÷3 (16.6-33.3 MHz) |
| VCO ÷ 12[c] | 16.67 - 33.3 | 0 | 0 | 1 | fref ·3 (50-100 MHz) | fref ·3 (50-100 MHz) | fref (16.67-33.3 MHz) |
| | | 0 | 1 | 1 | fref ·3 (50-100 MHz) | fref ·3 ÷ 2 (25-50 MHz) | fref (16.67-33.3 MHz) |
| | | 1 | 0 | 1 | fref ·3 ÷ 2 (25-50 MHz) | fref ·3 (50-100 MHz) | fref (16.67-33.3 MHz) |
| | | 1 | 1 | 1 | fref ·3 ÷ 2 (25-50 MHz) | fref ·3 ÷ 2 (25-50 MHz) | fref (16.67-33.3 MHz) |

a. fref is the input clock reference frequency (CCLK or PCLK)
b. QAx connected to FB_IN and FSELA = 1, PWR_DN = 1
c. QCx connected to FB_IN and FSELC = 1, PWR_DN = 1

2

## APPLICATIONS INFORMATION

### Power Supply Filtering

The MPC9331 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the VCC_PLL power supply impacts the device characteristics, for instance I/O jitter. The MPC9331 provides separate power supplies for the output buffers ($V_{CC}$) and the phase-locked loop (VCC_PLL) of the device.The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the VCC_PLL pin for the MPC9331. Figure 4 illustrates a typical power supply filter scheme. The MPC9331 frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor $R_F$. From the data sheet the $I_{CCA}$ current (the current sourced through the VCC_PLL pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V ($V_{CC}$ = 3.3V or $V_{CC}$ = 2.5V) must be maintained on the VCC_PLL pin. The resistor $R_F$ shown in Figure 3 must have a resistance of 270Ω ($V_{CC}$ = 3.3V) or 9-10Ω ($V_{CC}$ = 2.5V) to meet the voltage drop criteria.

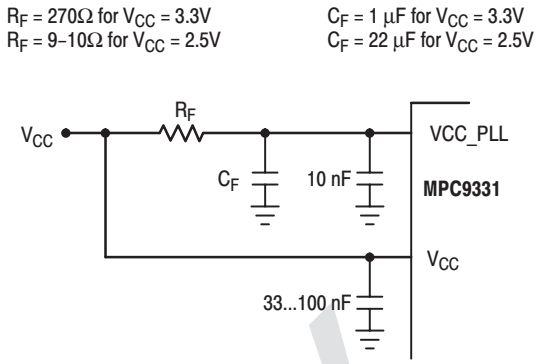



**Figure 3. $V_{CC\_PLL}$ Power Supply Filter**

The minimum values for RF and the filter capacitor $C_F$ are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9331 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

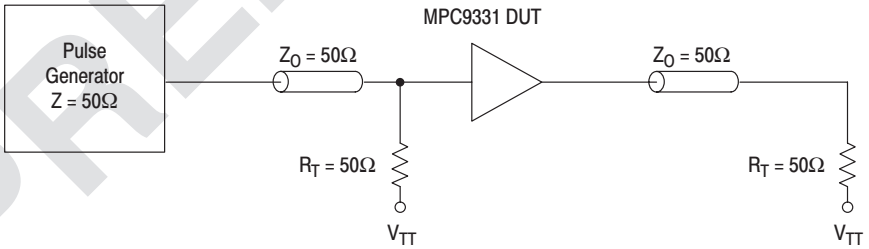
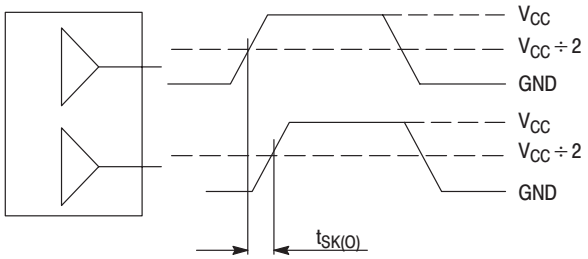



**Figure 4. CCLK MPC9331 AC test reference for $V_{cc}$ = 3.3V and $V_{cc}$ = 2.5V**




The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 5. Output–to–output Skew $t_{SK(O)}$**

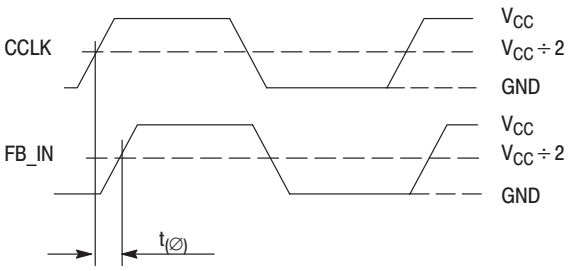
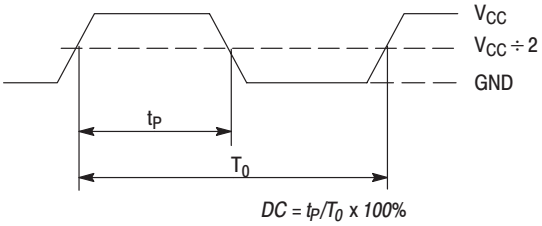
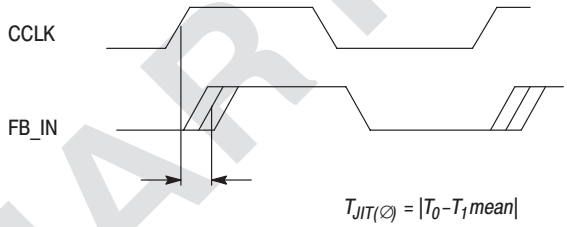



**Figure 6. Propagation delay ($t_{(\varnothing)}$, static phase offset) test reference**



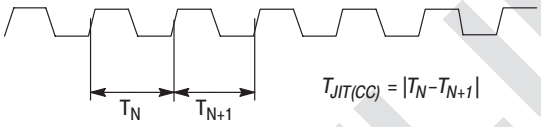

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 7. Output Duty Cycle (DC)**



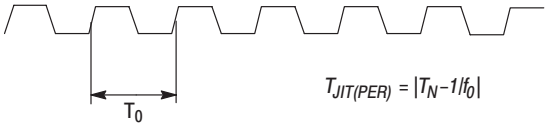

The deviation in $t_0$ for a controlled edge with respect to a $t_0$ mean in a random sample of cycles

**Figure 8. I/O Jitter**




The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

**Figure 9. Cycle–to–cycle Jitter**




The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

**Figure 10. Period Jitter**

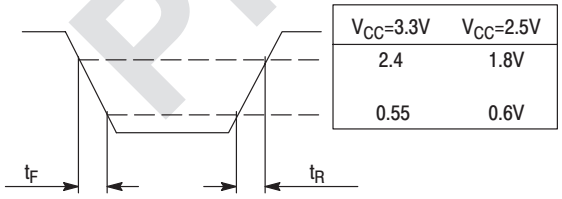



**Figure 11. Output Transition Time Test Reference**

**Order Number: MPC9350/D**
**Rev 2, 08/2001**

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*Product Preview*

# Low Voltage PLL Clock Driver

The MPC9350 is a 2.5V and 3.3V compatible, PLL based clock generator targeted for high performance clock distribution systems. With output frequencies of up to 200 MHz and maximum output skews of 200 ps the MPC9350 is ideal for the most demanding clock tree designs. The device offers 9 low skew clock outputs, each is configurable to support the clocking needs of the various high-performance microprocessors including the PowerQuicc II integrated communication microprocessor. The extended temperature range of the MPC9350 supports telecommunication and networking requirements. The devices employs a fully differential PLL design to minimize cycle-to-cycle and long-term jitter.

**Features**

- 9 outputs LVCMOS PLL clock generator
- 25 – 200 MHz output frequency range
- 2.5V and 3.3V compatible
- Compatible to various microprocessor such as PowerQuicc II
- Supports networking, telecommunications and computer applications
- Fully integrated PLL
- Configurable outputs: divide-by-2, 4 and 8 of VCO frequency
- Selectable output to input frequency ratio of 8:1, 4:1, 2:1 or 1:1
- Oscillator or crystal reference inputs
- Internal PLL feedback
- Output disable
- PLL enable/disable
- Low skew characteristics: maximum 200 ps output-to-output
- Cycle-to-cycle jitter max. ±50 ps
- 32 lead LQFP package
- Temperature range –40°C to +85°C

**MPC9350**

**LOW VOLTAGE 2.5V AND 3.3V PLL CLOCK GENERATOR**

**FA SUFFIX**
LQFP PACKAGE
CASE 873A–02



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.
**Rev 2**

**Functional Description**

The MPC9350 generates high frequency clock signals and provides nine exact frequency-multiplied copies of the reference clock signal. The internal PLL allows the MPC9350 to operate in frequency locked condition and to multiply the input reference clock. The reference clock frequency and the divider in the internal feedback path determine the VCO frequency. Two selectable PLL feedback frequency ratios are available on the MPC9350 to provide input frequency range flexibility. The FBSEL pin selects between divide-by-16 or divide-by-32 of the VCO frequency for PLL feedback. This feedback divider must be selected to match the VCO frequency range. With the available feedback output dividers the internal VCO of the MPC9350 is running at either 16x or 32x of the reference clock frequency. The frequency of the QA, QB, QC and QD outputs is either one half, one fourth or one eighth of the selected VCO frequency and can be configured for each output bank using the FSELA, FSELB, FSELC and FSELD pins, respectively. The available output to input frequency ratios are 16:1, 8:1, 4:1 and 2:1. The REF_SEL pin selects the crystal oscillator inputs or the LVCMOS compatible reference input (TCLK). TCLK also provides an external test clock in static test mode when the PLL enable pin (PLL_EN) is pulled to logic low state. In test mode, the selected input reference clock is routed directly to the output dividers without using the PLL. The test mode is intended for system diagnostics, test and debug purpose. This test mode is fully static and the minimum clock frequency specification does not apply. The outputs can be disabled by deasserting the $\overline{OE}$ pin (logic high state). In PLL mode, deasserting $\overline{OE}$ maintains PLL lock due to the internal feedback path. The MPC9350 is fully 2.5V and 3.3V compatible and requires no external loop filter components. The on-chip crystal oscillator requires no external components beyond a series resonant crystal. All inputs except the crystal oscillator interface accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9350 outputs can drive one or two traces giving the devices an effective fanout of 1:18. The device is packaged in a 7x7 $mm^2$ 32-lead LQFP package.

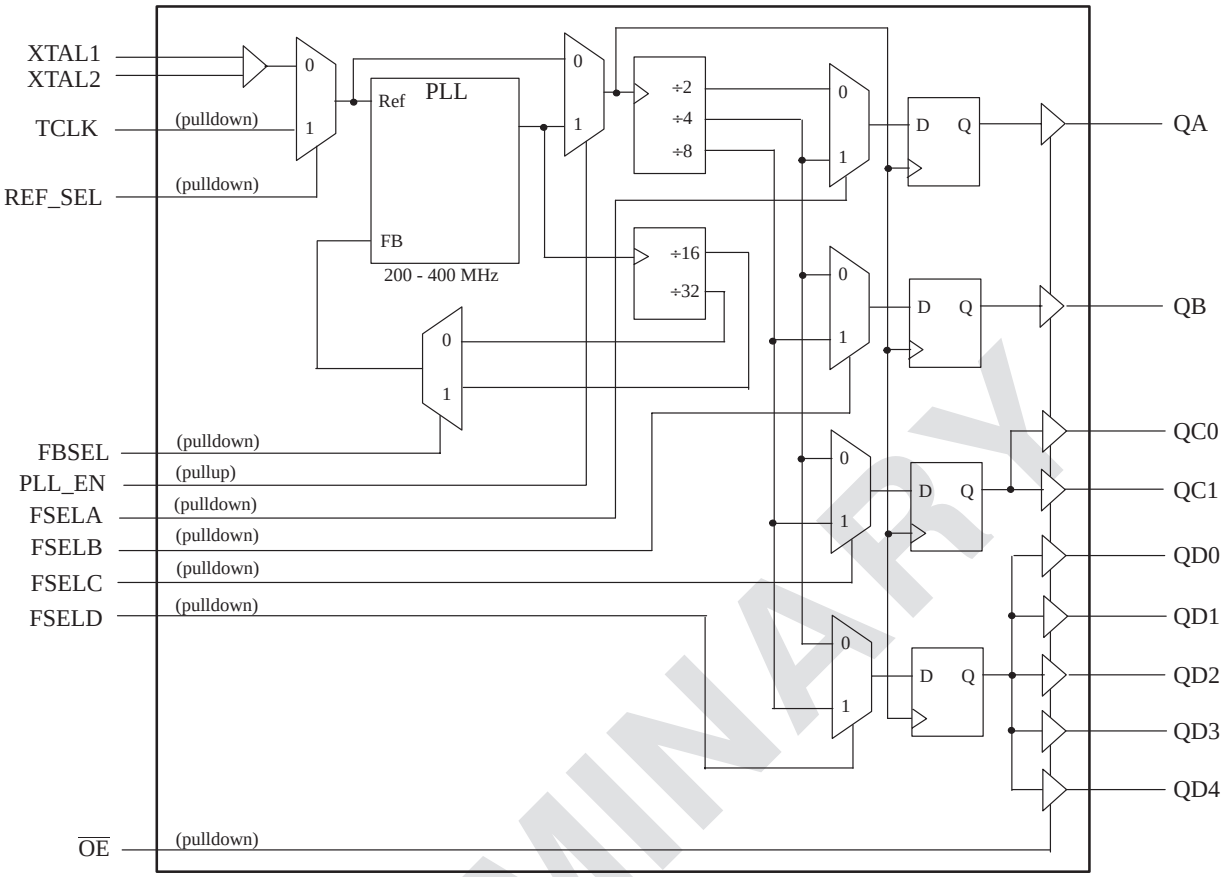



**Figure 1. MPC9350 Logic Diagram**

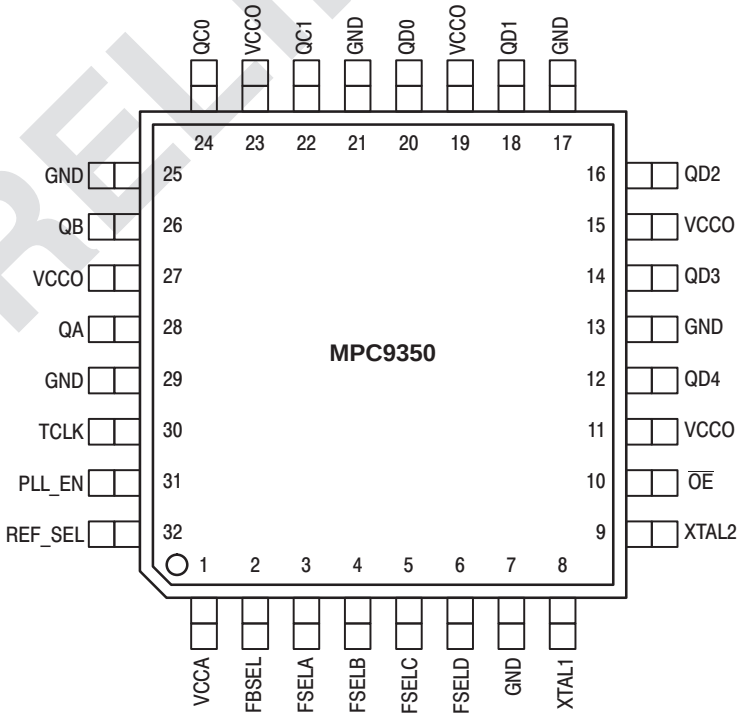



**Figure 2. Pinout: 32–Lead Package Pinout** (Top View)

## PIN CONFIGURATION

| Pin | I/O | Type | Function |
|---|---|---|---|
| XTAL1, XTAL2 | Input | Analog | Crystal oscillator terminals |
| TCLK | Input | LVCMOS | Single ended reference clock signal or test clock |
| FBSEL | Input | LVCMOS | Selects feedback divider ratio |
| REF_SEL | Input | LVCMOS | Selects input reference source |
| FSELA | Input | LVCMOS | Output A divider selection |
| FSELB | Input | LVCMOS | Output B divider selection |
| FSELC | Input | LVCMOS | Outputs C divider selection |
| FSELD | Input | LVCMOS | Outputs D divider selection |
| $\overline{OE}$ | Input | LVCMOS | Output enable/disable |
| QA | Output | LVCMOS | Bank A clock output |
| QB | Output | LVCMOS | Bank B clock output |
| QC0, QC1 | Output | LVCMOS | Bank C clock outputs |
| QD0 - QD4 | Output | LVCMOS | Bank D clock outputs |
| GND | Supply | Ground | Negative power supply |
| VCCA | Supply | VCC | Positive power supply for the PLL |
| VCC | Supply | VCC | Positive power supply for I/O and core |

## FUNCTION TABLE

| Control | Default | 0 | 1 |
|---|---|---|---|
| REF_SEL | 0 | Selects XTAL | Selects TCLK |
| PLL_EN | 1 | Test mode with PLL disabled. The input clock is directly routed to the output dividers | PLL enabled. The VCO output is routed to the output dividers |
| FBSEL | 0 | Selects feedback divider ÷ 32<br>VCO = 32 * Input reference clock | Selects feedback divider ÷ 16<br>VCO = 16 * Input reference clock |
| $\overline{OE}$ | 0 | Outputs enabled | Outputs disabled |
| FSELA | 0 | QA = VCO ÷ 2 | QA = VCO ÷ 4 |
| FSELB | 0 | QB = VCO ÷ 4 | QB = VCO ÷ 8 |
| FSELC | 0 | QC = VCO ÷ 4 | QC = VCO ÷ 8 |
| FSELD | 0 | QD = VCO ÷ 4 | QD = VCO ÷ 8 |

## ABSOLUTE MAXIMUM RATINGS[a]

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 4.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -40 | 125 | °C | |

a. Absolute maximum continuos ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

**DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40° to 85°C)

| Sym-bol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | -0.3 | | 0.8 | V | LVCMOS |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$=-24 mA[1.] |
| $V_{OL}$ | Output Low Voltage | | | 0.55<br>0.30 | V<br>V | $I_{OL}$= 24 mA<br>$I_{OL}$= 12 mA |
| $I_{IN}$ | Input Current | | | | µA | |
| $Z_{OUT}$ | Output impedance | | 14 - 17 | | Ω | |
| $C_{IN}$ | Input capacitance | | 4.0 | | pF | |
| $C_{PD}$ | Power Dissipation Capacitance | | 10 | | pF | Per Output |
| $I_{CCA}$ | Maximum PLL Supply Current | | | 10 | mA | $V_{CCA}$ Pin |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | | mA | All $V_{CC}$ Pins |
| $V_{TT}$ | Output termination voltage | | $V_{CC}$÷2 | | V | |

1. The MPC9350 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

**AC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40° to 85°C)[a,b]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency<br>÷ 8 feedback<br>÷ 16 feedback<br>Static Test Mode | <br>12.5<br>6.25<br>0 | | <br>25<br>12.5<br>300 | <br>MHz<br>MHz<br>MHz | <br>FBSEL = 1<br>FBSEL = 0<br>PLL_EN = 0 |
| $f_{XTAL}$ | Crystal Oscillator Frequency | 10 | | 25 | MHz | XTAL inputs |
| $f_{VCO}$ | VCO Frequency[b] | 200 | | 400 | MHz | PLL_EN = 1 |
| $f_{MAX}$ | Maximum Output Frequency<br>÷ 2 output<br>÷ 4 output<br>÷ 8 output | <br>100<br>50<br>25 | | <br>200<br>100<br>50 | <br>MHz<br>MHz<br>MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | 25 | | 75 | % | |
| tr, tf | TLCK Input Rise/Fall Time | | | 3.0 | ns | 0.8 to 2.0V |
| $t_{sk(o)}$ | Output-to-output Skew<br>Single Frequency<br>Multiple Frequencies | | | <br>150<br>200 | <br>ps<br>ps | |
| $t_{PW}$ | Output High Pulse Width | T÷2 - 200 | T | T÷2 + 200 | ps | T=Clock period |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.1 | | 1.0 | ns | 0.55 to 2.4V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | ns | |
| BW | PLL closed loop bandwidth<br>÷ 16 feedback<br>÷ 32 feedback | | | | <br>kHz<br>kHz | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter ÷ 16 feedback<br>÷ 32 feedback | | | | ps<br>ps | RMS value<br>RMS value |
| $t_{JIT(PER)}$ | Period Jitter ÷ 16 feedback<br>÷ 32 feedback | | | | ps<br>ps | RMS value<br>RMS value |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 1 | ms | |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$

b. AC characteristics pending characterization

**DC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40° to 85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | -0.3 | | 0.7 | V | LVCMOS |
| $V_{PP}$ | Peak-to-peak input voltage PCLK, $\overline{PCLK}$ | 500 | | 1000 | mV | LVPECL |
| $V_{CMR}$[a] | Common Mode Range PCLK, $\overline{PCLK}$ | $V_{CC}$-1.4 | | $V_{CC}$-0.6 | V | LVPECL |
| $V_{OH}$ | Output High Voltage | 1.8 | | | V | $I_{OH}$=-15 mA[b] |
| $V_{OL}$ | Output Low Voltage | | | 0.6 | V | $I_{OL}$= 15 mA |
| $Z_{OUT}$ | Output impedance | | 17 - 20 | | Ω | |
| $I_{IN}$ | Input Current | | | | µA | |
| $C_{IN}$ | Input capacitance | | | | pF | |
| $C_{PD}$ | Power Dissipation Capacitance | | 10 | | pF | Per Output |
| $I_{CCA}$ | Maximum PLL Supply Current | | | 10 | mA | $V_{CCA}$ Pin |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | | mA | All $V_{CC}$ Pins |
| $V_{TT}$ | Output termination voltage | | $V_{CC}$÷2 | | V | |

a. $V_{CMR}$ is the difference from $V_{CC}$ and the crosstalk of the differential input signal. Normal operation is obtained when the “high” input is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ specification.

b. The MPC9350 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.

**AC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40° to 85°C)[a,b]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency<br>÷ 16 feedback<br>÷ 32 feedback<br>Static test mode | <br>12.5<br>6.25<br>0 | | <br>25<br>12.5<br>300 | <br>MHz<br>MHz<br>MHz | <br>FBSEL = 1, PLL_EN = 1<br>FBSEL = 0, PLL_EN = 1<br>PLL_EN = 0 |
| $f_{XTAL}$ | Crystal Oscillator Frquency | 10 | | 25 | MHz | XTAL inputs |
| $f_{VCO}$ | VCO Frequency[b] | 200 | | 400 | MHz | PLL_EN = 1 |
| $f_{MAX}$ | Maximum Output Frequency<br>÷ 2 output<br>÷ 4 output<br>÷ 8 output | <br>100<br>50<br>25 | | <br>200<br>100<br>50 | <br>MHz<br>MHz<br>MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | 25 | | 75 | % | |
| $t_r$, $t_f$ | TLCK Input Rise/Fall Time | | | 3.0 | ns | 0.7 to 1.7V |
| $t_{sk(o)}$ | Output-to-output Skew<br>Single Frequency<br>Multiple Frequencies | | | <br>200<br>250 | <br>ps<br>ps | |
| $t_{PW}$ | Output High Pulse Width | T÷2 - 200 | T | T÷2 + 200 | ps | T=Clock period |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.1 | | 1.0 | ns | 0.6 to 1.8V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | ns | |
| BW | PLL closed loop bandwidth<br>÷ 16 feedback<br>÷ 32 feedback | | | | <br>kHz<br>kHz | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter ÷ 16 feedback<br>÷ 32 feedback | | | | ps<br>ps | RMS value<br>RMS value |
| $t_{JIT(PER)}$ | Period Jitter ÷ 16 feedback<br>÷ 32 feedback | | | | ps<br>ps | RMS value<br>RMS value |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 1 | ms | |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$

b. AC characteristics pending characterization

## APPLICATIONS INFORMATION

**Programming the MPC9350**

The MPC9350 clock driver outputs can be configured into several divider modes, in addition the internal feedback of the device allows for flexibility in establishing two input to output frequency relationships. The output division settings establish the output frequency relationship. The output divider of the four output groups allows the user to configure the outputs into 1:1, 2:1, 4:1 and 4:2:1 frequency ratios. The use of even dividers ensure that the output duty cycle is always 50%. “Output Frequency Relationship FBSEL = 1, (VC0 = 32 * CLK)” and “Output Frequency Relationship FBSEL = 0, (VC0 = 16 * CLK)” illustrate the various output configurations. The tables describes the outputs using the input clock frequency CLK as a reference.

In addition, it must be ensured that the VCO will be stable given the frequency of the outputs desired. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL supports output frequencies from 25 MHz to 200 MHz while the VCO frequency range is specified from 200 MHz to 400 MHz and should not be exceeded for stable operation.



**Output Frequency Relationship[a] FBSEL = 1, (VC0 = 32 * CLK)**

| Inputs | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|
| FSELA | FSELB | FSELC | FSELD | QA | QB | QC0, QC1 | QD0-QD4 |
| 0 | 0 | 0 | 0 | 16 * CLK | 8 * CLK | 8 * CLK | 8 * CLK |
| 0 | 0 | 0 | 1 | 16 * CLK | 8 * CLK | 8 * CLK | 4 * CLK |
| 0 | 0 | 1 | 0 | 16 * CLK | 8 * CLK | 4 * CLK | 8 * CLK |
| 0 | 0 | 1 | 1 | 16 * CLK | 8 * CLK | 4 * CLK | 4 * CLK |
| 0 | 1 | 0 | 0 | 16 * CLK | 4 * CLK | 8 * CLK | 8 * CLK |
| 0 | 1 | 0 | 1 | 16 * CLK | 4 * CLK | 8 * CLK | 4 * CLK |
| 0 | 1 | 1 | 0 | 16 * CLK | 4 * CLK | 4 * CLK | 8 * CLK |
| 0 | 1 | 1 | 1 | 16 * CLK | 4 * CLK | 4 * CLK | 4 * CLK |
| 1 | 0 | 0 | 0 | 8 * CLK | 8 * CLK | 8 * CLK | 8 * CLK |
| 1 | 0 | 0 | 1 | 8 * CLK | 8 * CLK | 8 * CLK | 4 * CLK |
| 1 | 0 | 1 | 0 | 8 * CLK | 8 * CLK | 4 * CLK | 8 * CLK |
| 1 | 0 | 1 | 1 | 8 * CLK | 8 * CLK | 4 * CLK | 4 * CLK |
| 1 | 1 | 0 | 0 | 8 * CLK | 4 * CLK | 8 * CLK | 8 * CLK |
| 1 | 1 | 0 | 1 | 8 * CLK | 4 * CLK | 8 * CLK | 4 * CLK |
| 1 | 1 | 1 | 0 | 8 * CLK | 4 * CLK | 4 * CLK | 8 * CLK |
| 1 | 1 | 1 | 1 | 8 * CLK | 4 * CLK | 4 * CLK | 4 * CLK |

a. Output frequency relationship with respect to input reference frequency CLK. Consult the MPC9351 datasheet more input to output relationships in external feedback mode.

**Output Frequency Relationship[a] FBSEL = 0, (VC0 = 16 * CLK)**

| Inputs | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|
| FSELA | FSELB | FSELC | FSELD | QA | QB | QC0, QC1 | QD0-QD4 |
| 0 | 0 | 0 | 0 | 8 * CLK | 4 * CLK | 4 * CLK | 4 * CLK |
| 0 | 0 | 0 | 1 | 8 * CLK | 4 * CLK | 4 * CLK | 2 * CLK |
| 0 | 0 | 1 | 0 | 8 * CLK | 4 * CLK | 2 * CLK | 4 * CLK |
| 0 | 0 | 1 | 1 | 8 * CLK | 4 * CLK | 2 * CLK | 2 * CLK |
| 0 | 1 | 0 | 0 | 8 * CLK | 2 * CLK | 4 * CLK | 4 * CLK |
| 0 | 1 | 0 | 1 | 8 * CLK | 2 * CLK | 4 * CLK | 2 * CLK |
| 0 | 1 | 1 | 0 | 8 * CLK | 2 * CLK | 2 * CLK | 4 * CLK |
| 0 | 1 | 1 | 1 | 8 * CLK | 2 * CLK | 2 * CLK | 2 * CLK |
| 1 | 0 | 0 | 0 | 4 * CLK | 4 * CLK | 4 * CLK | 4 * CLK |
| 1 | 0 | 0 | 1 | 4 * CLK | 4 * CLK | 4 * CLK | 2 * CLK |
| 1 | 0 | 1 | 0 | 4 * CLK | 4 * CLK | 2 * CLK | 4 * CLK |
| 1 | 0 | 1 | 1 | 4 * CLK | 4 * CLK | 2 * CLK | 2 * CLK |
| 1 | 1 | 0 | 0 | 4 * CLK | 2 * CLK | 4 * CLK | 4 * CLK |
| 1 | 1 | 0 | 1 | 4 * CLK | 2 * CLK | 4 * CLK | 2 * CLK |
| 1 | 1 | 1 | 0 | 4 * CLK | 2 * CLK | 2 * CLK | 4 * CLK |
| 1 | 1 | 1 | 1 | 4 * CLK | 2 * CLK | 2 * CLK | 2 * CLK |

a. Output frequency relationship with respect to input reference frequency CLK. Consult the MPC9351datasheet for more input to output relationships in external feedback mode.

2

**Power Supply Filtering**

The MPC9350 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC9350 provides separate power supplies for the output buffers ($V_{CCO}$) and the phase-locked loop ($V_{CCA}$) of the device.

The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level ofisolation may be required. The simplest form of isolation is a power supply filter on the $V_{CCA}$ pin for the MPC9350. Figure 3illustrates a typical power supply filter scheme. The MPC9350 is most susceptible to noise with spectral content in the 10kHz to 5MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the $V_{CCA}$ pin of the MPC9350. From the data sheet the $I_{VCCA}$ current (the current sourced through the $V_{CCA}$ pin) is typically 10 mA (15 mA maximum), assuming that a minimum of 3.0V must be maintained on the $V_{CCA}$ pin. Very little DC voltage drop can be tolerated when a 3.3V $V_{CC}$ supply is used. The resistor shown in Figure 3 “Power Supply Filter” must have a resistance of 10-15 Ω to meet the voltage drop criteria for $V_{CC}$=3.3V. For $V_{CC}$=2.5V operation, $R_S$ must be selected to maintain the minimum $V_{CC}$ specification of 2.375V for the PLL supply pin for proper operation. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8-10 Ω resistor to avoid potential $V_{CC}$ drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

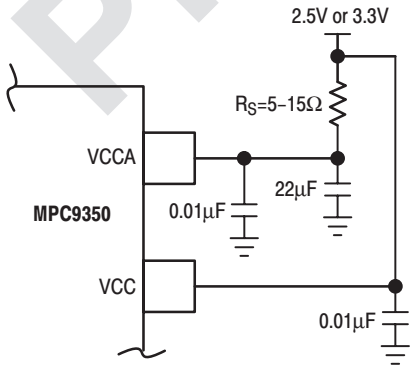



**Figure 3. Power Supply Filter**

Although the MPC9350 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Driving Transmission Lines**

The MPC9350 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 15Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}$÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9350 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9350 clock driver is effectively doubled due to its capability to drive multiple lines.

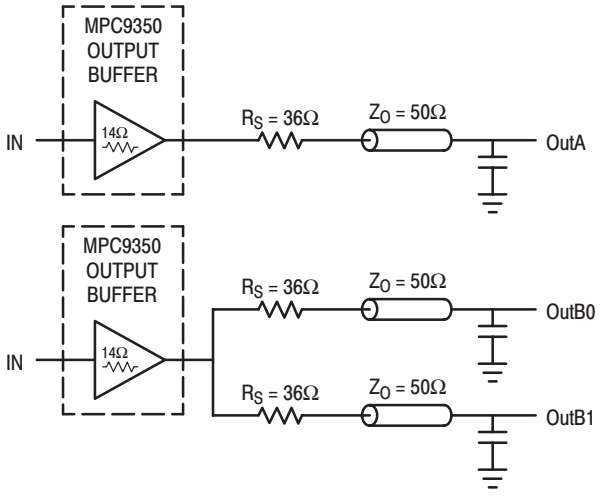



**Figure 4. Single versus Dual Transmission Lines**

The waveform plots in Figure 5 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9350 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9350. The output waveform in Figure 5 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$V_L = V_S ( Z_0 \div (R_S+R_0 +Z_0))$
$Z_0 = 50\Omega \parallel 50\Omega$
$R_S = 36\Omega \parallel 36\Omega$
$R_0 = 17\Omega$
$V_L = 3.0 ( 25 \div (18+17+25)$
$= 1.25V$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

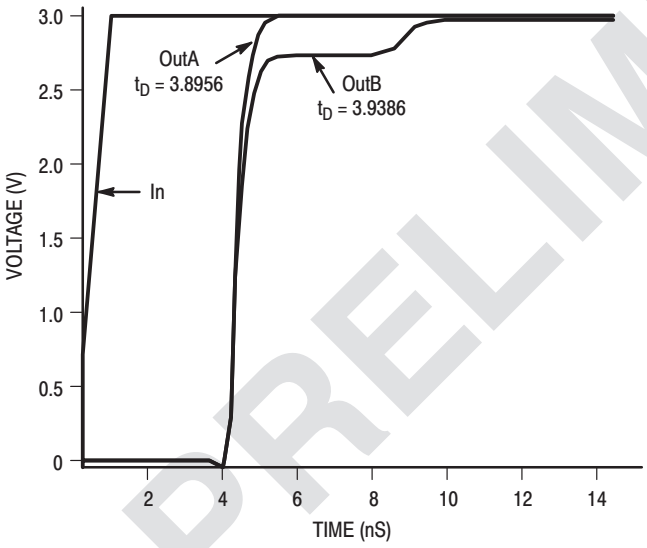
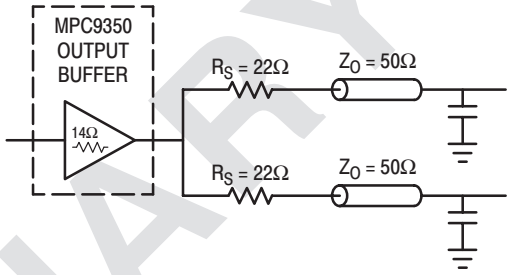



**Figure 5. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




$14\Omega + 22\Omega \parallel 22\Omega = 50\Omega \parallel 50\Omega$
$25\Omega = 25\Omega$

**Figure 6. Optimized Dual Line Termination**

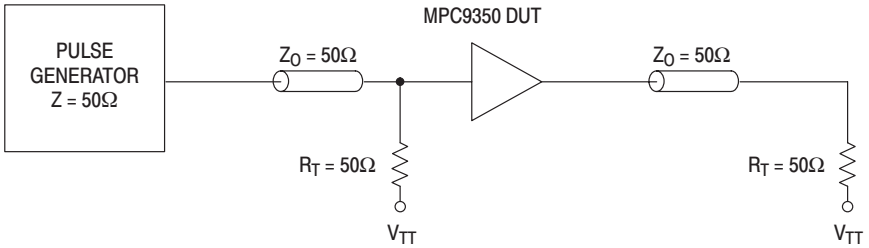
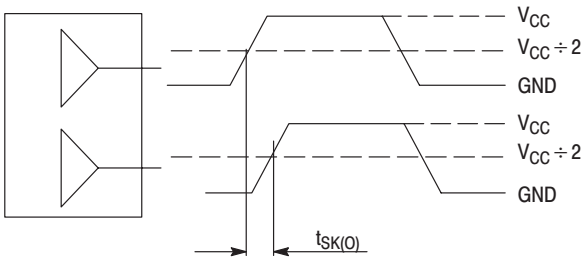


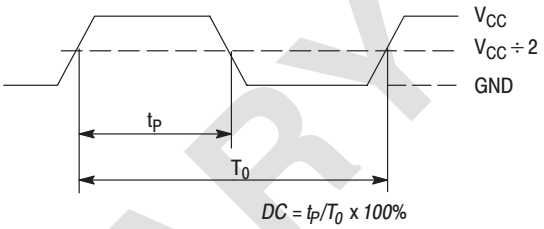

**Figure 7. TCLK MPC9350 AC test reference for $V_{cc}$ = 3.3V and $V_{cc}$ = 2.5V**

2



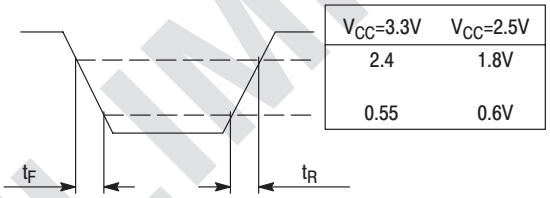

The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 8. Output–to–output Skew $t_{SK(O)}$**



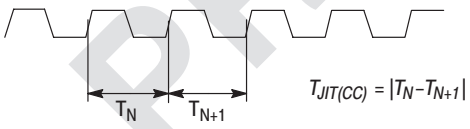

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 9. Output Duty Cycle (DC)**



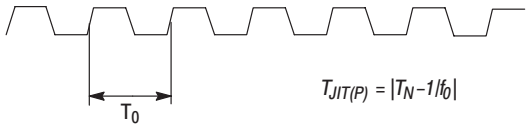

The time from the maximum low level voltage to minimum high level of a clock signal, expressed in ns

**Figure 10. Transition Time Test Reference**




The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

**Figure 11. Cycle–to–cycle Jitter**




The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

**Figure 12. Period Jitter**

# Low Voltage PLL Clock Driver

**MPC9351**

**LOW VOLTAGE 2.5V AND 3.3V PLL CLOCK GENERATOR**

**FA SUFFIX**
LQFP PACKAGE
CASE 873A–02

The MPC9351 is a 2.5 V and 3.3 V compatible, PLL based clock generator targeted for high performance clock distribution systems. With output frequencies of up to 200 MHz and a maximum output skew of 150 ps the MPC9351 is an ideal solution for the most demanding clock tree designs. The device offers 9 low skew clock outputs, each is configurable to support the clocking needs of the various high-performance microprocessors including the PowerQuicc II integrated communication microprocessor. The extended temperature range of the MPC9351 supports telecommunication and networking requirements.The devices employs a fully differential PLL design to minimize cycle-to-cycle and long-term jitter.

**Features**

- 9 outputs LVCMOS PLL clock generator
- 25 - 200 MHz output frequency range
- Fully integrated PLL
- 2.5V and 3.3V compatible
- Compatible to various microprocessors such as PowerQuicc II
- Supports networking, telecommunications and computer applications
- Configurable outputs: divide-by-2, 4 and 8 of VCO frequency
- LVPECL and LVCMOS compatible inputs
- External feedback enables zero-delay configurations
- Output enable/disable and static test mode (PLL enable/disable)
- Low skew characteristics: maximum 150 ps output-to-output
- Cycle-to-cycle jitter max. 22 ps RMS
- 32 lead LQFP package
- Ambient Temperature Range –40°C to +85°C

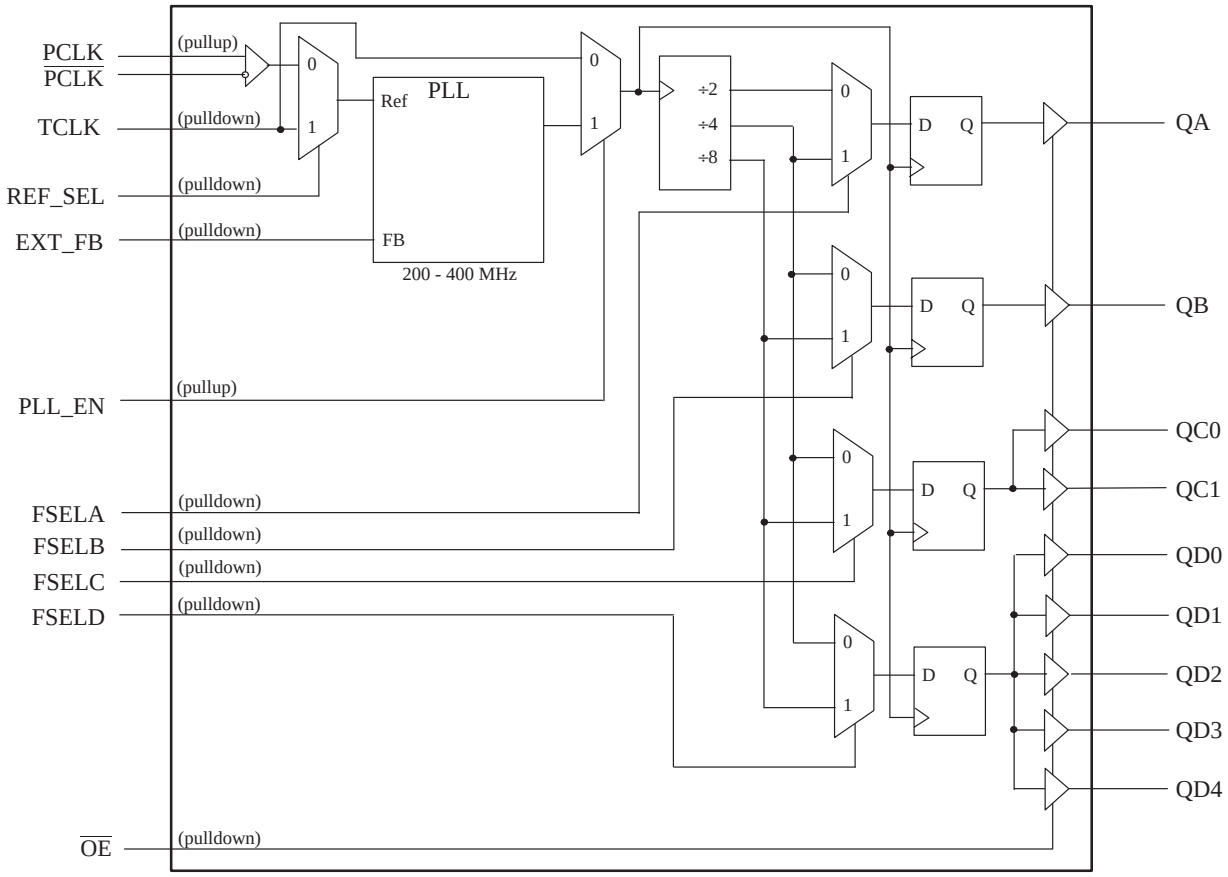
**Functional Description**

The MPC9351 utilizes PLL technology to frequency and phase lock its outputs onto an input reference clock. Normal operation of the MPC9351 requires a connection of one of the device outputs to the EXT_FB input to close the PLL feedback path. The reference clock frequency and the output divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. With available output dividers of divide-by-2, divide-by-4 and divide-by-8 the internal VCO of the MPC9351 is running at either 2x, 4x or 8x of the reference clock frequency. The frequency of the QA, QB, QC and QD outputs is either the one half, one fourth or one eighth of the selected VCO frequency and can be configured for each output bank using the FSELA, FSELB, FSELC and FSELD pins, respectively. The available output to input frequency ratios are 4:1, 2:1, 1:1, 1:2 and 1:4. The REF_SEL pin selects the differential LVPECL (PCLK and $\overline{\text{PCLK}}$) or the LVCMOS compatible reference input (TCLK). The MPC9351 also provides a static test mode when the PLL enable pin (PLL_EN) is pulled to logic low state. In test mode, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The test mode is intended for system diagnostics, test and debug purpose. This test mode is fully static and the minimum clock frequency specification does not apply. The outputs can be disabled by deasserting the $\overline{\text{OE}}$ pin (logic high state). In PLL mode, deasserting $\overline{\text{OE}}$ causes the PLL to loose lock due to no feedback signal presence at EXT_FB. Asserting OE will enable the outputs and close the phase locked loop, also enabling the PLL to recover to normal operation. The MPC9351 is fully 2.5V and 3.3V compatible and requires no external loop filter components. All inputs except PCLK and $\overline{\text{PCLK}}$ accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9351 outputs can drive one or two traces giving the devices an effective fanout of 1:18. The device is packaged in a 7x7 $mm^2$ 32-lead LQFP package.

**Application Information**

The fully integrated PLL of the MPC9351 allows the low skew outputs to lock onto a clock input and distribute it with essentially zero propagation delay to multiple components on the board. In zero-delay buffer mode, the PLL minimizes phase offset between the outputs and the reference signal.

**Rev 1**




The MPC9351 requires an external RC filter for the analog power supply pin VCCA. Please see application section for details.

**Figure 1. MPC9351 Logic Diagram**

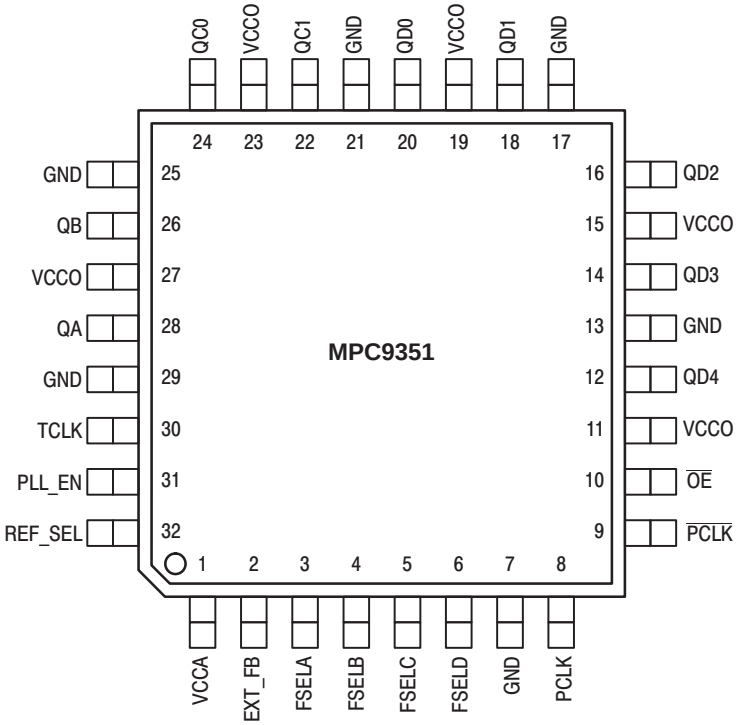



**Figure 2. Pinout: 32–Lead Package Pinout** (Top View)

### PIN CONFIGURATION

| Pin | I/O | Type | Function |
|---|---|---|---|
| PCLK, $\overline{PCLK}$ | Input | LVPECL | Differential clock reference<br>Low voltage positive ECL input |
| TCLK | Input | LVCMOS | Single ended reference clock signal or test clock |
| EXT_FB | Input | LVCMOS | Feedback signal input, connect to a QA, QB, QC, QD output |
| REF_SEL | Input | LVCMOS | Selects input reference clock |
| FSELA | Input | LVCMOS | Output A divider selection |
| FSELB | Input | LVCMOS | Output B divider selection |
| FSELC | Input | LVCMOS | Outputs C divider selection |
| FSELD | Input | LVCMOS | Outputs D divider selection |
| $\overline{OE}$ | Input | LVCMOS | Output enable/disable |
| QA | Output | LVCMOS | Bank A clock output |
| QB | Output | LVCMOS | Bank B clock output |
| QC0, QC1 | Output | LVCMOS | Bank C clock outputs |
| QD0 - QD4 | Output | LVCMOS | Bank D clock outputs |
| VCCA | Supply | VCC | Positive power supply for the PLL |
| VCC | Supply | VCC | Positive power supply for I/O and core |
| GND | Supply | Ground | Negative power supply |

### FUNCTION TABLE

| Control | Default | 0 | 1 |
|---|---|---|---|
| REF_SEL | 0 | Selects PCLK as reference clock | Selects TCLK as reference clock |
| PLL_EN | 1 | Test mode with PLL disabled. The input clock is directly routed to the output dividers | PLL enabled. The VCO output is routed to the output dividers |
| $\overline{OE}$ | 0 | Outputs enabled | Outputs disabled, PLL loop is open<br>VCO is forced to its minimum frequency |
| FSELA | 0 | QA = VCO ÷ 2 | QA = VCO ÷ 4 |
| FSELB | 0 | QB = VCO ÷ 4 | QB = VCO ÷ 8 |
| FSELC | 0 | QC = VCO ÷ 4 | QC = VCO ÷ 8 |
| FSELD | 0 | QD = VCO ÷ 4 | QD = VCO ÷ 8 |

### ABSOLUTE MAXIMUM RATINGS[a]

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 4.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage Temperature | -55 | 150 | °C | |

a. Absolute maximum continuos ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

### GENERAL SPECIFICATIONS

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output Termination Voltage | | $V_{CC}$ ÷ 2 | | V | |
| MM | ESD (Machine Model) | 200 | | | V | |
| HBM | ESD (Human Body Model) | 2000 | | | V | |
| LU | Latch–Up | 200 | | | mA | |
| $C_{PD}$ | Power Dissipation Capacitance | | 10 | | pF | Per output |
| $C_{IN}$ | | | 4.0 | | pF | Inputs |

**DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40° to 85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | | | 0.8 | V | LVCMOS |
| $V_{PP}$ | Peak-to-Peak Input Voltage PCLK, $\overline{PCLK}$ | 250 | | | mV | LVPECL |
| $V_{CMR}$[a] | Common Mode Range PCLK, $\overline{PCLK}$ | 1.0 | | $V_{CC}$-0.6 | V | LVPECL |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$=-24 mA[b] |
| $V_{OL}$ | Output Low Voltage | | | 0.55<br>0.30 | V<br>V | $I_{OL}$= 24 mA<br>$I_{OL}$= 12 mA |
| $Z_{OUT}$ | Output Impedance | | 14 - 17 | | Ω | |
| $I_{IN}$ | Input Leakage Current | | | ±150 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CCA}$ | Maximum PLL Supply Current | | 3.0 | 5.0 | mA | $V_{CCA}$ Pin |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (DC) specification.

b. The MPC9351 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

**AC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40° to 85°C)[a]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency ÷ 2 feedback<br>÷ 4 feedback<br>÷ 8 feedback<br>Static test mode | 100<br>50<br>25<br>0 | | 200<br>100<br>50<br>300 | MHz<br>MHz<br>MHz<br>MHz | PLL_EN = 1<br>PLL_EN = 1<br>PLL_EN = 1<br>PLL_EN = 0 |
| $f_{VCO}$ | VCO Frequency | 200 | | 400 | MHz | |
| $f_{MAX}$ | Maximum Output Frequency ÷ 2 output<br>÷ 4 output<br>÷ 8 output | 100<br>50<br>25 | | 200<br>100<br>50 | MHz<br>MHz<br>MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | 25 | | 75 | % | |
| $V_{PP}$ | Peak-to-Peak Input Voltage PCLK, $\overline{PCLK}$ | 500 | | 1000 | mV | LVPECL |
| $V_{CMR}$[b] | Common Mode Range PCLK, $\overline{PCLK}$ | 1.2 | | $V_{CC}$-0.9 | V | LVPECL |
| tr, tf | TCLK Input Rise/Fall Time | | | 1.0 | ns | 0.8 to 2.0V |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset)<br>TCLK to EXT_FB<br>PCLK to EXT_FB | <br>–50<br>+25 | | <br>+150<br>+325 | <br>ps<br>ps | <br>PLL locked<br>PLL locked |
| $t_{sk(o)}$ | Output-to-Output Skew | | | 150 | ps | |
| DC | Output Duty Cycle 100 – 200 MHz<br>50 – 100 MHz<br>25 – 50 MHz | 45<br>47.5<br>48.75 | 50<br>50<br>50 | 55<br>52.5<br>51.75 | %<br>%<br>% | |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.1 | | 1.0 | ns | 0.55 to 2.4V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | 10 | ns | |
| $t_{PZL, ZH}$ | Output Enable Time | | | 10 | ns | |
| BW | PLL closed loop bandwidth ÷ 2 feedback<br>÷ 4 feedback<br>÷ 8 feedback | | 9.0 – 20.0<br>3.0 – 9.5<br>1.2 – 2.1 | | MHz<br>MHz<br>MHz | –3 db point of<br>PLL transfer<br>characteristic |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter ÷ 4 feedback<br>Single Output Frequency Configuration | | 10 | 22 | ps | RMS value |
| $t_{JIT(PER)}$ | Period Jitter ÷ 4 feedback<br>Single Output Frequency Configuration | | 8.0 | 15 | ps | RMS value |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | | 4.0 – 17 | | ps | RMS value |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 1.0 | ms | |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$

b. $V_{CMR}$ (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ or $V_{PP}$ impacts static phase offset $t_{(\varnothing)}$.

**DC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40° to 85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | | | 0.7 | V | LVCMOS |
| $V_{PP}$ | Peak-to-Peak Input Voltage PCLK, $\overline{PCLK}$ | 250 | | | mV | LVPECL |
| $V_{CMR}$[a] | Common Mode Range PCLK, $\overline{PCLK}$ | 1.0 | | $V_{CC}$-0.6 | V | LVPECL |
| $V_{OH}$ | Output High Voltage | 1.8 | | | V | $I_{OH}$=-15 mA[b] |
| $V_{OL}$ | Output Low Voltage | | | 0.6 | V | $I_{OL}$= 15 mA |
| $Z_{OUT}$ | Output Impedance | | 17 - 20 | | Ω | |
| $I_{IN}$ | Input Leakage Current | | | ±150 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | |
| $C_{PD}$ | Power Dissipation Capacitance | | 10 | | pF | Per Output |
| $I_{CCA}$ | Maximum PLL Supply Current | | 3.0 | 5.0 | mA | $V_{CCA}$ Pin |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (DC) specification.

b. The MPC9351 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.

**AC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40° to 85°C)[a]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency ÷ 2 feedback<br>÷ 4 feedback<br>÷ 8 feedback | 100<br>50<br>25 | | 200<br>100<br>50 | MHz<br>MHz<br>MHz | |
| $f_{VCO}$ | VCO Frequency | 200 | | 400 | MHz | |
| $f_{MAX}$ | Maximum Output Frequency ÷ 2 output<br>÷ 4 output<br>÷ 8 output | 100<br>50<br>25 | | 200<br>100<br>50 | MHz<br>MHz<br>MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | 25 | | 75 | % | |
| $V_{PP}$ | Peak-to-Peak Input Voltage PCLK, $\overline{PCLK}$ | 500 | | 1000 | mV | LVPECL |
| $V_{CMR}$[b] | Common Mode Range PCLK, $\overline{PCLK}$ | 1.2 | | $V_{CC}$-0.6 | V | LVPECL |
| tr, tf | TCLK Input Rise/Fall Time | | | 1.0 | ns | 0.7 to 1.7V |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset)<br>TCLK to EXT_FB<br>PCLK to EXT_FB | <br>–100<br>0 | | <br>+100<br>+300 | <br>ps<br>ps | <br>PLL locked<br>PLL locked |
| $t_{sk(o)}$ | Output-to-Output Skew | | | 150 | ps | |
| DC | Output Duty Cycle 100 – 200 MHz<br>50 – 100 MHz<br>25 – 50 MHz | 45<br>47.5<br>48.75 | 50<br>50<br>50 | 55<br>52.5<br>51.75 | %<br>%<br>% | |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.1 | | 1.0 | ns | 0.6 to 1.8V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | 12 | ns | |
| $t_{PZL, ZH}$ | Output Enable Time | | | 12 | ns | |
| BW | PLL closed loop bandwidth ÷ 2 feedback<br>÷ 4 feedback<br>÷ 8 feedback | | 4.0 – 15.0<br>2.0 – 7.0<br>0.7 – 2.0 | | MHz<br>MHz<br>MHz | –3dB point of PLL transfer characteristic |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter ÷ 4 feedback<br>Single Output Frequency Configuration | | 10 | 22 | ps | RMS value |
| $t_{JIT(PER)}$ | Period Jitter ÷ 4 feedback<br>Single Output Frequency Configuration | | 8.0 | 15 | ps | RMS value |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | | 6.0 – 25 | | ps | RMS value |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 1.0 | ms | |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$

b. $V_{CMR}$ (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ or $V_{PP}$ impacts static phase offset $t_{(\varnothing)}$.

## APPLICATIONS INFORMATION

### Programming the MPC9351

The MPC9351 clock driver outputs can be configured into several divider modes, in addition the external feedback of the device allows for flexibility in establishing various input to output frequency relationships. The output divider of the four output groups allows the user to configure the outputs into 1:1, 2:1, 4:1 and 4:2:1 frequency ratios. The use of even dividers ensure that the output duty cycle is always 50%. “Output Frequency Relationship for an Example Configuration” illustrates the various output configurations, the table describes the outputs using the input clock frequency CLK as a reference.

The output division settings establish the output relationship, in addition, it must be ensured that the VCO will be stable given the frequency of the outputs desired. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL supports output frequencies from 25 MHz to 200 MHz while the VCO frequency range is specified from 200 MHz to 400 MHz and should not be exceeded for stable operation.

**Output Frequency Relationship[a] for an Example Configuration**

| Inputs | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|
| FSELA | FSELB | FSELC | FSELD | QA | QB | QC | QD |
| 0 | 0 | 0 | 0 | 2 * CLK | CLK | CLK | CLK |
| 0 | 0 | 0 | 1 | 2 * CLK | CLK | CLK | CLK ÷ 2 |
| 0 | 0 | 1 | 0 | 4 * CLK | 2 * CLK | CLK | 2* CLK |
| 0 | 0 | 1 | 1 | 4 * CLK | 2 * CLK | CLK | CLK |
| 0 | 1 | 0 | 0 | 2 * CLK | CLK ÷ 2 | CLK | CLK |
| 0 | 1 | 0 | 1 | 2 * CLK | CLK ÷ 2 | CLK | CLK ÷ 2 |
| 0 | 1 | 1 | 0 | 4 * CLK | CLK | CLK | 2 * CLK |
| 0 | 1 | 1 | 1 | 4 * CLK | CLK | CLK | CLK |
| 1 | 0 | 0 | 0 | CLK | CLK | CLK | CLK |
| 1 | 0 | 0 | 1 | CLK | CLK | CLK | CLK ÷ 2 |
| 1 | 0 | 1 | 0 | 2 * CLK | 2 * CLK | CLK | 2 * CLK |
| 1 | 0 | 1 | 1 | 2 * CLK | 2 * CLK | CLK | CLK |
| 1 | 1 | 0 | 0 | CLK | CLK ÷ 2 | CLK | CLK |
| 1 | 1 | 0 | 1 | CLK | CLK ÷ 2 | CLK | CLK ÷ 2 |
| 1 | 1 | 1 | 0 | 2 * CLK | CLK | CLK | 2 * CLK |
| 1 | 1 | 1 | 1 | 2 * CLK | CLK | CLK | CLK |

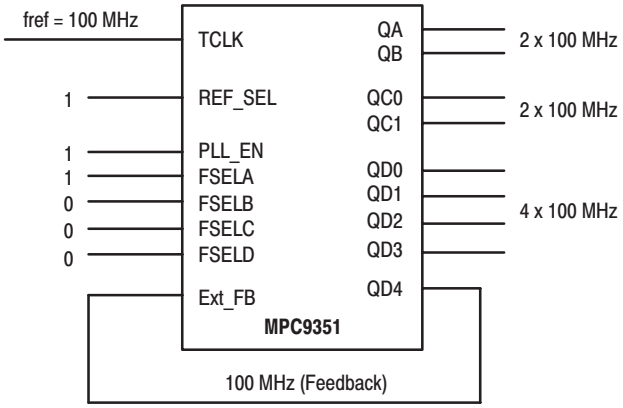
a. Output frequency relationship with respect to input reference frequency CLK. QC1 is connected to EXT_FB. More frequency ratios are available by the connection of QA to the feedback input (EXT_FB).

### Using the MPC9351 in zero–delay applications

Nested clock trees are typical applications for the MPC9351. For these applications the MPC9351 offers a differential LVPECL clock input pair as a PLL reference. This allows for the use of differential LVPECL primary clock distribution devices such as the Motorola MC100EP111 or MC10EP222, taking advantage of its superior low-skew performance. Clock trees using LVPECL for clock distribution and the MPC9351 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers.

The external feedback option of the MPC9351 PLL allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge and virtually eliminates the propagation delay through the device.

The remaining insertion delay (skew error) of the MPC9351 in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset (SPO or $t_{(\varnothing)}$), I/O jitter ($t_{JIT(\varnothing)}$, phase or long-term jitter), feedback path delay and the output-to-output skew ($t_{SK(O)}$ relative to the feedback output.




**MPC9351 zero–delay configuration (feedback of QD4)**

### Calculation of part-to-part skew

The MPC9351 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs (TCLK or PCLK) of two or more MPC9351 are connected together, the maxi-

mum overall timing uncertainty from the common TCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

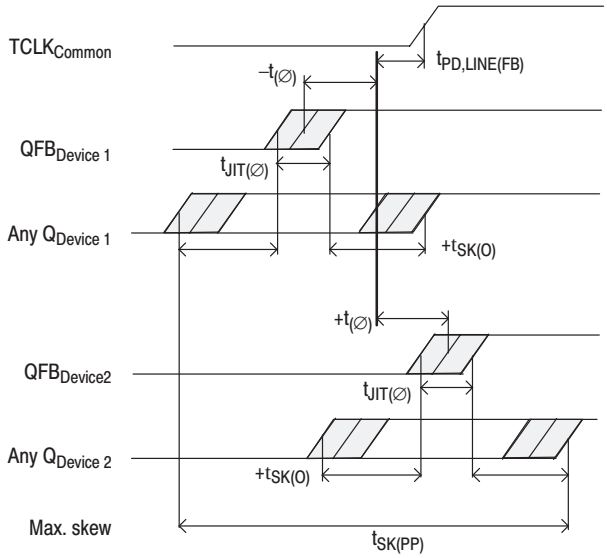



**Figure 3. MPC9351 max. device-to-device skew**

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

**Table 8: Confidence Facter CF**

| CF | Probability of clock edge within the distribution |
|---|---|
| ± 1σ | 0.68268948 |
| ± 2σ | 0.95449988 |
| ± 3σ | 0.99730007 |
| ± 4σ | 0.99993663 |
| ± 5σ | 0.99999943 |
| ± 6σ | 0.99999999 |

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of -251 ps to 351 ps relative to TCLK ($V_{CC}$=3.3V and $f_{VCO}$ = 400 MHz):

$$t_{SK(PP)} = [–50ps...150ps] + [–150ps...150ps] + [(17ps \cdot –3)...(17ps \cdot 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [–251ps...351ps] + t_{PD,\ LINE(FB)}$$

Above equation uses the maximum I/O jitter number shown in the AC characteristic table for $V_{CC}$=3.3V (17 ps RMS). I/O jitter is frequency dependant with a maximum at the lowest VCO frequency (200 MHz for the MPC9351). Applications using a higher VCO frequency exhibit less I/O jitter than the AC characteristic limit. The I/O jitter characteristics in Figure 4 and Figure 5 can be used to derive a smaller I/O jitter number at the specific VCO frequency, resulting in tighter timing limits in zero-delay mode and for part-to-part skew $t_{SK(PP)}$.

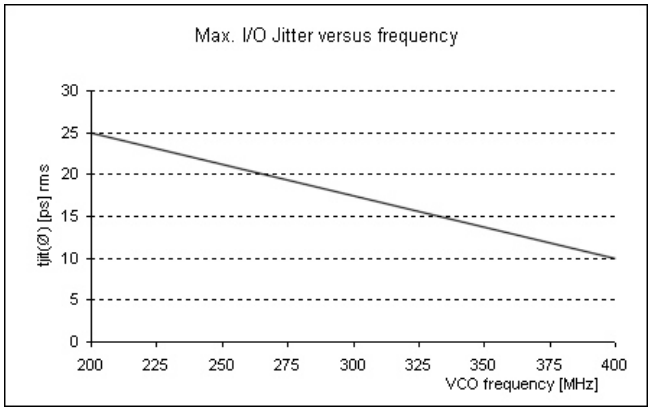



**Figure 4. Max. I/O Jitter (RMS) versus frequency for $V_{CC}$=2.5V**

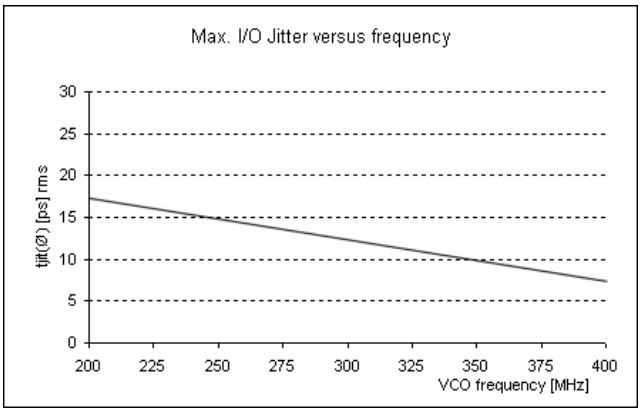



**Figure 5. Max. I/O Jitter (RMS) versus frequency for $V_{CC}$=3.3V**

**Power Supply Filtering**

The MPC9351 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Noise on the $V_{CCA}$ (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC9351 provides separate power supplies for the output buffers ($V_{CC}$) and the phase-locked loop ($V_{CCA}$) of the device.The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the $V_{CCA}$ pin for the MPC9351. Figure 6 illustrates a typical power supply filter scheme. The MPC9351 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor $R_F$. From the data sheet the $I_{CCA}$ current (the current sourced through the $V_{CCA}$ pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V ($V_{CC}$=3.3V or $V_{CC}$=2.5V) must be maintained on the $V_{CCA}$ pin. The resistor $R_F$ shown in Figure 6 "$V_{CCA}$ Power Supply Filter" must have a resistance of 270Ω ($V_{CC}$=3.3V) or 9-10Ω ($V_{CC}$=2.5V) to meet the voltage drop criteria.

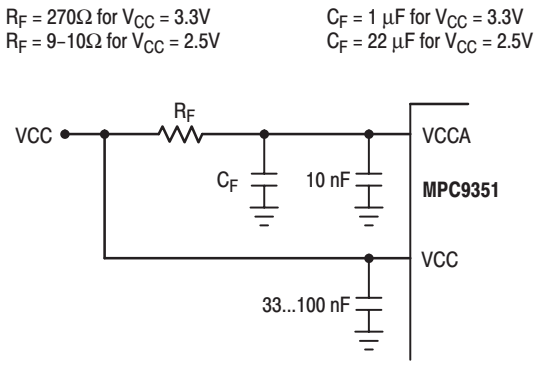



**Figure 6. $V_{CCA}$ Power Supply Filter**

The minimum values for $R_F$ and the and the filter capacitor $C_F$ are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 6 "$V_{CCA}$ Power Supply Filter", the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9351 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Driving Transmission Lines**

The MPC9351 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}$÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9351 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 7 "Single versus Dual Transmission Lines" illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9351 clock driver is effectively doubled due to its capability to drive multiple lines.

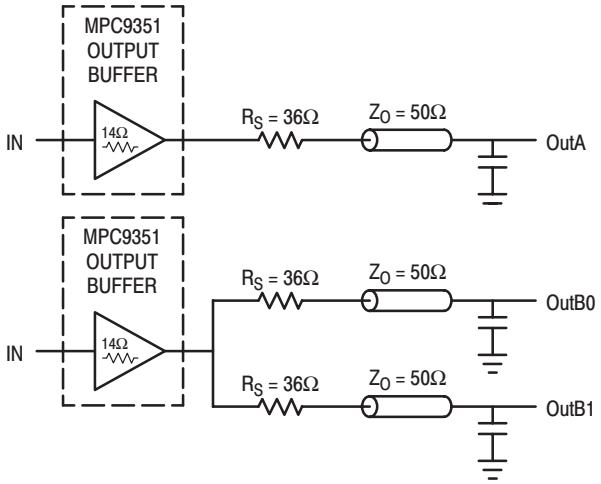



**Figure 7. Single versus Dual Transmission Lines**

The waveform plots in Figure 8 "Single versus Dual Line Termination Waveforms" show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9351 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9351. The output waveform in Figure 8 "Single versus Dual Line Termination Waveforms" shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S ( Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\Omega \,||\, 50\Omega$$
$$R_S = 36\Omega \,||\, 36\Omega$$
$$R_0 = 14\Omega$$
$$V_L = 3.0 ( 25 \div (18+17+25)$$
$$= 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

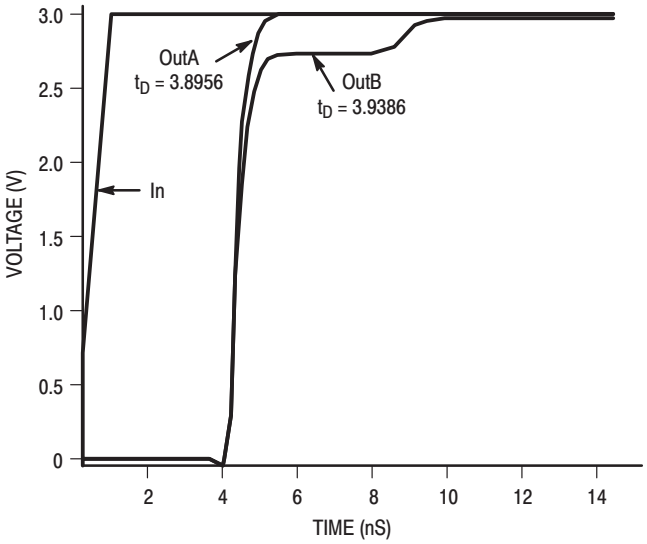
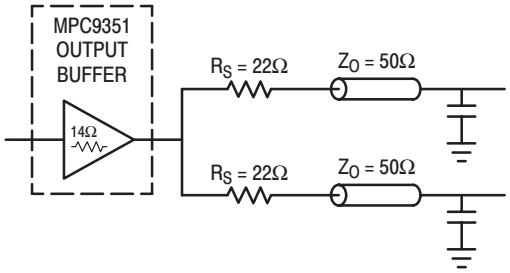



**Figure 8. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 9 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




14Ω + 22Ω || 22Ω = 50Ω || 50Ω
25Ω = 25Ω

**Figure 9. Optimized Dual Line Termination**

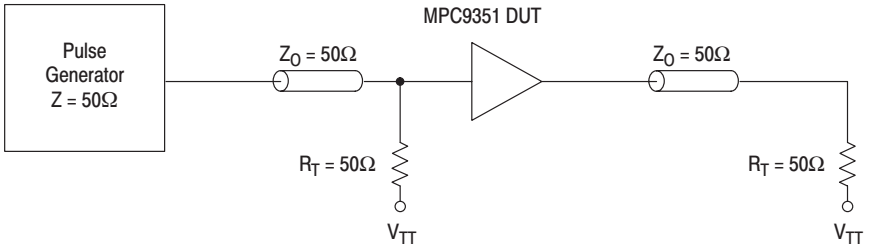



**Figure 10. TCLK MPC9351 AC test reference for $V_{cc}$ = 3.3V and $V_{cc}$ = 2.5V**

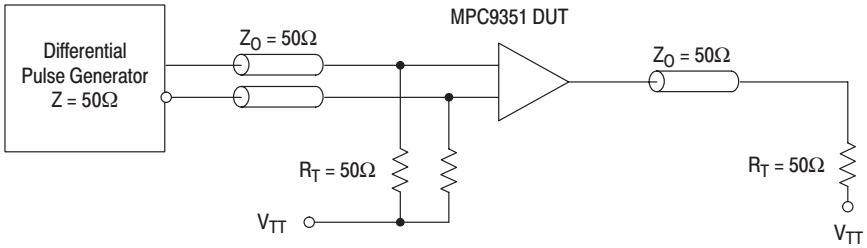



**Figure 11. PCLK MPC9351 AC test reference**

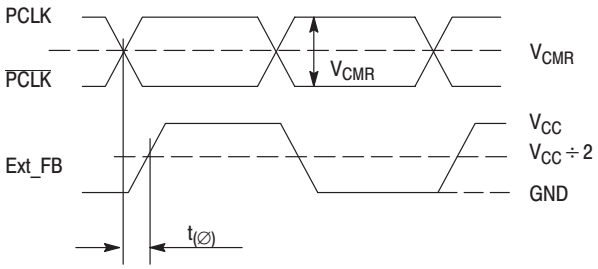



**Figure 12. Propagation delay ($t_{PD}$, static phase offset) test reference**

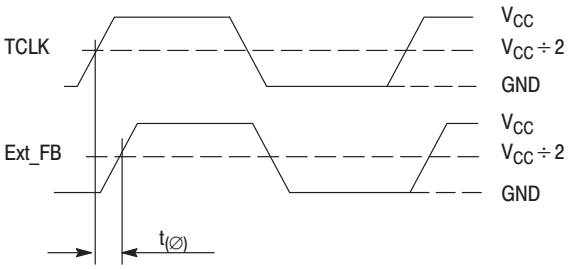
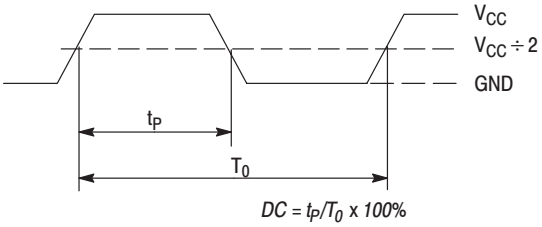
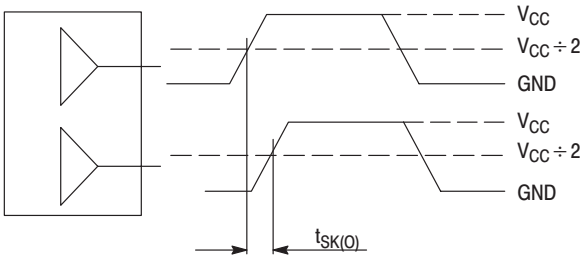



**Figure 13. Propagation delay ($t_{PD}$) test reference**



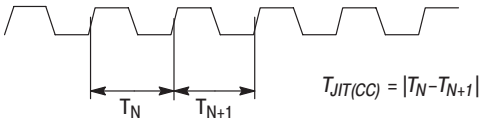

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 14. Output Duty Cycle (DC)**



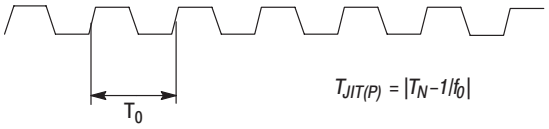

The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 15. Output–to–output Skew $t_{SK(O)}$**



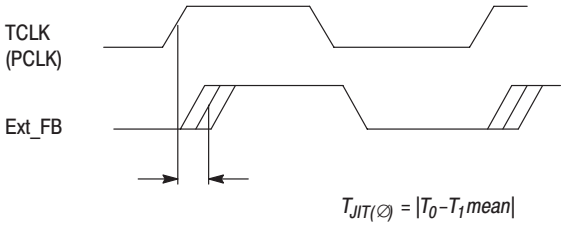

The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

**Figure 16. Cycle–to–cycle Jitter**




The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

**Figure 17. Period Jitter**




The deviation in $t_0$ for a controlled edge with respect to a $t_0$ mean in a random sample of cycles

**Figure 18. I/O Jitter**

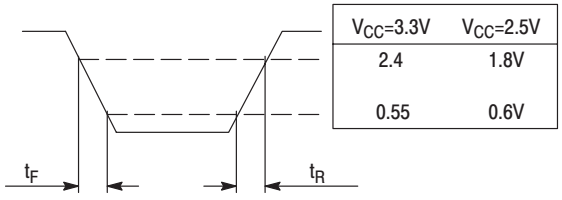



**Figure 19. Transition Time Test Reference**

*Product Preview*

# 3.3V/2.5V 1:11 LVCMOS Zero Delay Clock Generator

**MPC9352**

**LOW VOLTAGE 3.3V/2.5V LVCMOS 1:11 CLOCK GENERATOR**



**FA SUFFIX**
32 LEAD LQFP PACKAGE
CASE 873A

The MPC9352 is a 3.3V or 2.5V compatible, 1:11 PLL based clock generator targeted for high performance clock tree applications. With output frequencies up to 200 MHz and output skews lower than 150 ps[1] the device meets the needs of most demanding clock applications.

**Features**

- Configurable 11 outputs LVCMOS PLL clock generator
- Fully integrated PLL
- Wide range of output clock frequency of 16.67 MHz to 200 MHz
- Multiplication of the input reference clock frequency by 3, 2, 1, 3 ÷ 2, 2 ÷ 3, 1 ÷ 3 and 1 ÷ 2
- 2.5V and 3.3V LVCMOS compatible
- Maximum output skew of 150 ps[1]
- Supports zero–delay applications: maximum static phase offset window of ±100 ps[1]
- Designed for high–performance telecom, networking and computing applications
- 32 lead LQFP package
- Ambient Temperature Range –40°C to +85°C

**Functional Description**

The MPC9352 is a fully 3.3V or 2.5V compatible PLL clock generator and clock driver. The device has the capability to generate output clock signals of 16.67 to 200 MHz from external clock sources. The internal PLL optimized for its frequency range and does not require external look filter components. One output of the MPC9352 has to be connected to the PLL feedback input FB_IN to close the external PLL feedback path. The output divider of this output setting determines the PLL frequency multiplication factor. This multiplication factor, F_RANGE and the reference clock frequency must be selected to situate the VCO in its specified lock range. The frequency of the clock outputs can be configured individually for all three output banks by the FSELx pins supporting systems with different but phase-aligned clock frequencies.

The PLL of the MPC9352 minimizes the propagation delay and therefore supports zero-delay applications. All inputs and outputs are LVCMOS compatible. The outputs are optimized to drive parallel terminated 50Ω transmission lines. Alternatively, each output can drive up to two series terminated transmission lines giving the device an effective fanout of 22.

The device also supports output high-impedance disable and a PLL bypass mode for static system test and diagnosis. The MPC9352 is package in a 32 ld LQFP.



1. Design target, pending final characterization.



**Rev 0**

2

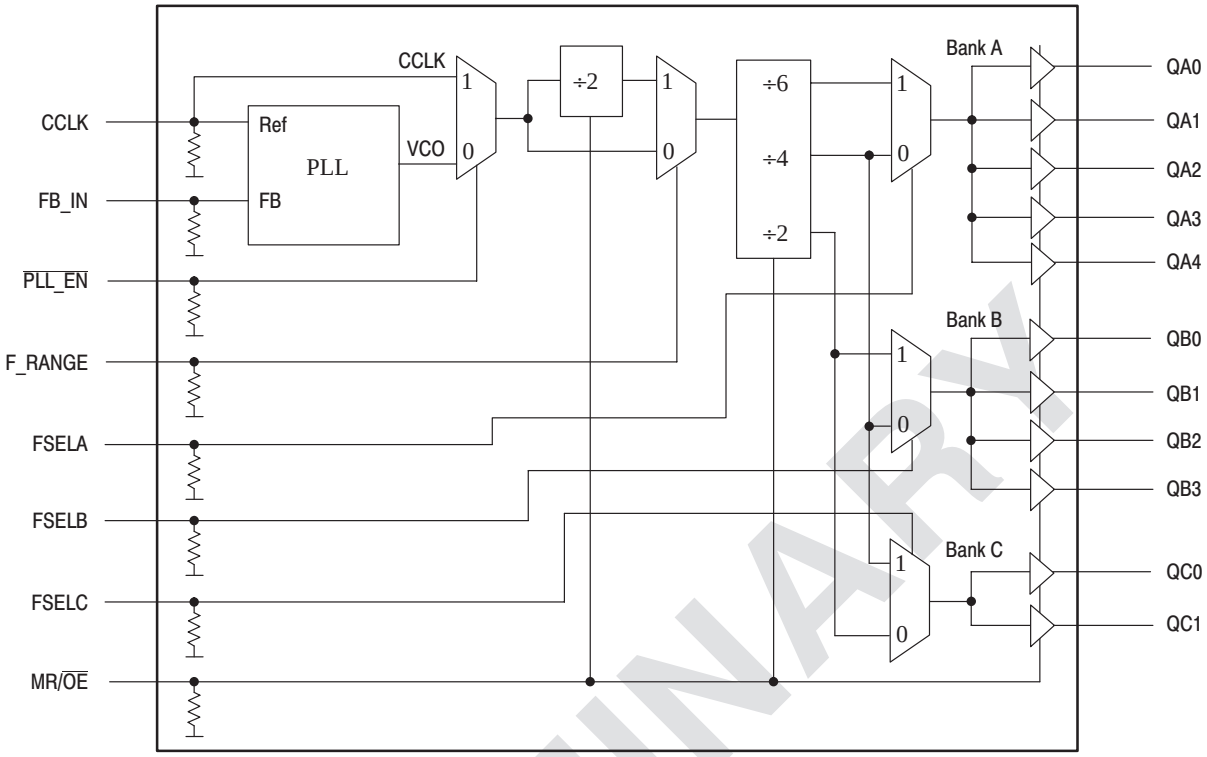
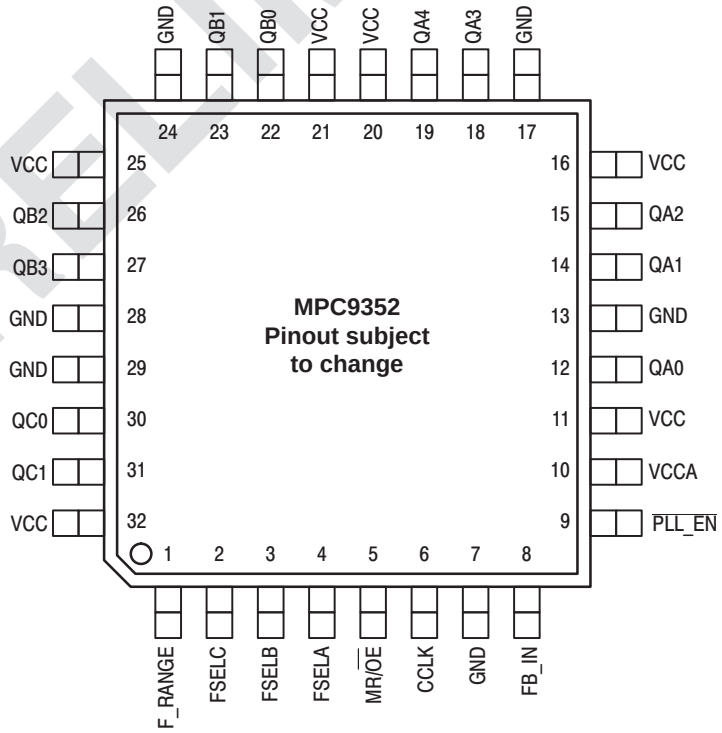



**Figure 1. MPC9352 Logic Diagram**




The MPC9352 requires an external RC filter for the analog power supply pin VCCA. Please see application section for details.

**Figure 2. MPC9352 32–Lead Package Pinout** (Top View)

**Table 1: PIN CONFIGURATION**

| Pin | I/O | Type | Function |
|---|---|---|---|
| CCLK | Input | LVCMOS | PLL reference clock signal |
| FB_IN | Input | LVCMOS | PLL feedback signal input, connect to an output |
| F_RANGE | Input | LVCMOS | PLL frequency range select |
| FSELA | Input | LVCMOS | Frequency divider select for bank A outputs |
| FSELB | Input | LVCMOS | Frequency divider select for bank B outputs |
| FSELC | Input | LVCMOS | Frequency divider select for bank C outputs |
| $\overline{\text{PLL\_EN}}$ | Input | LVCMOS | PLL enable/disable |
| MR/$\overline{\text{OE}}$ | Input | LVCMOS | Output enable/disable (high–impedance tristate) and device reset |
| QA0–4, QB0–3, QC0–1 | Output | LVCMOS | Clock outputs |
| GND | Supply | Ground | Negative power supply |
| VCCA | Supply | VCC | PLL positive power supply (analog power supply). The MPC9352 requires an external RC filter for the analog power supply pin $V_{CCA}$. Please see applications section for details. |
| VCC | Supply | VCC | Positive power supply for I/O and core |

**Table 2: FUNCTION TABLE**

| Control | Default | 0 | 1 |
|---|---|---|---|
| F_RANGE, FSELA, FSELB, and FSELC control the operating PLL frequency range and input/output frequency ratios. See Table 1 and Table 2 for supported frequency ranges and output to input frequency ratios. | | | |
| F_RANGE | 0 | VCO ÷ 1 (High input frequency range) | VCO ÷ 2 (Low input frequency range) |
| FSELA | 0 | Output divider ÷ 4 | Output divider ÷ 6 |
| FSELB | 0 | Output divider ÷ 4 | Output divider ÷ 2 |
| FSELC | 0 | Output divider ÷ 2 | Output divider ÷ 4 |
| MR/$\overline{\text{OE}}$ | 0 | Outputs enabled (active) | Outputs disabled (high–impedance state) and reset of the device. During reset, the PLL feedback loop is open and the VCO is operating at its lowest frequency. The MPC9352 requires reset at power–up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than two reference clock cycles (CCLK). |
| $\overline{\text{PLL\_EN}}$ | 0 | Normal operation mode with PLL enabled. | Test mode with PLL disabled. CCLK is substituted for the internal VCO output. MPC9352 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable. |

**Table 3: GENERAL SPECIFICATIONS**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output Termination Voltage | | $V_{CC} \div 2$ | | V | |
| MM | ESD Protection (Machine Model) | 200 | | | V | |
| HBM | ESD Protection (Human Body Model) | 2000 | | | V | |
| LU | Latch–Up Immunity | 200 | | | mA | |
| $C_{PD}$ | Power Dissipation Capacitance | | 10 | | pF | Per output |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | Inputs |

2

**Table 4: ABSOLUTE MAXIMUM RATINGS[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage Temperature | -65 | 125 | °C | |

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 5: DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40° to 85°C)

| Sym-bol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | | | 0.8 | V | LVCMOS |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$=-24 mA[a] |
| $V_{OL}$ | Output Low Voltage | | | 0.55<br>0.30 | V<br>V | $I_{OL}$= 24 mA<br>$I_{OL}$= 12 mA |
| $Z_{OUT}$ | Output Impedance | | 14 - 17 | | Ω | |
| $I_{IN}$ | Input Current[b] | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CCA}$ | Maximum PLL Supply Current | | 3.0 | 5.0 | mA | $V_{CCA}$ Pin |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a. The MPC9352 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.
b. Inputs have pull–down resistors affecting the input current.

**Table 6: AC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40° to 85°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Reference Frequency in PLL mode[c] | ÷ 2 feedback[d] | 100 | | 200 | MHz | |
| | | ÷ 4 feedback | 50 | | 100 | MHz | |
| | | ÷ 6 feedback | 33.3 | | 66.6 | MHz | |
| | | ÷ 8 feedback | 25 | | 50 | MHz | |
| | | ÷ 12 feedback | 16.67 | | 33.3 | MHz | |
| | Input Reference Frequency in PLL bypass mode[e] | | | | TBD | MHz | |
| $f_{VCO}$ | VCO Lock Frequency Range[f] | | 200 | | 400 | MHz | |
| $f_{MAX}$ | Output Frequency | ÷ 2 output[g] | 100 | | 200 | MHz | |
| | | ÷ 4 output | 50 | | 100 | MHz | |
| | | ÷ 6 output | 33.3 | | 66.6 | MHz | |
| | | ÷ 8 output | 25 | | 50 | MHz | |
| | | ÷ 12 output | 16.67 | | 33.3 | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 25 | | 75 | % | |
| $t_r$, $t_f$ | CCLK Input Rise/Fall Time | | | | 1.0 | ns | 0.8 to 2.0V |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) | CCLK to FB_IN | | ±100 | | ps | PLL locked |
| $t_{sk(o)}$ | Output-to-Output Skew[h] | | | | 150 | ps | |
| DC | Output Duty Cycle | | 45 | 50 | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.55 to 2.4V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 10 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 10 | ns | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1σ)[i] | | TBD | | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1σ) | | TBD | | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1σ) | | TBD | | ps | |
| BW | PLL closed loop bandwidth[j] | ÷ 2 feedback | | | TBD | kHz | |
| | | ÷ 4 feedback | | | TBD | kHz | |
| | | ÷ 6 feedback | | | TBD | kHz | |
| | | ÷ 8 feedback | | | TBD | kHz | |
| | | ÷ 12 feedback | | | TBD | kHz | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 10 | | ms | |

a. All AC characteristics are design targets and subject to change upon device characterization.
b. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
c. PLL mode requires PLL_EN = 0 to enable the PLL and zero–delay operation.
d. ÷2 feedback (FB) can be accomplished by setting F_RANGE = 0 and the connection of one ÷2 output to FB_IN. See Table 1 for other feedback configurations.
e. In bypass mode, the MPC9352 divides the input reference clock.
f. The input frequency $f_{ref}$ on CCLK must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$.
g. See Table 9 and Table 10 for output divider configurations.
h. See application section for part–to–part skew calculation.
i. See application section for a jitter calculation for other confidence factors than 1 σ.
j. –3 dB point of PLL transfer characteristics.

**Table 7: DC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40° to 85°C)

| Sym-bol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | –0.3 | | 0.7 | V | LVCMOS |
| $V_{OH}$ | Output High Voltage | 1.8 | | | V | $I_{OH}$=-15 mA[a] |
| $V_{OL}$ | Output Low Voltage | | | 0.6 | V | $I_{OL}$= 15 mA |
| $Z_{OUT}$ | Output Impedance | | 17 - 20 | | Ω | |
| $I_{IN}$ | Input Current | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CCA}$ | Maximum PLL Supply Current | | 2.0 | 5.0 | mA | $V_{CCA}$ Pin |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a. The MPC9352 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.

**Table 8: AC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40° to 85°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Reference Frequency in PLL mode[c] | ÷ 2 feedback[d] | 100 | | 200 | MHz | |
| | | ÷ 4 feedback | 50 | | 100 | MHz | |
| | | ÷ 6 feedback | 33.3 | | 66.6 | MHz | |
| | | ÷ 8 feedback | 25 | | 50 | MHz | |
| | | ÷ 12 feedback | 16.67 | | 33.3 | MHz | |
| | Input Reference Frequency in PLL bypass mode[e] | | | | TBD | MHz | |
| $f_{VCO}$ | VCO Lock Frequency Range[f] | | 200 | | 400 | MHz | |
| $f_{MAX}$ | Output Frequency | ÷ 2 output[g] | 100 | | 200 | MHz | |
| | | ÷ 4 output | 50 | | 100 | MHz | |
| | | ÷ 6 output | 33.3 | | 66.6 | MHz | |
| | | ÷ 8 output | 25 | | 50 | MHz | |
| | | ÷ 12 output | 16.67 | | 33.3 | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 25 | | 75 | % | |
| $t_r$, $t_f$ | CCLK Input Rise/Fall Time | | | | 1.0 | ns | 0.7 to 1.7V |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) | CCLK to FB_IN | | ±100 | | ps | PLL locked |
| $t_{sk(o)}$ | Output-to-Output Skew[h] | | | | 150 | ps | |
| DC | Output Duty Cycle | | 45 | 50 | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.6 to 1.8V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 10 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 10 | ns | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1σ)[i] | | TBD | | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1σ) | | TBD | | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1σ) | | TBD | | ps | |
| BW | PLL closed loop bandwidth[j] | ÷ 2 feedback | | | TBD | kHz | |
| | | ÷ 4 feedback | | | TBD | kHz | |
| | | ÷ 6 feedback | | | TBD | kHz | |
| | | ÷ 8 feedback | | | TBD | kHz | |
| | | ÷ 12 feedback | | | TBD | kHz | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 10 | | ms | |

a. All AC characteristics are design targets and subject to change upon device characterization.
b. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
c. PLL mode requires PLL_EN = 0 to enable the PLL and zero–delay operation.
d. ÷2 feedback (FB) can be accomplished by setting F_RANGE = 0 and the connection of one ÷2 output to FB_IN. See Table 1 for other feedback configurations.
e. In bypass mode, the MPC9352 divides the input reference clock.
f. The input frequency $f_{ref}$ on CCLK must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$.
g. See Table 9 and Table 10 for output divider configurations.
h. See application section for part–to–part skew calculation.
i. See application section for a jitter calculation for other confidence factors than 1 σ.
j. –3 dB point of PLL transfer characteristics.

## APPLICATIONS INFORMATION

### Programming the MPC9352

The MPC9352 supports output clock frequencies from 16.67 to 200 MHz. Different feedback and output divider configurations can be used to achieve the desired input to output frequency relationship. The feedback frequency and divider should be used to situate the VCO in the frequency lock range between 200 and 400 MHz for stable and optimal operation. The FSELA, FSELB, FSELC pins select the desired output clock frequencies. Possible frequency ratios of the reference clock input to the outputs are 1:1, 1:2, 1:3, 3:2 as well as 2:3, 3:1 and 2:1. Table 1 illustrates the various output configurations and frequency ratios supported by the MPC9352. See also Table 9, Table 10 and Figure 3 to Figure 6 for further reference.



**Table 9: MPC9352 Example Configuration (F_RANGE = 0)**

| PLL Feedback | fref[a] [MHz] | FSELA | FSELB | FSELC | QA[0:4]:fref ratio | QB[0:3]:fref ratio | QC[0:1]:fref ratio |
|---|---|---|---|---|---|---|---|
| VCO ÷ 2[b] | 100-200 | 0 | 1 | 0 | fref ÷ 2 (50-100 MHz) | fref (100-200 MHz) | fref (100-200 MHz) |
| | | 0 | 1 | 1 | fref ÷ 2 (50-100 MHz) | fref (100-200 MHz) | fref ÷ 2 (50-100 MHz) |
| | | 1 | 1 | 0 | fref ÷ 3 (33-67 MHz) | fref (100-200 MHz) | fref (100-200 MHz) |
| | | 1 | 1 | 1 | fref ÷ 3 (33-67 MHz) | fref (100-200 MHz) | fref ÷ 2 (50-100 MHz) |
| VCO ÷ 4[c] | 50-100 | 0 | 0 | 0 | fref (50-100 MHz) | fref (50-100 MHz) | fref · 2 (100-200 MHz) |
| | | 0 | 0 | 1 | fref (50-100 MHz) | fref (50-100 MHz) | fref (50-100 MHz) |
| | | 1 | 0 | 0 | fref · 2÷3 (33-66 MHz) | fref (50-100 MHz) | fref · 2 (100-200 MHz) |
| | | 1 | 0 | 1 | fref · 2÷3 (33-66 MHz) | fref (50-100 MHz) | fref (50-100 MHz) |
| VCO ÷ 6[d] | 33.3-66.67 | 1 | 0 | 0 | fref (33-66 MHz) | fref ·3÷2 (50-100 MHz) | fref · 3 (100-200 MHz) |
| | | 1 | 0 | 1 | fref (33-66 MHz) | fref ·3÷2 (50-100 MHz) | fref ·3÷2 (50-100 MHz) |
| | | 1 | 1 | 0 | fref (33-66 MHz) | fref · 3 (100-200 MHz) | fref · 3 (100-200 MHz) |
| | | 1 | 1 | 1 | fref (33-66 MHz) | fref · 3 (100-200 MHz) | fref ·3÷2 (50-100 MHz) |

a. fref is the input clock reference frequency (CCLK)
b. QBx connected to FB_IN and FSELB=1
c. QBx connected to FB_IN and FSELB=0
d. QAx connected to FB_IN and FSELA=1

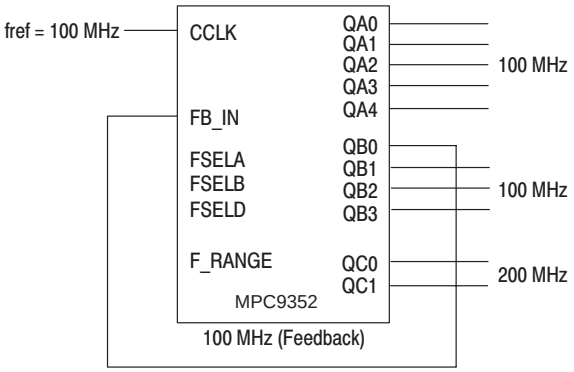
**Table 10: MPC9352 Example Configurations (F_RANGE = 1)**

| PLL Feedback | fref[a] [MHz] | FSELA | FSELB | FSELC | QA[0:4]:fref ratio | QB[0:3]:fref ratio | QC[0:1]:fref ratio |
|---|---|---|---|---|---|---|---|
| VCO ÷ 8[b] | 25-50 | 0 | 0 | 0 | fref (25-50 MHz) | fref (25-50 MHz) | fref · 2 (50-100 MHz) |
| | | 0 | 0 | 1 | fref (25-50 MHz) | fref (25-50 MHz) | fref (25-50 MHz) |
| | | 1 | 0 | 0 | fref ·2÷3 (16-33 MHz) | fref (25-50 MHz) | fref · 2 (50-100 MHz) |
| | | 1 | 0 | 1 | fref ·2÷3 (16-33 MHz) | fref (25-50 MHz) | fref (25-50 MHz) |
| VCO ÷ 12[c] | 16.67-33.3 | 1 | 0 | 0 | fref (16-33 MHz) | fref ·3÷2 (25-50 MHz) | fref · 3 (50-100 MHz) |
| | | 1 | 0 | 1 | fref (16-33 MHz) | fref ·3÷2 (25-50 MHz) | fref ·3÷2 (25-50 MHz) |
| | | 1 | 1 | 0 | fref (16-33 MHz) | fref · 3 (50-100 MHz) | fref · 3 (50-100 MHz) |
| | | 1 | 1 | 1 | fref (16-33 MHz) | fref · 3 (50-100 MHz) | fref ·3÷2 (25-50 MHz) |

a. fref is the input clock reference frequency (CCLK)
b. QBx connected to FB_IN and FSELB=0
c. QAx connected to FB_IN and FSELA=1

### Example Configurations for the MPC9352

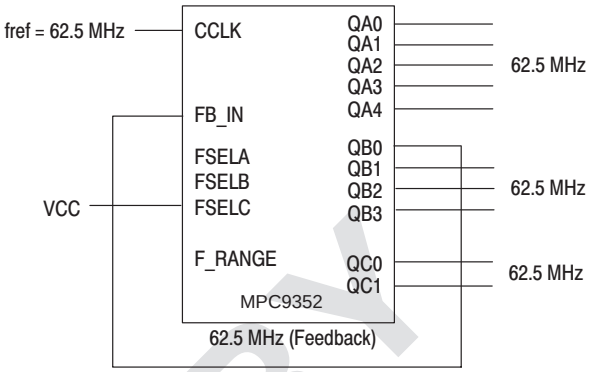
**Figure 3. MPC9352 Default Configuration**




MPC9352 default configuration (feedback of QB0 = 100 MHz). All control pins are left open.

| Frequency range | Min | Max |
|---|---|---|
| Input | 50 MHz | 100 MHz |
| QA outputs | 50 MHz | 10 MHz |
| QB outputs | 50 MHz | 100 MHz |
| QC outputs | 100 MHz | 200 MHz |

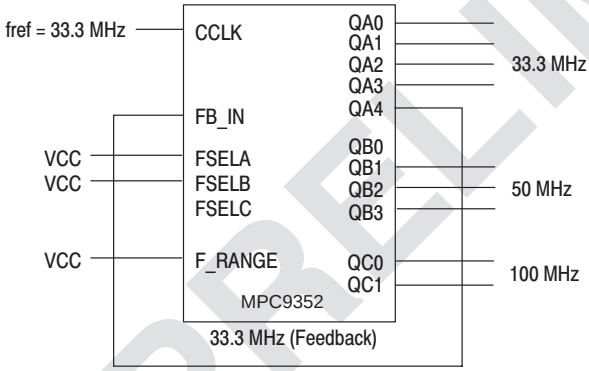
**Figure 4. MPC9352 Zero Delay Buffer Configuration**




MPC9352 zero–delay (feedback of QB0 = 62.5 MHz). All control pins are left open except FSELC = 1. All outputs are locked in frequency and phase to the input clock.

| Frequency range | Min | Max |
|---|---|---|
| Input | 50 MHz | 100 MHz |
| QA outputs | 50 MHz | 10 MHz |
| QB outputs | 50 MHz | 100 MHz |
| QC outputs | 50 MHz | 100 MHz |

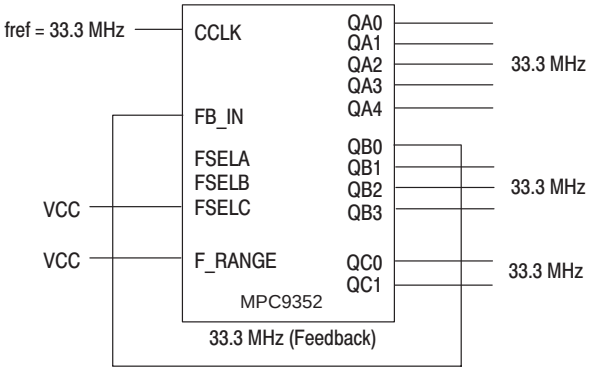
**Figure 5. MPC9352 Default Configuration**




MPC9352 configuration to multiply the reference frequency by 3, 3÷2 and 1. PLL feedback of QA4 = 33.3 MHz.

| Frequency range | Min | Max |
|---|---|---|
| Input | 25 MHz | 50 MHz |
| QA outputs | 50 MHz | 10 MHz |
| QB outputs | 50 MHz | 100 MHz |
| QC outputs | 100 MHz | 200 MHz |

**Figure 6. MPC9352 Zero Delay Buffer Config. 2**




MPC9352 zero–delay (feedback of QB0 = 33.3 MHz). Equivalent to Table 2 except F_RANGE = 1 enabling a lower input and output clock frequency.

| Frequency range | Min | Max |
|---|---|---|
| Input | 25 MHz | 50 MHz |
| QA outputs | 25 MHz | 50 MHz |
| QB outputs | 25 MHz | 50 MHz |
| QC outputs | 25 MHz | 50 MHz |

2

**Power Supply Filtering**

The MPC9352 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the $V_{CCA}$ (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC9352 provides separate power supplies for the output buffers ($V_{CC}$) and the phase-locked loop ($V_{CCA}$) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the $V_{CCA}$ pin for the MPC9352. Figure 7 illustrates a typical power supply filter scheme. The MPC9352 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor $R_F$. From the data sheet the $I_{CCA}$ current (the current sourced through the $V_{CCA}$ pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V ($V_{CC}$=3.3V or $V_{CC}$=2.5V) must be maintained on the $V_{CCA}$ pin. The resistor $R_F$ shown in Figure 7 "$V_{CCA}$ Power Supply Filter" must have a resistance of 270Ω ($V_{CC}$=3.3V) or 9-10Ω ($V_{CC}$=2.5V) to meet the voltage drop criteria.

$R_F$ = 270Ω for $V_{CC}$ = 3.3V
$R_F$ = 9–10Ω for $V_{CC}$ = 2.5V

$C_F$ = 1 μF for $V_{CC}$ = 3.3V
$C_F$ = 22 μF for $V_{CC}$ = 2.5V

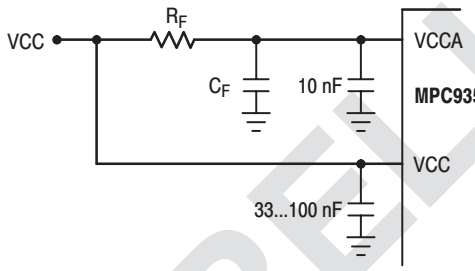



**Figure 7. $V_{CCA}$ Power Supply Filter**

The minimum values for $R_F$ and the filter capacitor $C_F$ are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 7 "$V_{CCA}$ Power Supply Filter", the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9352 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Using the MPC9352 in zero–delay applications**

Nested clock trees are typical applications for the MPC9352. Designs using the MPC9352 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC9352 clock driver allows for its use as a zero delay buffer. One example configuration is to use a ÷4 output as a feedback to the PLL and configuring all other outputs to a divide-by-4 mode. The propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

**Calculation of part-to-part skew**

The MPC9352 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9352 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\,LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

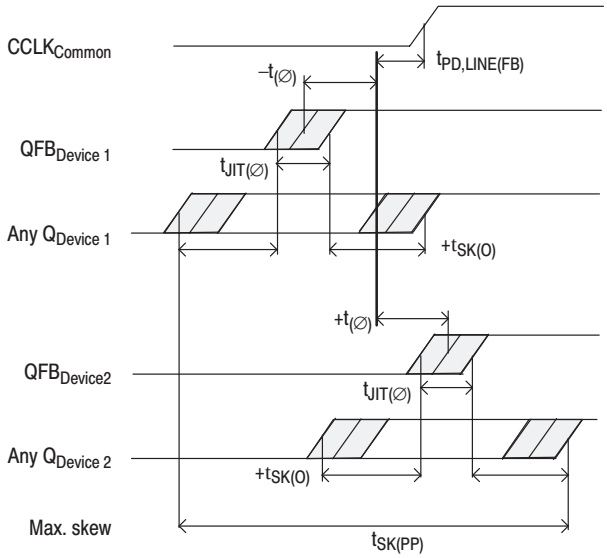



**Figure 8. MPC9352 max. device-to-device skew**

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 11.

**Table 11: Confidence Facter CF**

| CF | Probability of clock edge within the distribution |
|---|---|
| ± 1σ | 0.68268948 |
| ± 2σ | 0.95449988 |
| ± 3σ | 0.99730007 |
| ± 4σ | 0.99993663 |
| ± 5σ | 0.99999943 |
| ± 6σ | 0.99999999 |

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of -295 ps to 295 ps[1] relative to CCLK:

$t_{SK(PP)}$ = *[–100ps...100ps] + [–150ps...150ps] + [(15ps · –3)...(15ps · 3)] +* $t_{PD,\ LINE(FB)}$

$t_{SK(PP)}$ = *[–295ps...295ps] +* $t_{PD,\ LINE(FB)}$

Due to the frequency dependence of the I/O jitter, Figure 9 “Max. I/O Jitter versus frequency” can be used for a more precise timing performance analysis.

TBD
See MPC961C application section for
an example I/O jitter characteristics

**Figure 9. Max. I/O Jitter versus frequency**

**Driving Transmission Lines**

The MPC9352 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}$÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9352 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 10 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9352 clock driver is effectively doubled due to its capability to drive multiple lines.

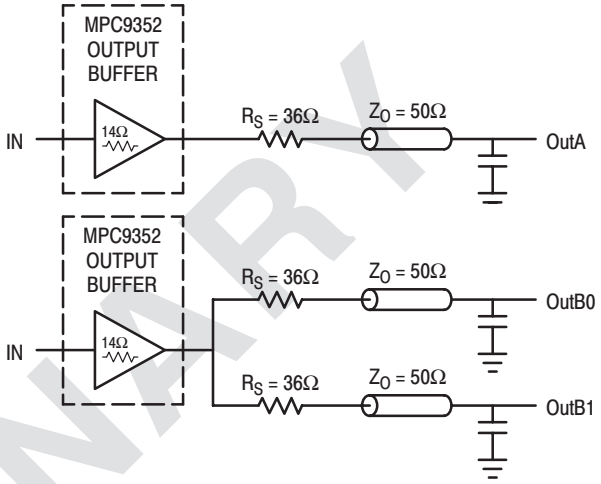



**Figure 10. Single versus Dual Transmission Lines**

The waveform plots in Figure 11 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9352 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9352. The output waveform in Figure 11 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$V_L = V_S ( Z_0 \div (R_S + R_0 + Z_0))$
$Z_0 = 50\Omega \parallel 50\Omega$
$R_S = 36\Omega \parallel 36\Omega$
$R_0 = 14\Omega$
$V_L = 3.0 ( 25 \div (18+17+25)$
$= 1.31V$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

1. Final skew data pending specification.

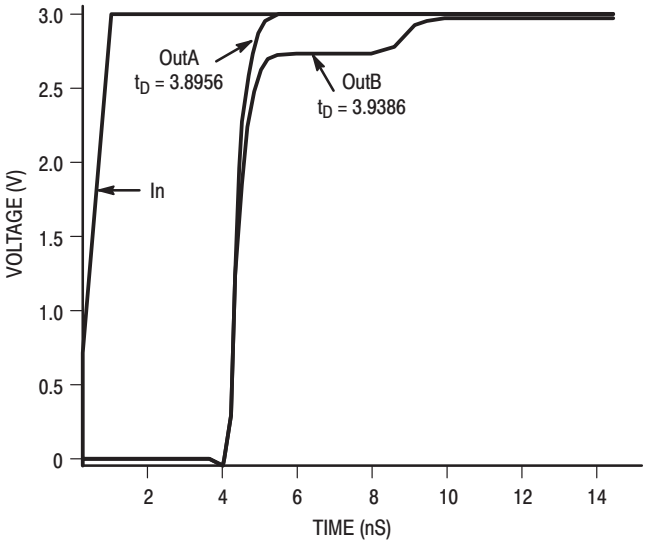
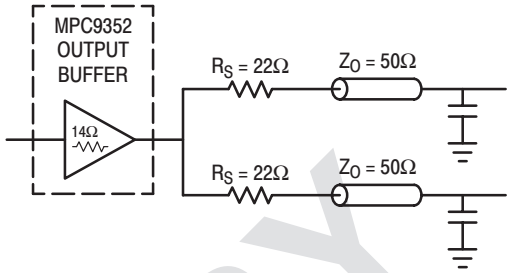



**Figure 11. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 12 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




$14\Omega + 22\Omega \parallel 22\Omega = 50\Omega \parallel 50\Omega$
$25\Omega = 25\Omega$

**Figure 12. Optimized Dual Line Termination**

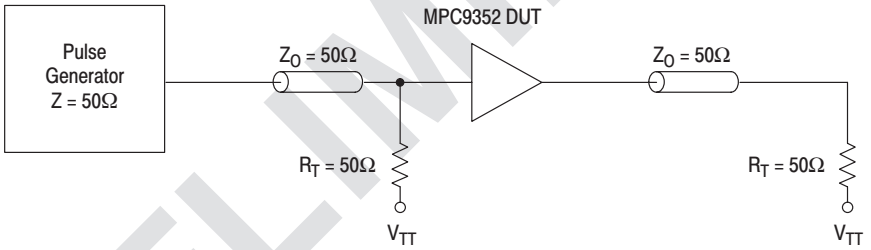
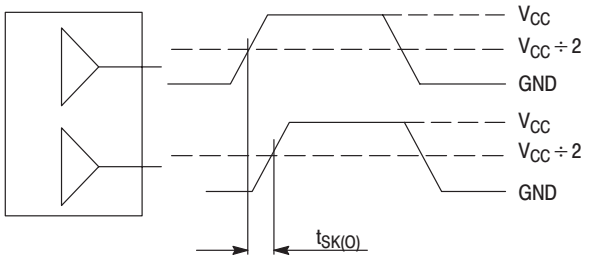



**Figure 13. CCLK MPC9352 AC test reference for $V_{cc}$ = 3.3V and $V_{cc}$ = 2.5V**




The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 14. Output–to–output Skew $t_{SK(O)}$**

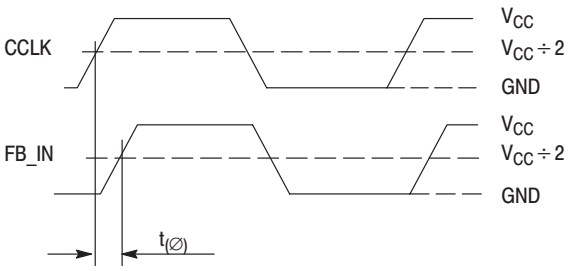
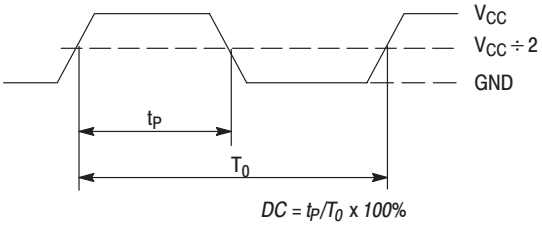
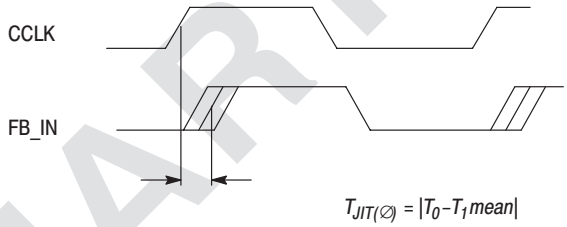



**Figure 15. Propagation delay ($t_{(\varnitheta)}$, static phase offset) test reference**



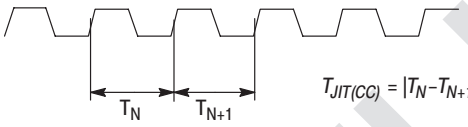

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 16. Output Duty Cycle (DC)**



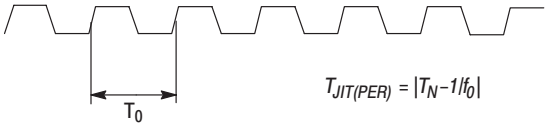

The deviation in $t_0$ for a controlled edge with respect to a $t_0$ mean in a random sample of cycles

**Figure 17. I/O Jitter**




The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

**Figure 18. Cycle–to–cycle Jitter**




The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

**Figure 19. Period Jitter**

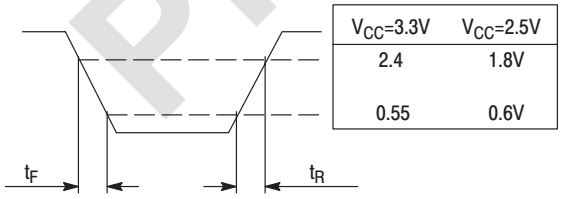



**Figure 20. Output Transition Time Test Reference**

# Low Voltage PLL Clock Driver

**MPC950**

**See Upgrade Product – MPC9350**

**LOW VOLTAGE PLL CLOCK DRIVER**

**FA SUFFIX**
32–LEAD LQFP PACKAGE
CASE 873A–02

2

The MPC950 is a 3.3V compatible, PLL based clock driver device targeted for high performance clock tree designs. With output frequencies of up to 180MHz and output skews of 375ps the MPC950 is ideal for the most demanding clock tree designs. The devices employ a fully differential PLL design to minimize cycle–to–cycle and long term jitter. This parameter is of significant importance when the clock driver is providing the reference clock for PLL's on board today's microprocessors and ASiC's. The devices offer 9 low skew outputs, the outputs are configurable to support the clocking needs of the various high performance microprocessors.

- Fully Integrated PLL
- Oscillator or Crystal Reference Input
- Output Frequency up to 180MHz
- Outputs Disable in High Impedance
- Compatible with **PowerPC**™, Intel and High Performance RISC Microprocessors
- LQFP Packaging
- Output Frequency Configurable
- ±100ps Typical Cycle–to–Cycle Jitter

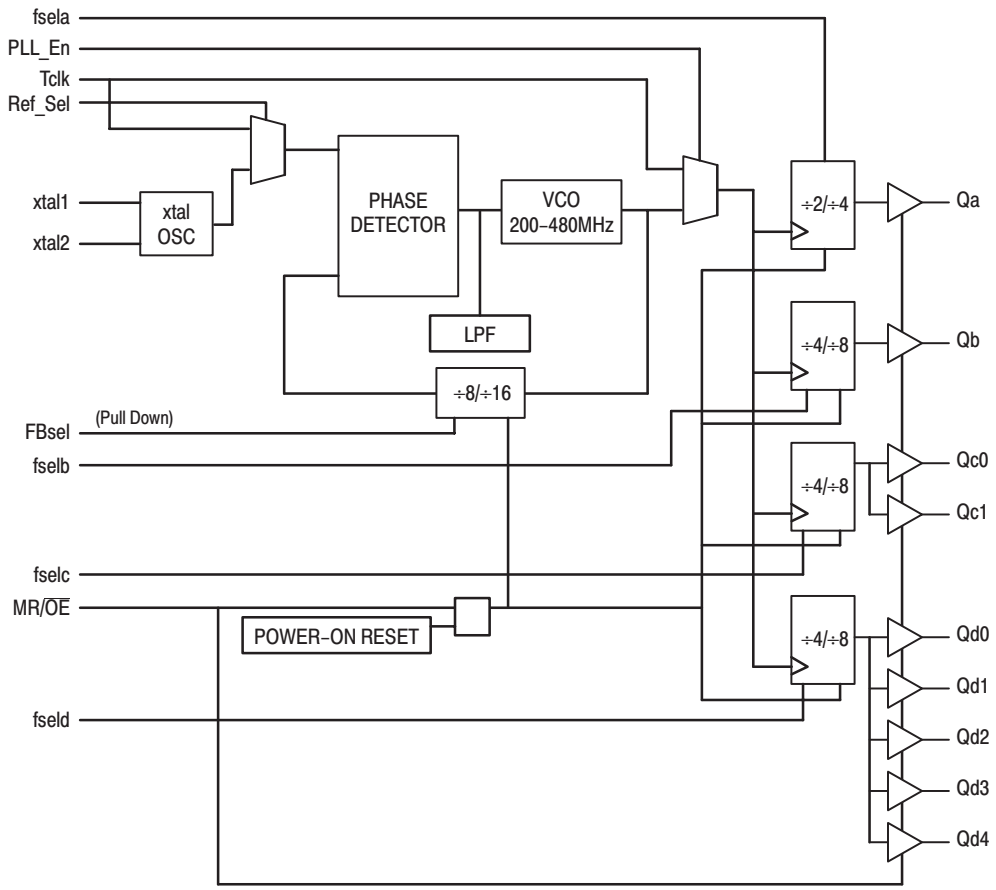
Two selectable feedback division ratios are available on the MPC950 to provide input reference clock flexibility. The FBSEL pin will choose between a divide by 8 or a divide by 16 of the VCO frequency to be compared with the input reference to the MPC950. The internal VCO is running at either 2x or 4x the high speed output, depending on configuration, so that the input reference will be either one half, one fourth or one eighth the high speed output.

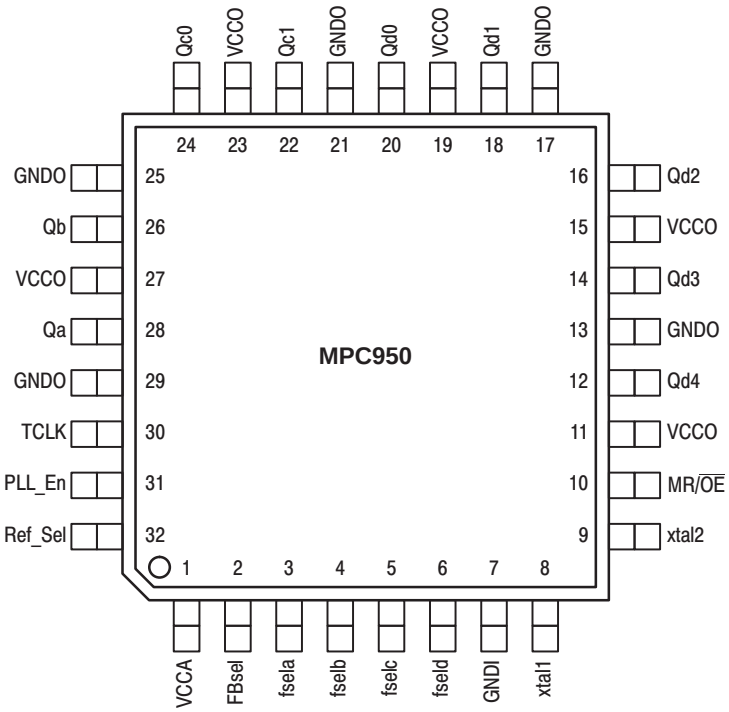
The MPC950 provides an external test clock input for scan clock distribution or system diagnostics. In addition the REF_SEL pin allows the user to select between a crystal input to an on–board oscillator for the reference or to chose a TTL level oscillator input directly. The on–board crystal oscillator requires no external components beyond a series resonant crystal.

The MPC950 is fully 3.3V compatible and require no external loop filter components. All inputs accept LVCMOS or LVTTL compatible levels while the outputs provide LVCMOS levels with the capability to drive terminated 50Ω transmission lines. Select inputs do not have internal pull–up/pull–down resistors and thus must be set externally. For series terminated 50Ω lines, each of the MPC950 outputs can drive two traces giving the device an effective fanout of 1:18. The device is packaged in a 7x7mm 32–lead LQFP package to provide the optimum combination of board density and performance.


**Rev 7**

## MPC950 LOGIC DIAGRAM




### FUNCTION TABLES

| Ref_Sel | Function |
|---|---|
| 1 | TCLK |
| 0 | XTAL_OSC |

| PLL_En | Function |
|---|---|
| 1 | PLL Enabled |
| 0 | PLL Bypass |

| FBsel | Function |
|---|---|
| 1 | ÷8 |
| 0 | ÷16 |

| MR/$\overline{OE}$ | Function |
|---|---|
| 1 | Outputs Disabled |
| 0 | Outputs Enabled |

| fseln | Function |
|---|---|
| 1 | Qa = ÷4; Qb:d = ÷8 |
| 0 | Qa = ÷2; Qb:d = ÷4 |

**FUNCTION TABLE – MPC950**

| INPUTS | | | | OUTPUTS | | | | TOTALS | | |
|---|---|---|---|---|---|---|---|---|---|---|
| fsela | fselb | fselc | fseld | Qa(1) | Qb(1) | Qc(2) | Qd(5) | Total 2x | Total x | Total x/2 |
| 0 | 0 | 0 | 0 | 2x | x | x | x | 1 | 8 | 0 |
| 0 | 0 | 0 | 1 | 2x | x | x | x/2 | 1 | 3 | 5 |
| 0 | 0 | 1 | 0 | 2x | x | x/2 | x | 1 | 6 | 2 |
| 0 | 0 | 1 | 1 | 2x | x | x/2 | x/2 | 1 | 1 | 7 |
| 0 | 1 | 0 | 0 | 2x | x/2 | x | x | 1 | 7 | 1 |
| 0 | 1 | 0 | 1 | 2x | x/2 | x | x/2 | 1 | 2 | 6 |
| 0 | 1 | 1 | 0 | 2x | x/2 | x/2 | x | 1 | 3 | 5 |
| 0 | 1 | 1 | 1 | 2x | x/2 | x/2 | x/2 | 1 | 0 | 8 |
| 1 | 0 | 0 | 0 | x | x | x | x | 0 | 9 | 0 |
| 1 | 0 | 0 | 1 | x | x | x | x/2 | 0 | 4 | 5 |
| 1 | 0 | 1 | 0 | x | x | x/2 | x | 0 | 7 | 2 |
| 1 | 0 | 1 | 1 | x | x | x/2 | x/2 | 0 | 2 | 7 |
| 1 | 1 | 0 | 0 | x | x/2 | x | x | 0 | 8 | 1 |
| 1 | 1 | 0 | 1 | x | x/2 | x | x/2 | 0 | 3 | 6 |
| 1 | 1 | 1 | 0 | x | x/2 | x/2 | x | 0 | 6 | 3 |
| 1 | 1 | 1 | 1 | x | x/2 | x/2 | x/2 | 0 | 1 | 8 |

NOTE: x = $f_{VCO}/4$; 200MHz < $f_{VCO}$ < 480MHz.

**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 4.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | Input Current | | ±20 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

**THERMAL CHARACTERISTICS**

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | LVCMOS Inputs | 2.0 | | 3.6 | V | |
| $V_{IL}$ | Input LOW Voltage | LVCMOS Inputs | | | 0.8 | V | |
| $V_{OH}$ | Output HIGH Voltage | | 2.4 | | | V | $I_{OH}$ = –40mA, Note 1. |
| $V_{OL}$ | Output LOW Voltage | | | | 0.5 | V | $I_{OL}$ = 40mA, Note 1. |
| $I_{IN}$ | Input Current | | | | ±120 | µA | |
| $C_{IN}$ | Input Capacitance | | | | 4 | pF | |
| $C_{pd}$ | Power Dissipation Capacitance | | | 25 | | pF | Per Output |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | 90 | 115 | mA | All VCC Pins |
| $I_{CCPLL}$ | Maximum PLL Supply Current | | | 15 | 20 | mA | VCCA Pin Only |

1. The MPC950 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}/2$) transmission lines on the incident edge (see Applications Info section).

**PLL INPUT REFERENCE CHARACTERISTICS** ($T_A$ = 0 to 70°C)

| Symbol | Characteristic | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $t_r$, $t_f$ | TCLK Input Rise/Falls | | 3.0 | ns | |
| $f_{ref}$ | Reference Input Frequency | Note 1. | Note 1. | MHz | |
| $f_{Xtal}$ | Crystal Oscillator Frequency | 10 | 25 | MHz | Note 2. |
| $f_{refDC}$ | Reference Input Duty Cycle | 25 | 75 | % | |

1. Maximum and minimum input reference is limited by the VCO lock range and the feedback divider for the TCLK inputs.
2. See Applications Info section for more crystal information.

2

**AC CHARACTERISTICS** ($T_A$ = 0°C to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.10 | | 1.0 | ns | 0.8 to 2.0V, Note 1. |
| $t_{pw}$ | Output Duty Cycle | $t_{CYCLE}$/2–1000 | | $t_{CYCLE}$/2+1000 | ps | Note 1. |
| $t_{sk(O)}$ | Output–to–Output Skews Same Frequencies | | 200 | 375 | ps | Note 1. |
| | Different Frequencies<br>$Qa_{fmax}$ < 150MHz<br>$Qa_{fmax}$ > 150MHz | | 325 | 500<br>750 | | |
| $f_{VCO}$ | PLL VCO Lock Range | 200 | | 480 | MHz | |
| $f_{max}$ | Maximum Output Frequency<br>Qa (÷2)<br>Qa/Qb (÷4)<br>Qb (÷8) | | | 180<br>120<br>60 | MHz | Note 1. |
| $t_{PLZ,HZ}$ | Output Disable Time | | | 7 | ns | Note 1. |
| $t_{PZL}$ | Output Enable Time | | | 6 | ns | Note 1. |
| $t_{jitter}$ | Cycle–to–Cycle Jitter (Peak–to–Peak) | | ±100 | | ps | Note 2. |
| $t_{lock}$ | Maximum PLL Lock Time | | | 10 | ms | |

1. Termination of 50Ω to $V_{CC}$/2.
2. See Applications Info section for more jitter information.

## APPLICATIONS INFORMATION

### Programming the MPC950

The MPC950 clock driver outputs can be configured into several frequency relationships. The output dividers for the four output groups allows the user to configure the outputs into 1:1, 2:1, 4:1 and 4:2:1 frequency ratios. The use of even dividers ensures that the output duty cycle is always 50%. Table 1 illustrates the various output configurations, the table describes the outputs using the VCO frequency as a reference. As an example for a 4:2:1 relationship the Qa outputs would be set at VCO/2, the Qb's and Qc's at VCO/4 and the Qd's at VCO/8. These settings will provide output frequencies with a 4:2:1 relationship.

The division settings establish the output relationship, but one must still ensure that the VCO will be stable given the frequency of the outputs desired. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL is such that for output frequencies between 25 and 180MHz the MPC950 can generally be configured into a stable region.

The relationship between the input reference and the output frequency is also very flexible. Table 2 shows the multiplication factors between the inputs and outputs for the MPC950. Figure 1 through Figure 4 illustrates several programming possibilities, although not exhaustive it is representative of the potential applications.

**Table 1. Programmable Output Frequency Relationships**

| INPUTS | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|
| fsela | fselb | fselc | fseld | Qa | Qb | Qc | Qd |
| 0 | 0 | 0 | 0 | VCO/2 | VCO/4 | VCO/4 | VCO/4 |
| 0 | 0 | 0 | 1 | VCO/2 | VCO/4 | VCO/4 | VCO/8 |
| 0 | 0 | 1 | 0 | VCO/2 | VCO/4 | VCO/8 | VCO/4 |
| 0 | 0 | 1 | 1 | VCO/2 | VCO/4 | VCO/8 | VCO/8 |
| 0 | 1 | 0 | 0 | VCO/2 | VCO/8 | VCO/4 | VCO/4 |
| 0 | 1 | 0 | 1 | VCO/2 | VCO/8 | VCO/4 | VCO/8 |
| 0 | 1 | 1 | 0 | VCO/2 | VCO/8 | VCO/8 | VCO/4 |
| 0 | 1 | 1 | 1 | VCO/2 | VCO/8 | VCO/8 | VCO/8 |
| 1 | 0 | 0 | 0 | VCO/4 | VCO/4 | VCO/4 | VCO/4 |
| 1 | 0 | 0 | 1 | VCO/4 | VCO/4 | VCO/4 | VCO/8 |
| 1 | 0 | 1 | 0 | VCO/4 | VCO/4 | VCO/8 | VCO/4 |
| 1 | 0 | 1 | 1 | VCO/4 | VCO/4 | VCO/8 | VCO/8 |
| 1 | 1 | 0 | 0 | VCO/4 | VCO/8 | VCO/4 | VCO/4 |
| 1 | 1 | 0 | 1 | VCO/4 | VCO/8 | VCO/4 | VCO/8 |
| 1 | 1 | 1 | 0 | VCO/4 | VCO/8 | VCO/8 | VCO/4 |
| 1 | 1 | 1 | 1 | VCO/4 | VCO/8 | VCO/8 | VCO/8 |

**Table 2. Input Reference versus Output Frequency Relationships**

| | | | | | FB_Sel = ‘1’ | | | | FB_Sel = ‘0’ | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Config | fsela | fselb | fselc | fseld | Qa | Qb | Qc | Qd | Qa | Qb | Qc | Qd |
| 1 | 0 | 0 | 0 | 0 | 4x | 2x | 2x | 2x | 8x | 4x | 4x | 4x |
| 2 | 0 | 0 | 0 | 1 | 4x | 2x | 2x | x | 8x | 4x | 4x | 2x |
| 3 | 0 | 0 | 1 | 0 | 4x | 2x | x | 2x | 8x | 4x | 2x | 4x |
| 4 | 0 | 0 | 1 | 1 | 4x | 2x | x | x | 8x | 4x | 2x | 2x |
| 5 | 0 | 1 | 0 | 0 | 4x | x | 2x | 2x | 8x | 2x | 4x | 4x |
| 6 | 0 | 1 | 0 | 1 | 4x | x | 2x | x | 8x | 2x | 4x | 2x |
| 7 | 0 | 1 | 1 | 0 | 4x | x | x | 2x | 8x | 2x | 2x | 4x |
| 8 | 0 | 1 | 1 | 1 | 4x | x | x | x | 8x | 2x | 2x | 2x |
| 9 | 1 | 0 | 0 | 0 | 2x | 2x | 2x | 2x | 4x | 4x | 4x | 4x |
| 10 | 1 | 0 | 0 | 1 | 2x | 2x | 2x | x | 4x | 4x | 4x | 2x |
| 11 | 1 | 0 | 1 | 0 | 2x | 2x | x | 2x | 4x | 4x | 2x | 4x |
| 12 | 1 | 0 | 1 | 1 | 2x | 2x | x | x | 4x | 4x | 2x | 2x |
| 13 | 1 | 1 | 0 | 0 | 2x | x | 2x | 2x | 4x | 2x | 4x | 4x |
| 14 | 1 | 1 | 0 | 1 | 2x | x | 2x | x | 4x | 2x | 4x | 2x |
| 15 | 1 | 1 | 1 | 0 | 2x | x | x | 2x | 4x | 2x | 2x | 4x |
| 16 | 1 | 1 | 1 | 1 | 2x | x | x | x | 4x | 2x | 2x | 2x |

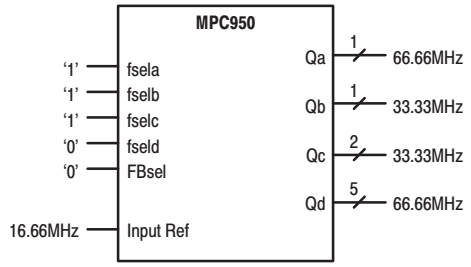



**Figure 1. Dual Frequency Configuration**

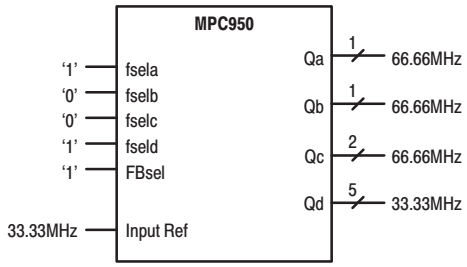



**Figure 2. Dual Frequency Configuration**



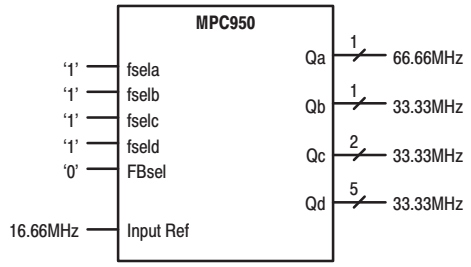



**Figure 3. Dual Frequency Configuration**

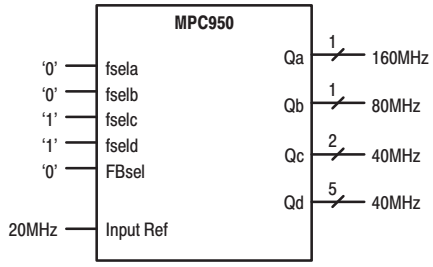



**Figure 4. Triple Frequency Configuration**

**Jitter Performance of the MPC950**

With the clock rates of today's digital systems continuing to increase more emphasis is being placed on clock distribution design and management. Among the issues being addressed is system clock jitter and how that affects the overall system timing budget. The MPC950 was designed to minimize clock jitter by employing a differential bipolar PLL as well as incorporating numerous power and ground pins in the design. The following few paragraphs will outline the jitter performance of the MPC950, illustrate the measurement limitations and provide guidelines to minimize the jitter of the device.

The most commonly specified jitter parameter is cycle–to–cycle jitter. Unfortunately with today's high performance measurement equipment there is no way to measure this parameter for jitter performance in the class demonstrated by the MPC950. As a result different methods are used which approximate cycle–to–cycle jitter. The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak–to–peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. If this is not the case the measurement inaccuracy will add significantly to the measured jitter. The oscilloscope cannot collect adjacent pulses, rather it collects data from a very large sample of pulses. It is safe to assume that collecting pulse information in this mode will produce jitter values somewhat larger than if consecutive cycles were measured, therefore, this measurement will represent an upper bound of cycle–to–cycle jitter. Most likely, this is a conservative estimate of the cycle–to–cycle jitter.

There are two sources of jitter in a PLL based clock driver, the commonly known random jitter of the PLL and the less intuitive jitter caused by synchronous, different frequency outputs switching. For the case where all of the outputs are switching at the same frequency the total jitter is exactly equal to the PLL jitter. In a device, like the MPC950, where a number of the outputs can be switching synchronously but at different frequencies a "multi–modal" jitter distribution can be seen on the highest frequency outputs. Because the output being monitored is affected by the activity on the other outputs it is important to consider what is happening on those other outputs. From Figure 5, one can see for each rising edge on the higher frequency signal the activity on the lower frequency signal is not constant. The activity on the other outputs tends to alter the internal thresholds of the device such that the placement of the edge being monitored is displaced in time. Because the signals are synchronous the relationship is periodic and the resulting jitter is a compilation of the PLL jitter superimposed on the displaced edges. When histograms are plotted the jitter looks like a "multi–modal" distribution as pictured in Figure 5. Depending on the size of the PLL jitter and the relative displacement of the edges the "multi–modal" distribution will appear truly "multi–modal" or simply like a "fat" Gaussian distribution. Again note that in the case where all the outputs are switching at the same frequency there is no edge displacement and the jitter is reduced to that of the PLL.

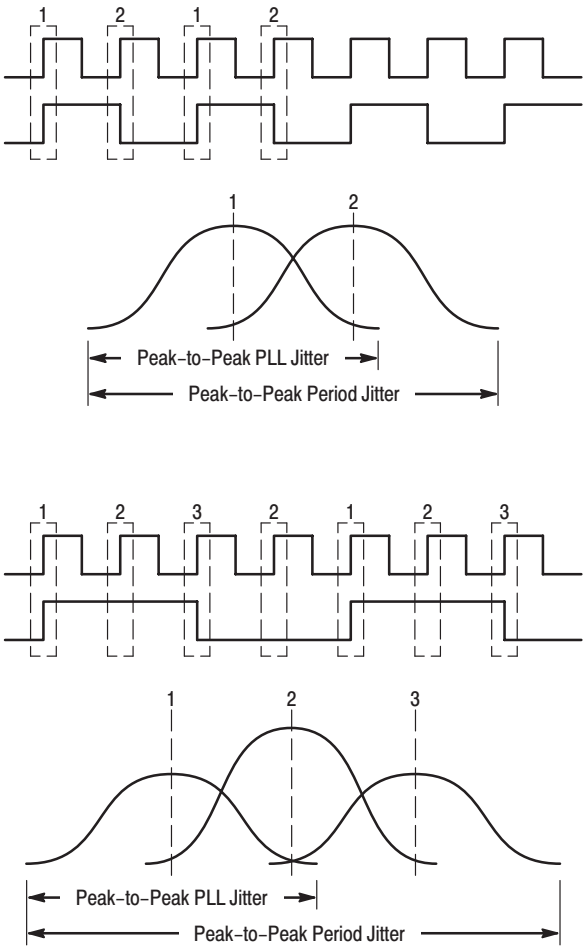
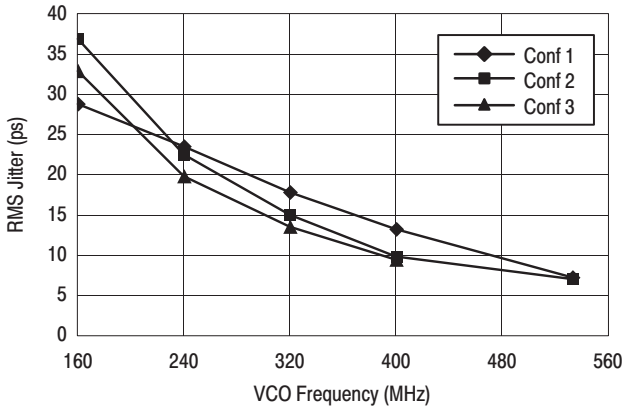
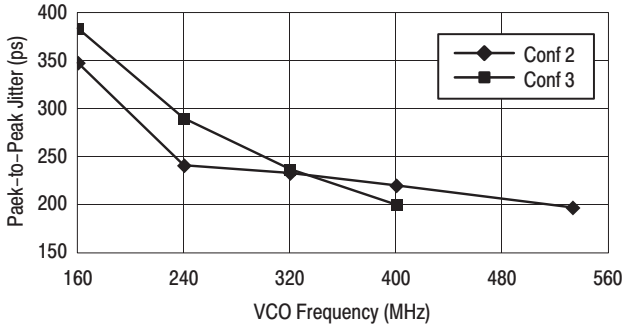



**Figure 5. PLL Jitter and Edge Displacement**




Conf 1 = All Outputs at the Same Frequency
Conf 2 = 4 Outputs at X, 5 Outputs at X/2
Conf 3 = 1 Output at X, 8 Outputs at X/4

**Figure 6. RMS PLL Jitter versus VCO Frequency**




Conf 2 = 4 Outputs at X, 5 Outputs at X/2
Conf 3 = 1 Output at X, 8 Outputs at X/4

**Figure 7. Peak–to–Peak Period Jitter versus VCO Frequency**

Figure 6 graphically represents the PLL jitter of the MPC950. The data was taken for several different output configurations. By triggering on the lowest frequency output the PLL jitter can be measured for configurations in which outputs are switching at different frequencies. As one can see in the figure the PLL jitter is much less dependent on output configuration than on internal VCO frequency.

Two different configurations were chosen to look at the period displacement caused by the switching outputs. Configuration 3 is considered worst case as the “trimodal” distribution (as pictured in Figure 5) represents the largest spread between distribution peaks. Configuration 2 is considered a typical configuration with half the outputs at a high frequency and the remaining outputs at one half the high frequency. For these cases the peak–to–peak numbers are reported in Figure 7 as the sigma numbers are useless because the distributions are not Gaussian. For situations where the outputs are synchronous and switching at different frequencies the measurement technique described here is insufficient to use for establishing guaranteed limits. Other techniques are currently being investigated to identify a more accurate and repeatable measurement so that guaranteed limits can be provided. The data generated does give a good indication of the general performance, a performance that in most cases is well within the requirements of today’s microprocessors.

Finally from the data there are some general guidelines that, if followed, will minimize the output jitter of the device. First and foremost always configure the device such that the VCO runs as fast as possible. This is by far the most critical parameter in minimizing jitter. Second keep the reference frequency as high as possible. More frequent updates at the phase detector will help to reduce jitter. Note that if there is a tradeoff between higher reference frequencies and higher VCO frequency always chose the higher VCO frequency to minimize jitter. The third guideline may be the most difficult, and in some cases impossible, to follow. Try to minimize the number of different frequencies sourced from a single chip. The fixed edge displacement associated with the switching noise in most cases nearly doubles the “effective” jitter of a high speed output.

**Power Supply Filtering**

The MPC950 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC950 provides separate power supplies for the output buffers (VCCO) and the phase–locked loop (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital out-

puts from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC950.

Figure 8 illustrates a typical power supply filter scheme. The MPC950 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the VCCA pin of the MPC950. From the data sheet the $I_{VCCA}$ current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V $V_{CC}$ supply is used. The resistor shown in Figure 8 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8–10Ω resistor to avoid potential $V_{CC}$ drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

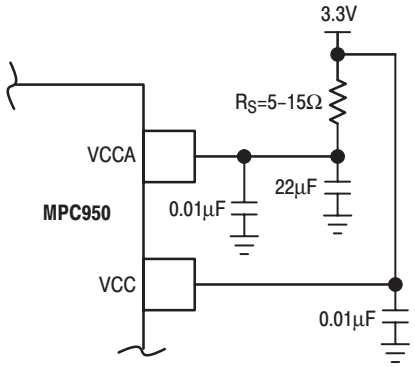



**Figure 8. Power Supply Filter**

Although the MPC950 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Using the On–Board Crystal Oscillator**

The MPC950 features an on–board crystal oscillator to allow for seed clock generation as well as final distribution. The on–board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC950 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required.

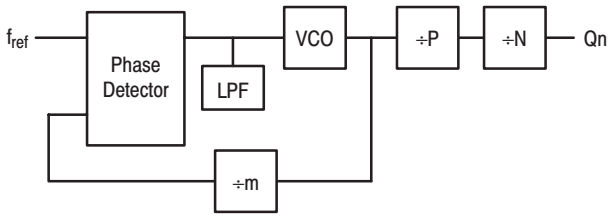
The oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on–board capacitors. Because the design is a series resonant design for the optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most off the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC950 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implementations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

**Table 3. Crystal Recommendation**

| Parameter | Value |
|---|---|
| Crystal Cut | Fundamental AT Cut |
| Resonance | Series Resonance* |
| Frequency Tolerance | ±75ppm at 25°C |
| Frequency/Temperature Stability | ±150ppm 0 to 70°C |
| Operating Range | 0 to 70°C |
| Shunt Capacitance | 5–7pF |
| Equivalent Series Resistance (ESR) | 50 to 80Ω Max |
| Correlation Drive Level | 100μW |
| Aging | 5ppm/Yr (First 3 Years) |

* See accompanying text for series versus parallel resonant discussion.

The MPC950 is a clock driver which was designed to generate outputs with programmable frequency relationships and not a synthesizer with a fixed input frequency. As a result the crystal input frequency is a function of the desired output frequency. To determine the crystal required to produce the desired output frequency for an application which utilizes internal feedback the block diagram of Figure 9 should be used. The P and the M values for the MPC950 are also included in Figure 9. The M values can be found in the configuration tables included in this applications section.




$$f_{ref} = \frac{f_{VCO}}{m}, \quad f_{VCO} = fQn \cdot N \cdot P$$

$$\therefore f_{ref} = \frac{fQn \cdot N \cdot P}{m}$$

m = 8 (FBsel = '1'), 16(FBsel = '0')
P = 1

**Figure 9. PLL Block Diagram**

For the MPC950 clock driver, the following will provide an example of how to determine the crystal frequency required for a given design.

Given:

Qa = 160MHz
Qb = 80MHz
Qc = 40MHz
Qd = 40MHz
FBSel = '0'

$$f_{ref} = \frac{fQn \cdot N \cdot P}{m}$$

From Table 3

fQd = VCO/8 then N = 8 OR fQa = VCO/2 then N = 2

From Figure 9

m = 16 and P = 1

$$f_{ref} = \frac{40 \cdot 8 \cdot 1}{16} = 20MHz \text{ OR } \frac{160 \cdot 2 \cdot 1}{16} = 20MHz$$

**Driving Transmission Lines**

The MPC950 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC950 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 10 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fan-out of the MPC950 clock driver is effectively doubled due to its capability to drive multiple lines.

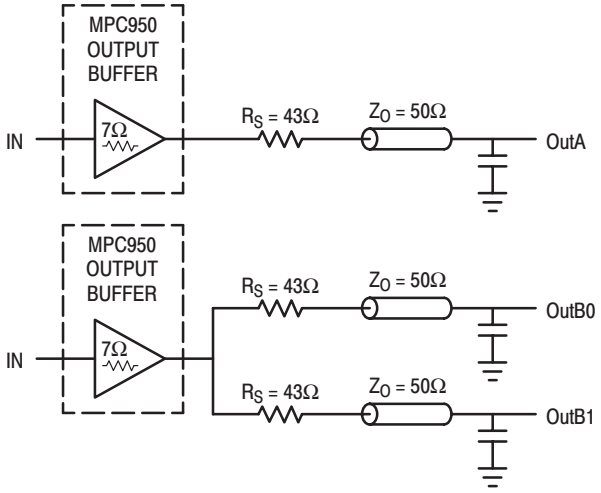



**Figure 10. Single versus Dual Transmission Lines**

The waveform plots of Figure 11 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC950 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC950. The output waveform in Figure 11 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

VL = VS ( Zo / (Rs + Ro +Zo))

Zo = 50Ω || 50Ω
Rs = 43Ω || 43Ω
Ro = 7Ω

VL = 3.0 (25 / (21.5 + 7 + 25) = 3.0 (25 / 53.5)
= 1.40V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

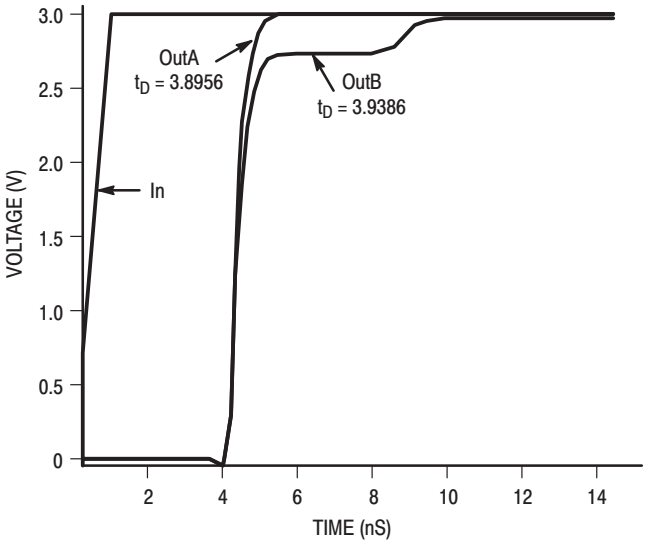



**Figure 11. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 12 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

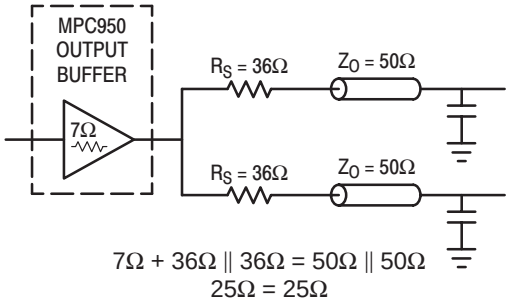



**Figure 12. Optimized Dual Line Termination**

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

# Low Voltage PLL Clock Driver

**MPC951**

**See Upgrade Product – MPC9351**

**LOW VOLTAGE PLL CLOCK DRIVER**



The MPC951 is a 3.3V compatible, PLL based clock driver device targeted for high performance clock tree designs. With output frequencies of up to 180MHz and output skews of 375ps the MPC951 is ideal for the most demanding clock tree designs. The devices employ a fully differential PLL design to minimize cycle–to–cycle and long term jitter. This parameter is of significant importance when the clock driver is providing the reference clock for PLL's on board today's microprocessors and ASiC's. The devices offer 9 low skew outputs, the outputs are configurable to support the clocking needs of the various high performance microprocessors.

- Fully Integrated PLL
- Output Frequency up to 180MHz
- Outputs Disable in High Impedance
- Compatible with **PowerPC**™, Intel and High Performance RISC Microprocessors
- LQFP Packaging
- Output Frequency Configurable
- ±100ps Typical Cycle–to–Cycle Jitter

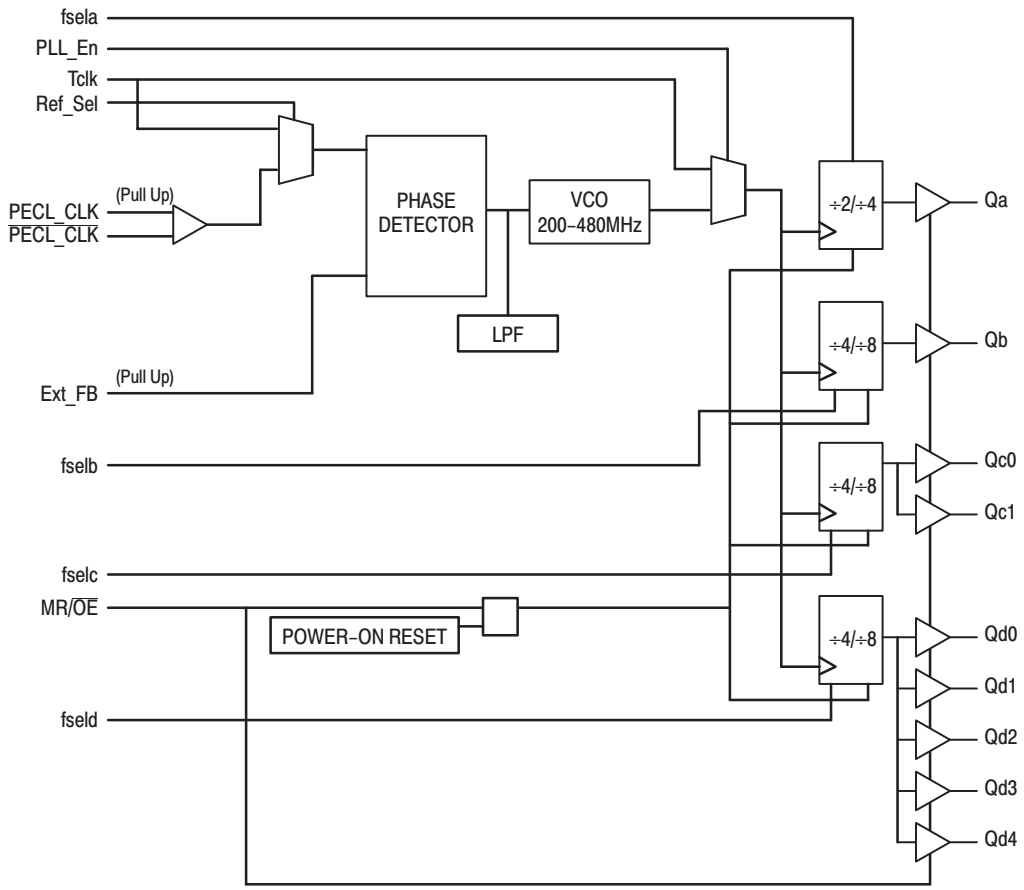
**FA SUFFIX**
32–LEAD LQFP PACKAGE
CASE 873A–02

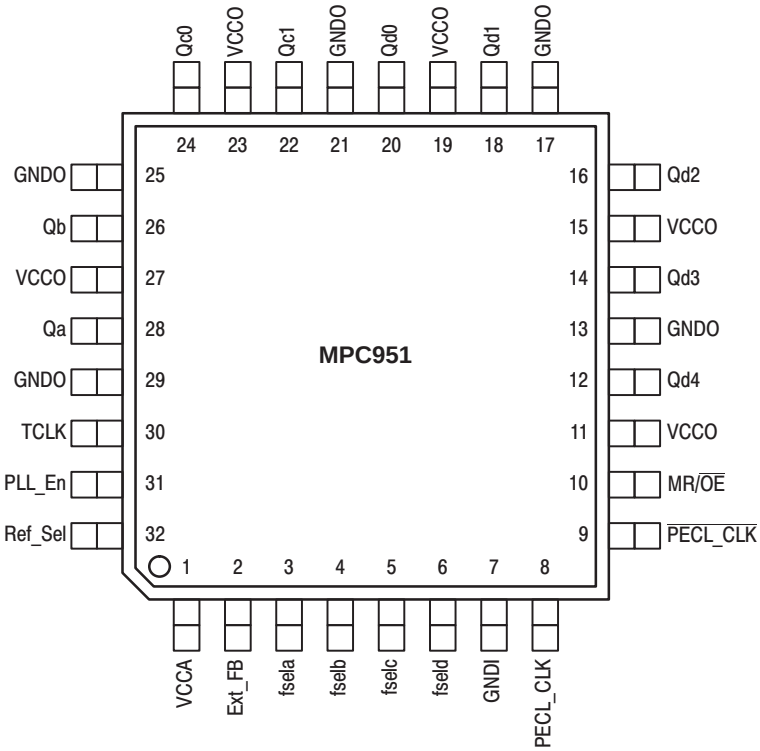
The MPC951 uses a differential PECL reference input and an external feedback input. These features allow for the MPC951 to be used as a zero delay, low skew fanout buffer. In addition, the external feedback allows for a wider variety of input–to–output frequency relationships. The REF_SEL pin allows for the selection of an alternate LVCMOS input clock to be used as a test clock or to provide the reference for the PLL from an LVCMOS source.

The MPC951 is fully 3.3V compatible and require no external loop filter components. All inputs accept LVCMOS or LVTTL compatible levels while the outputs provide LVCMOS levels with the capability to drive terminated 50Ω transmission lines. Select inputs do not have internal pull–up/pull–down resistors and thus must be set externally. If the PECL_CLK inputs are not used, they can be left open. For series terminated 50Ω lines, each of the MPC951 outputs can drive two traces giving the device an effective fanout of 1:18. The device is packaged in a 7x7mm 32–lead LQFP package to provide the optimum combination of board density and performance.


**Rev 0**

**MPC951 LOGIC DIAGRAM**




**FUNCTION TABLES**

| Ref_Sel | Function |
|---|---|
| 1 | TCLK |
| 0 | PECL_CLK |

| PLL_En | Function |
|---|---|
| 1 | PLL Enabled |
| 0 | PLL Bypass |

| MR/$\overline{OE}$ | Function |
|---|---|
| 1 | Outputs Disabled |
| 0 | Outputs Enabled |

| fseln | Function |
|---|---|
| 1 | Qa = ÷4; Qb:d = ÷8 |
| 0 | Qa = ÷2; Qb:d = ÷4 |

**FUNCTION TABLE – MPC951**

| INPUTS | | | | OUTPUTS | | | | TOTALS | | |
|---|---|---|---|---|---|---|---|---|---|---|
| fsela | fselb | fselc | fseld | Qa(1) | Qb(1) | Qc(2) | Qd(5) | Total 2x | Total x | Total x/2 |
| 0 | 0 | 0 | 0 | 2x | x | x | x | 1 | 8 | 0 |
| 0 | 0 | 0 | 1 | 2x | x | x | x/2 | 1 | 3 | 5 |
| 0 | 0 | 1 | 0 | 2x | x | x/2 | x | 1 | 6 | 2 |
| 0 | 0 | 1 | 1 | 2x | x | x/2 | x/2 | 1 | 1 | 7 |
| 0 | 1 | 0 | 0 | 2x | x/2 | x | x | 1 | 7 | 1 |
| 0 | 1 | 0 | 1 | 2x | x/2 | x | x/2 | 1 | 2 | 6 |
| 0 | 1 | 1 | 0 | 2x | x/2 | x/2 | x | 1 | 3 | 5 |
| 0 | 1 | 1 | 1 | 2x | x/2 | x/2 | x/2 | 1 | 0 | 8 |
| 1 | 0 | 0 | 0 | x | x | x | x | 0 | 9 | 0 |
| 1 | 0 | 0 | 1 | x | x | x | x/2 | 0 | 4 | 5 |
| 1 | 0 | 1 | 0 | x | x | x/2 | x | 0 | 7 | 2 |
| 1 | 0 | 1 | 1 | x | x | x/2 | x/2 | 0 | 2 | 7 |
| 1 | 1 | 0 | 0 | x | x/2 | x | x | 0 | 8 | 1 |
| 1 | 1 | 0 | 1 | x | x/2 | x | x/2 | 0 | 3 | 6 |
| 1 | 1 | 1 | 0 | x | x/2 | x/2 | x | 0 | 6 | 3 |
| 1 | 1 | 1 | 1 | x | x/2 | x/2 | x/2 | 0 | 1 | 8 |

NOTE: x = $f_{VCO}/4$; 200MHz < $f_{VCO}$ < 480MHz.

**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 4.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | Input Current | | ±20 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

**THERMAL CHARACTERISTICS**

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | LVCMOS Inputs | 2.0 | | 3.6 | V | |
| $V_{IL}$ | Input LOW Voltage | LVCMOS Inputs | | | 0.8 | V | |
| $V_{PP}$ | Peak–to–Peak Input Voltage | PECL_CLK | 300 | | 1000 | mV | |
| $V_{CMR}$ | Common Mode Range | PECL_CLK | $V_{CC}$–2.0 | | $V_{CC}$–0.6 | V | Note 1. |
| $V_{OH}$ | Output HIGH Voltage | | 2.4 | | | V | $I_{OH}$ = –40mA, Note 2. |
| $V_{OL}$ | Output LOW Voltage | | | | 0.5 | V | $I_{OL}$ = 40mA, Note 2. |
| $I_{IN}$ | Input Current | | | | ±120 | µA | |
| $C_{IN}$ | Input Capacitance | | | | 4 | pF | |
| $C_{pd}$ | Power Dissipation Capacitance | | | 25 | | pF | Per Output |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | 90 | 115 | mA | All VCC Pins |
| $I_{CCPLL}$ | Maximum PLL Supply Current | | | 15 | 20 | mA | VCCA Pin Only |

1. $V_{CMR}$ is the difference from the most positive side of the differential input signal. Normal operation is obtained when the “HIGH” input is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ specification.
2. The MPC951 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}/2$) transmission lines on the incident edge (see Applications Info section).

**PLL INPUT REFERENCE CHARACTERISTICS** ($T_A$ = 0 to 70°C)

| Symbol | Characteristic | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $t_r$, $t_f$ | TCLK Input Rise/Falls | | 3.0 | ns | |
| $f_{ref}$ | Reference Input Frequency | | 100 | MHz | Note 1. |
| $f_{refDC}$ | Reference Input Duty Cycle | 25 | 75 | % | |

1. Maximum and minimum input reference is limited by the VCO lock range and the feedback divider for the TCLK or PECL_CLK inputs.



**AC CHARACTERISTICS** ($T_A$ = 0°C to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.10 | | 1.0 | ns | 0.8 to 2.0V, Note 4. |
| $t_{pw}$ | Output Duty Cycle | $t_{CYCLE}$/2–1000 | | $t_{CYCLE}$/2+1000 | ps | Note 4. |
| $t_{sk(O)}$ | Output–to–Output Skews Same Frequencies | | 200 | 375 | ps | Note 4. |
| | Different Frequencies<br>$Qa_{fmax}$ < 150MHz<br>$Qa_{fmax}$ > 150MHz | | 325 | 500<br>750 | | |
| $f_{VCO}$ | PLL VCO Lock Range | 200 | | 480 | MHz | Note 3. |
| $f_{max}$ | Maximum Output Frequency Qa (÷2)<br>Qa/Qb (÷4)<br>Qb (÷8) | | | 180<br>120<br>60 | MHz | Note 4. |
| $t_{pd}$ | Input to Ext_FB Delay (Note 1.) TCLK<br>PECL_CLK | 50<br>–950 | 250<br>–770 | 400<br>–600 | ps | $f_{ref}$ = 50MHz<br>Feedback=VCO/8<br>Note 4. |
| $t_{PLZ,HZ}$ | Output Disable Time | | | 7 | ns | Note 4. |
| $t_{PZL}$ | Output Enable Time | | | 6 | ns | Note 4. |
| $t_{jitter}$ | Cycle–to–Cycle Jitter (Peak–to–Peak) | | ±100 | | ps | Note 2. |
| $t_{lock}$ | Maximum PLL Lock Time | | | 10 | ms | |

1. The $t_{pd}$ window is specified for a 50Mhz input reference clock. The window will enlarge/reduce proportionally from the minimum limits with an increase/decrease of the input reference clock period. The $t_{pd}$ does not include jitter.
2. See Applications Info section for more jitter information.
3. The PLL will be unstable with a divide by 2 feedback ratio.
4. Termination of 50Ω to $V_{CC}$/2.

## APPLICATIONS INFORMATION

### Programming the MPC951

The MPC951 clock driver outputs can be configured into several frequency relationships. The output dividers for the four output groups allows the user to configure the outputs into 1:1, 2:1, 4:1 and 4:2:1 frequency ratios. The use of even dividers ensures that the output duty cycle is always 50%. Table 1 illustrates the various output configurations, the table describes the outputs using the VCO frequency as a reference. As an example for a 4:2:1 relationship the Qa outputs would be set at VCO/2, the Qb's and Qc's at VCO/4 and the Qd's at VCO/8. These settings will provide output frequencies with a 4:2:1 relationship.

The division settings establish the output relationship, but one must still ensure that the VCO will be stable given the frequency of the outputs desired. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL is such that for output frequencies between 25 and 180MHz the MPC951 can generally be configured into a stable region.

The relationship between the input reference and the output frequency is also very flexible. Table 1 can be used to determine the multiplication factor, there are too many potential combinations to tabularize the external feedback condition. Figure 1 through Figure 2 illustrates several programming possibilities, although not exhaustive it is representative of the potential applications.

### Using the MPC951 as a Zero Delay Buffer

The external feedback of the MPC951 clock driver allows for its use as a zero delay buffer. By using one of the outputs as a feedback to the PLL the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The input reference frequency affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs.

When used as a zero delay buffer the MPC951 will likely be in a nested clock tree application. For these applications the MPC951 offers a LVPECL clock input as a PLL reference. This allows the user to use LVPECL as the primary clock distribution device to take advantage of its far superior skew performance. The MPC951 then can lock onto the LVPECL reference and translate with near zero delay to low skew LVCMOS outputs. Clock trees implemented in this fashion will show significantly tighter skews than trees developed from CMOS fanout buffers.

To minimize part–to–part skew the external feedback option again should be used. The PLL in the MPC951 decouples the delay of the device from the propagation delay variations of the internal gates. From the specification table one sees a Tpd variation of only ±200ps, thus for multiple devices under identical configurations the part–to–part skew will be around 1000ps (350ps for Tpd variation plus 350ps output–to–output skew plus 300ps for I/O jitter). By running the devices at the highest possible input reference, this part–to– part skew can be minimized. Higher input reference frequencies will minimize both I/O jitter and $t_{pd}$ variations.

**Table 1. Programmable Output Frequency Relationships**

| INPUTS | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|
| **fsela** | **fselb** | **fselc** | **fseld** | **Qa** | **Qb** | **Qc** | **Qd** |
| 0 | 0 | 0 | 0 | VCO/2 | VCO/4 | VCO/4 | VCO/4 |
| 0 | 0 | 0 | 1 | VCO/2 | VCO/4 | VCO/4 | VCO/8 |
| 0 | 0 | 1 | 0 | VCO/2 | VCO/4 | VCO/8 | VCO/4 |
| 0 | 0 | 1 | 1 | VCO/2 | VCO/4 | VCO/8 | VCO/8 |
| 0 | 1 | 0 | 0 | VCO/2 | VCO/8 | VCO/4 | VCO/4 |
| 0 | 1 | 0 | 1 | VCO/2 | VCO/8 | VCO/4 | VCO/8 |
| 0 | 1 | 1 | 0 | VCO/2 | VCO/8 | VCO/8 | VCO/4 |
| 0 | 1 | 1 | 1 | VCO/2 | VCO/8 | VCO/8 | VCO/8 |
| 1 | 0 | 0 | 0 | VCO/4 | VCO/4 | VCO/4 | VCO/4 |
| 1 | 0 | 0 | 1 | VCO/4 | VCO/4 | VCO/4 | VCO/8 |
| 1 | 0 | 1 | 0 | VCO/4 | VCO/4 | VCO/8 | VCO/4 |
| 1 | 0 | 1 | 1 | VCO/4 | VCO/4 | VCO/8 | VCO/8 |
| 1 | 1 | 0 | 0 | VCO/4 | VCO/8 | VCO/4 | VCO/4 |
| 1 | 1 | 0 | 1 | VCO/4 | VCO/8 | VCO/4 | VCO/8 |
| 1 | 1 | 1 | 0 | VCO/4 | VCO/8 | VCO/8 | VCO/4 |
| 1 | 1 | 1 | 1 | VCO/4 | VCO/8 | VCO/8 | VCO/8 |

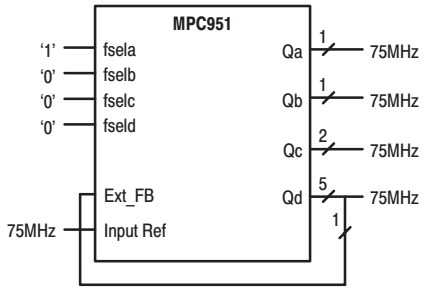



**Figure 1. "Zero" Delay Buffer**

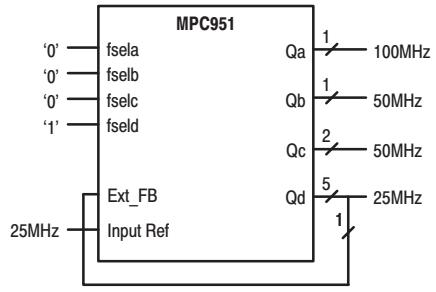



**Figure 2. "Zero" Delay Frequency Multiplier**

### Jitter Performance of the MPC951

With the clock rates of today's digital systems continuing to increase more emphasis is being placed on clock distribution design and management. Among the issues being addressed is system clock jitter and how that affects the overall system timing budget. The MPC951 was designed to minimize clock jitter by employing a differential bipolar PLL as well as incorporating numerous power and ground pins in the design. The following few paragraphs will outline the jitter performance of the MPC951, illustrate the measurement limitations and provide guidelines to minimize the jitter of the device.

The most commonly specified jitter parameter is cycle–to–cycle jitter. Unfortunately with today's high performance measurement equipment there is no way to measure this parameter for jitter performance in the class demonstrated by the MPC951. As a result different methods are used which approximate cycle–to–cycle jitter. The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak–to–peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. If this is not the case the measurement inaccura-

cy will add significantly to the measured jitter. The oscilloscope cannot collect adjacent pulses, rather it collects data from a very large sample of pulses. It is safe to assume that collecting pulse information in this mode will produce jitter values somewhat larger than if consecutive cycles were measured, therefore, this measurement will represent an upper bound of cycle–to–cycle jitter. Most likely, this is a conservative estimate of the cycle–to–cycle jitter.

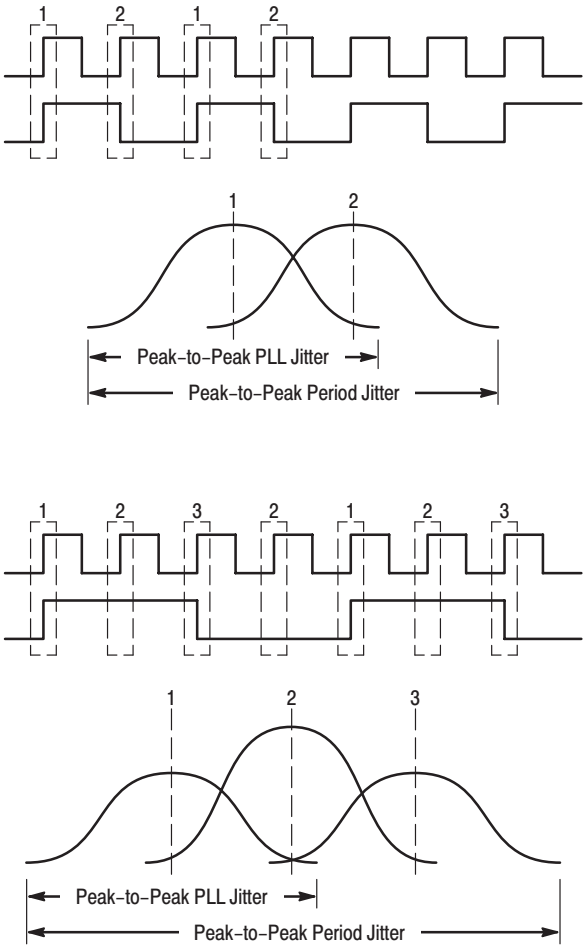
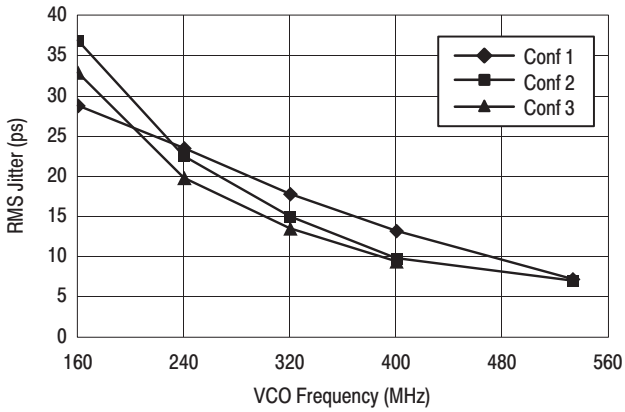



**Figure 3. PLL Jitter and Edge Displacement**

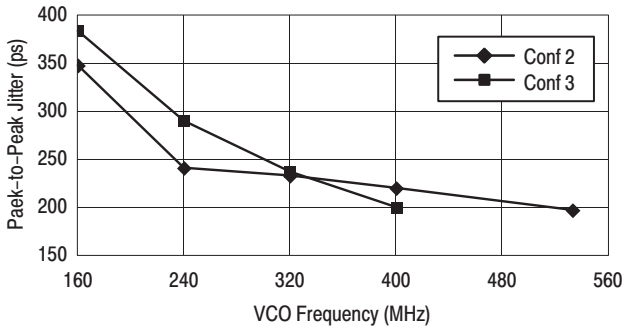
There are two sources of jitter in a PLL based clock driver, the commonly known random jitter of the PLL and the less intuitive jitter caused by synchronous, different frequency outputs switching. For the case where all of the outputs are switching at the same frequency the total jitter is exactly equal to the PLL jitter. In a device, like the MPC951, where a number of the outputs can be switching synchronously but at different frequencies a “multi–modal” jitter distribution can be seen on the highest frequency outputs. Because the output being monitored is affected by the activity on the other outputs it is important to consider what is happening on those other outputs. From Figure 3, one can see for each rising edge on the higher frequency signal the activity on the lower frequency signal is not constant. The activity on the other outputs tends to alter the internal thresholds of the device such that the placement of the edge being monitored is displaced in time. Because the signals are synchronous the relationship is periodic and the resulting jitter is a compilation of the PLL jitter superimposed on the displaced edges. When histograms are plotted the jitter looks like a “multi–modal” distribution as pictured in Figure 3. Depending on the size of the PLL jitter and the relative displacement of the edges the “multi–modal” distribution will appear truly “multi–modal” or simply like a “fat” Gaussian distribution. Again note that in the case where all the outputs are switching at the same frequency there is no edge displacement and the jitter is reduced to that of the PLL.

Figure 4 graphically represents the PLL jitter of the MPC951. The data was taken for several different output configurations. By triggering on the lowest frequency output the PLL jitter can be measured for configurations in which outputs are switching at different frequencies. As one can see in the figure the PLL jitter is much less dependent on output configuration than on internal VCO frequency.




Conf 1 = All Outputs at the Same Frequency
Conf 2 = 4 Outputs at X, 5 Outputs at X/2
Conf 3 = 1 Output at X, 8 Outputs at X/4

**Figure 4. RMS PLL Jitter versus VCO Frequency**




Conf 2 = 4 Outputs at X, 5 Outputs at X/2
Conf 3 = 1 Output at X, 8 Outputs at X/4

**Figure 5. Peak–to–Peak Period Jitter versus VCO Frequency**

Two different configurations were chosen to look at the period displacement caused by the switching outputs. Configuration 3 is considered worst case as the “trimodal” distribution (as pictured in Figure 3) represents the largest spread between distribution peaks. Configuration 2 is considered a typical configuration with half the outputs at a high frequency and the remaining outputs at one half the high frequency. For these cases the peak–to–peak numbers are reported in Figure 5 as

the sigma numbers are useless because the distributions are not Gaussian. For situations where the outputs are synchronous and switching at different frequencies the measurement technique described here is insufficient to use for establishing guaranteed limits. Other techniques are currently being investigated to identify a more accurate and repeatable measurement so that guaranteed limits can be provided. The data generated does give a good indication of the general performance, a performance that in most cases is well within the requirements of today's microprocessors.

Finally from the data there are some general guidelines that, if followed, will minimize the output jitter of the device. First and foremost always configure the device such that the VCO runs as fast as possible. This is by far the most critical parameter in minimizing jitter. Second keep the reference frequency as high as possible. More frequent updates at the phase detector will help to reduce jitter. Note that if there is a tradeoff between higher reference frequencies and higher VCO frequency always chose the higher VCO frequency to minimize jitter. The third guideline may be the most difficult, and in some cases impossible, to follow. Try to minimize the number of different frequencies sourced from a single chip. The fixed edge displacement associated with the switching noise in most cases nearly doubles the "effective" jitter of a high speed output.

**Power Supply Filtering**

The MPC951 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC951 provides separate power supplies for the output buffers (VCCO) and the phase–locked loop (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC951.

Figure 6 illustrates a typical power supply filter scheme. The MPC951 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the VCCA pin of the MPC951. From the data sheet the $I_{VCCA}$ current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V $V_{CC}$ supply is used. The resistor shown in Figure 6 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8–10Ω resistor to avoid potential $V_{CC}$ drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

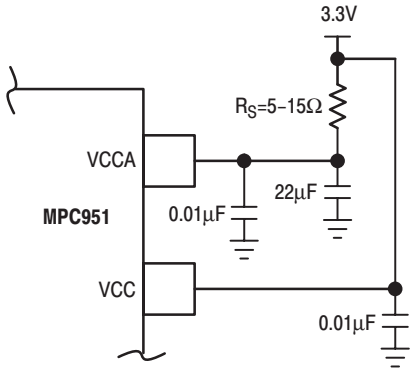



**Figure 6. Power Supply Filter**

Although the MPC951 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Driving Transmission Lines**

The MPC951 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC951 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 7 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC951 clock driver is effectively doubled due to its capability to drive multiple lines.

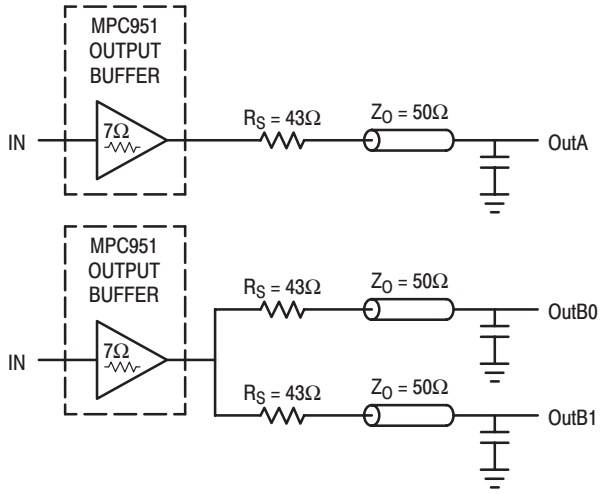



**Figure 7. Single versus Dual Transmission Lines**

The waveform plots of Figure 8 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC951 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC951. The output waveform in Figure 8 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS ( Zo / (Rs + Ro + Zo))$$

$Zo = 50\Omega \parallel 50\Omega$
$Rs = 43\Omega \parallel 43\Omega$
$Ro = 7\Omega$

$$VL = 3.0 (25 / (21.5 + 7 + 25) = 3.0 (25 / 53.5)$$
$$= 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

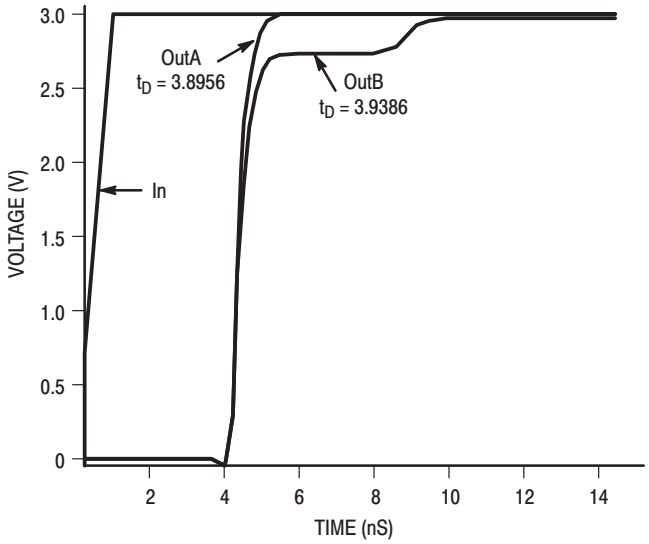



**Figure 8. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 9 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

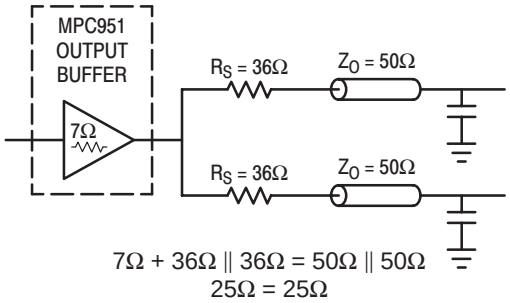



**Figure 9. Optimized Dual Line Termination**

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

# Low Voltage PLL Clock Driver

**MPC952**

**See Upgrade Product – MPC9352**

**LOW VOLTAGE PLL CLOCK DRIVER**

**FA SUFFIX**
LQFP PACKAGE
CASE 873A-02

2

The MPC952 is a 3.3V compatible, PLL based clock driver device targeted for high performance clock tree applications. The device features a fully integrated PLL with no external components required. With output frequencies of up to 180MHz and eleven low skew outputs the MPC952 is well suited for high performance designs. The device employs a fully differential PLL design to optimize jitter and noise rejection performance. Jitter is an increasingly important parameter as more microprocessors and ASiC's are employing on chip PLL clock distribution.

- Fully Integrated PLL
- Output Frequency up to 180MHz
- High Impedance Disabled Outputs
- Compatible with **PowerPC**™, Intel and High Performance RISC Microprocessors
- Output Frequency Configurable
- LQFP Packaging
- ±100ps Cycle–to–Cycle Jitter

The MPC952 features three banks of individually configurable outputs. The banks contain 5 outputs, 4 outputs and 2 outputs. The internal divide circuitry allows for output frequency ratios of 1:1, 2:1, 3:1 and 3:2:1. The output frequency relationship is controlled by the fsel frequency control pins. The fsel pins as well as the other inputs are LVCMOS/LVTTL compatible inputs.

The MPC952 uses external feedback to the PLL. This features allows for the use of the device as a "zero delay" buffer. Any of the eleven outputs can be used as the feedback to the PLL. The VCO_Sel pin allows for the choice of two VCO ranges to optimize PLL stability and jitter performance. The MR/$\overline{OE}$ pin allows the user to force the outputs into high impedance for board level test.

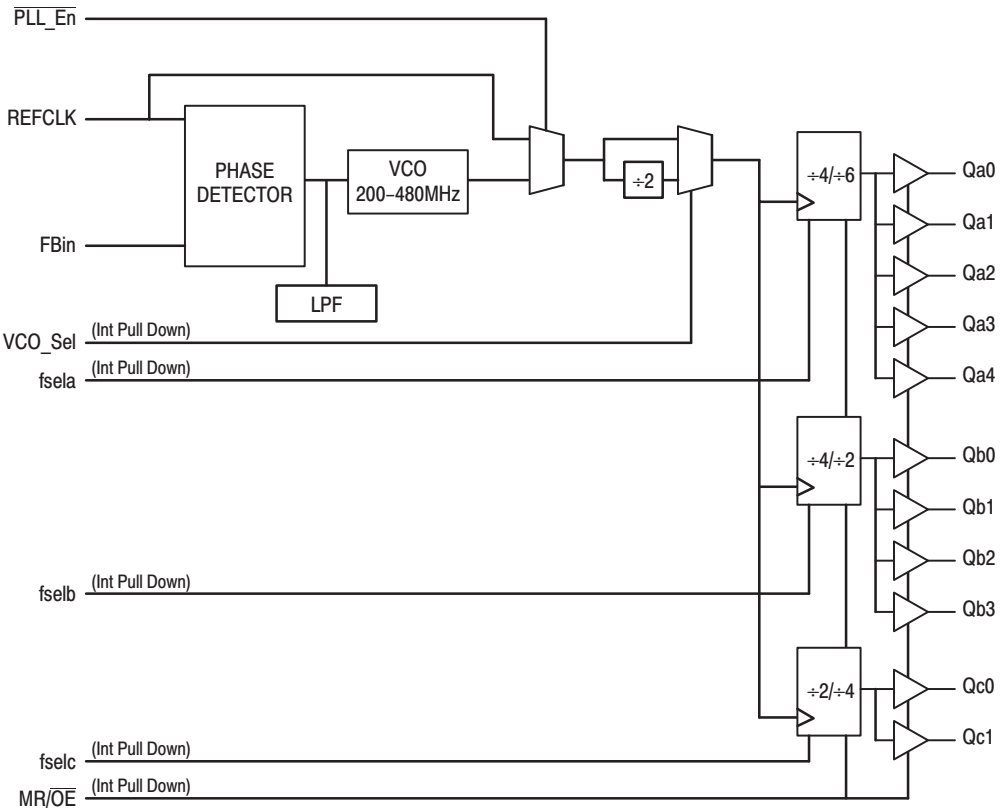
For system debug the PLL of the MPC952 can be bypassed. When forced to a logic HIGH, the PLLEN input will route the signal on the RefClk input around the PLL directly to the internal dividers. Because the signal is routed through the dividers, it may take several transitions of the RefClk to affect a transition on the outputs. This features allows a designer to single step the design for debug purposes.

The outputs of the MPC952 are LVCMOS outputs. The outputs are optimally designed to drive terminated transmission lines. For applications using series terminated transmission lines each MPC952 output can drive two lines. This capability provides an effective fanout of 22, more than enough clocks for most clock tree designs. For more information on driving transmission lines consult the applications section of this data sheet.



**Rev 5**

**Figure 1. MPC952 Logic Diagram**



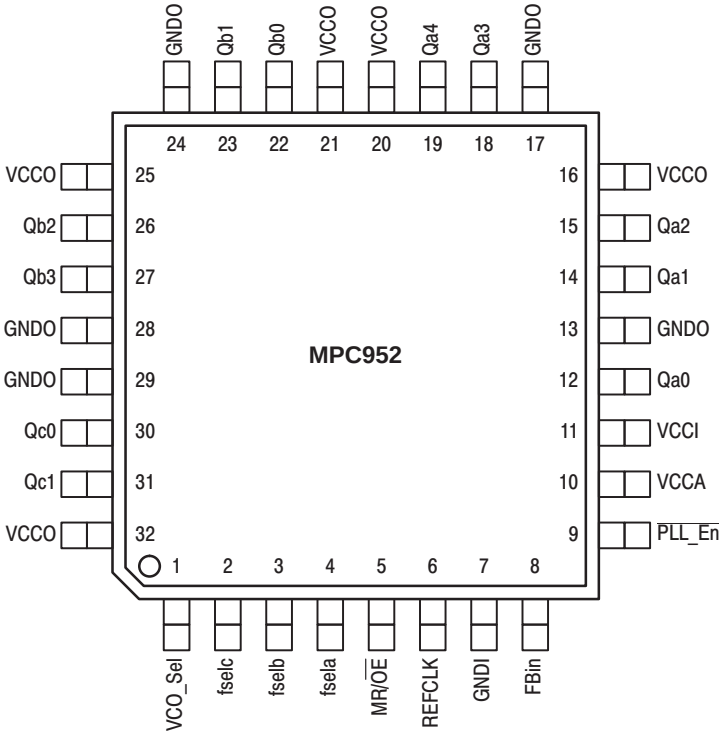




**Figure 2. 32–Lead Pinout** (Top View)

**FUNCTION TABLES**

| fsela | Qan | fselb | Qbn | fselc | Qcn |
|---|---|---|---|---|---|
| 0 | ÷4 | 0 | ÷4 | 0 | ÷2 |
| 1 | ÷6 | 1 | ÷2 | 1 | ÷4 |

| Control Pin | Logic ‘0’ | Logic ‘1’ |
|---|---|---|
| VCO_Sel | fVCO | fVCO/2 |
| MR/$\overline{OE}$ | Output Enable | High Z |
| $\overline{PLL\_En}$ | Enable PLL | Disable PLL |

| Pin Name | Description |
|---|---|
| VCCA | PLL Power Supply |
| VCCO | Output Buffer Power Supply |
| VCCI | Internal Core Logic Power Supply |
| GNDI | Internal Ground |
| GNDO | Output Buffer Ground |

**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 4.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | Input Current | | ±20 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

2

**THERMAL CHARACTERISTICS**

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CCO}$ = $V_{CCI}$ = $V_{CCA}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | 3.6 | V | |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | $I_{OH}$ = –20mA (Note 1.) |
| $V_{OL}$ | Output LOW Voltage | | | 0.5 | V | $I_{OL}$ = 20mA (Note 1.) |
| $I_{IN}$ | Input Current | | | ±120 | µA | Note 2. |
| $C_{IN}$ | Input Capacitance | | 2.7 | 4.0 | pF | |
| $C_{pd}$ | Power Dissipation Capacitance | | 25 | | pF | |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | 160 | mA | Total ICC Static Current |
| $I_{CCA}$ | PLL Supply Current | | 15 | 20 | mA | |

1. The MPC952 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CCO}$/2) transmission lines on the incident edge (see Applications Info section).
2. Inputs have pull–up, pull–down resistors which affect input current.

**PLL INPUT REFERENCE CHARACTERISTICS** ($T_A$ = 0 to 70°C)

| Symbol | Characteristic | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $t_r$, $t_f$ | TCLK Input Rise/Falls | | 3.0 | ns | |
| $f_{ref}$ | Reference Input Frequency | | 100 | MHz | Note 3. |
| $f_{refDC}$ | Reference Input Duty Cycle | 25 | 75 | % | |

3. Maximum and minimum input reference is limited by the VCO lock range and the feedback divider.

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CCO}$ = $V_{CCI}$ = $V_{CCA}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $t_r$, $t_f$ | Output Rise/Fall Time (Note 4.) | 0.10 | | 1.0 | ns | 0.8 to 2.0V |
| $t_{pw}$ | Output Pulse Width (Note 4.) | $t_{CYCLE}$/2 –750 | $t_{CYCLE}$/2 ±500 | $t_{CYCLE}$/2 +750 | ps | |
| $t_{os}$ | Output-to-Output Skew (Note 4.) Excluding Qa0<br>All Outputs<br>All Outputs | | | 350<br>450<br>550 | ps | Same Frequencies<br>Same Frequencies<br>Different Frequencies |
| $f_{VCO}$ | PLL VCO Lock Range | 200 | | 480 | MHz | Note 6. |
| $f_{max}$ | Maximum Output Frequency Qc,Qb (÷2)<br>Qa,Qb,Qc (÷4)<br>Qa (÷6) | 180<br>120<br>80 | | | MHz | Note 4. |
| $t_{pd}$ | REFCLK to FBIN Delay | –200 | 0 | 200 | ps | Notes 4., 5. |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time | 2 | | 8 | ns | Note 4. |
| $t_{PZL}$, $t_{PLH}$ | Output Enable Time | 2 | | 10 | ns | Note 4. |
| $t_{jit(cc)}$ | Cycle–to–Cycle Jitter | | ±100 | | ps | |
| $t_{lock}$ | Maximum PLL Lock Time | | | 10 | ms | |

4. Termination of 50Ω to $V_{CCO}$/2.
5. $t_{pd}$ is specified for 50MHz input ref, the window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The $t_{pd}$ does not include jitter.
6. The PLL may be unstable with a divide by 2 feedback ratio.

## APPLICATIONS INFORMATION

### Driving Transmission Lines

The MPC952 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 7Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091.

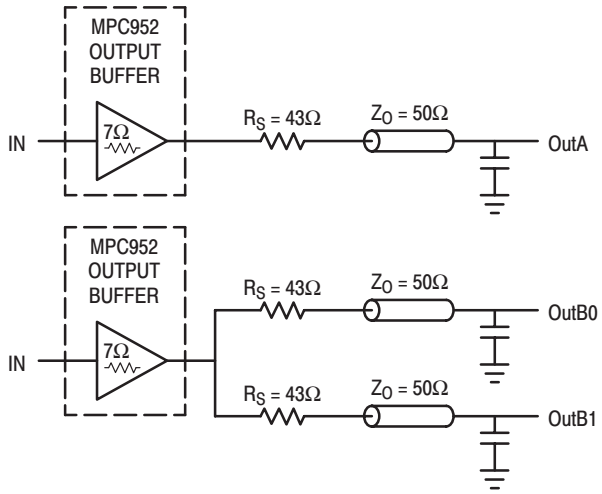



**Figure 3. Single versus Dual Transmission Lines**

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CCO}$/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC952 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC952 clock driver is effectively doubled due to its capability to drive multiple lines.

The waveform plots of Figure 4 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC952 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC952. The output waveform in Figure 4 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS (Zo / Rs + Ro + Zo) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

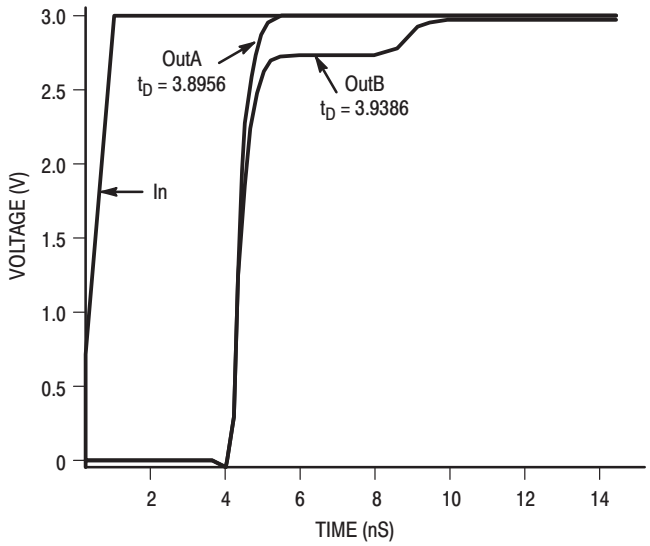
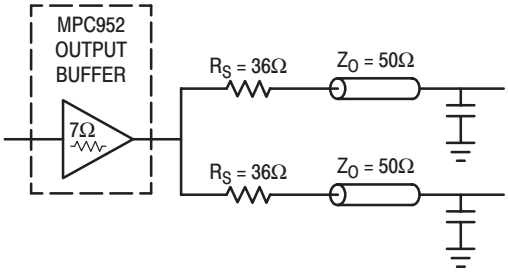



**Figure 4. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




$7\Omega + 36\Omega \parallel 36\Omega = 50\Omega \parallel 50\Omega$
$25\Omega = 25\Omega$

**Figure 5. Optimized Dual Line Termination**

### Power Supply Filtering

The MPC952 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC952 provides separate power supplies for the output buffers ($V_{CCO}$) and the internal PLL (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC952.

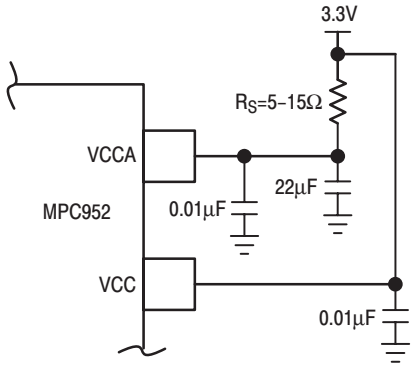



**Figure 6. Power Supply Filter**

Figure 6 illustrates a typical power supply filter scheme. The MPC952 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the VCCA pin of the MPC952. From the data sheet the $I_{VCCA}$ current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.3V – 5% must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V $V_{CC}$ supply is used. The resistor shown in Figure 6 must have a resistance of 5–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

Although the MPC952 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Order Number: MPC9600/D**
**Rev. 2, 11/2001**

# Low Voltage 2.5 V and 3.3 V CMOS PLL Clock Driver

**MPC9600**

**3.3 V OR 2.5 V LOW VOLTAGE CMOS PLL CLOCK DRIVER**

**FA SUFFIX**
48–LEAD LQFP PACKAGE
CASE 932–03

2

The MPC9600 is a low voltage 2.5 V or 3.3 V compatible, 1:21 PLL based clock driver and fanout buffer. With output frequencies up to 200 MHz and output skews of 150 ps, the device meets the needs of the most demanding clock tree applications.

**Features:**

- Multiplication of input frequency by 2, 3, 4 and 6
- Distribution of output frequency to 21 outputs organized in three output banks: QA0-QA6, QB0-QB6, QC0-QC6, each fully selectable
- Fully integrated PLL
- Selectable output frequency range is 50 to 100 MHz and 100 to 200 MHz
- Selectable input frequency range is 16.67 to 33 MHz and 25 to 50 MHz
- LVCMOS outputs
- Outputs disable to high impedance (except QFB)
- LVCMOS or LVPECL reference clock options
- 48 lead QFP packaging
- ±50 ps cycle-to-cycle jitter
- 150 ps maximum output-to-output skew
- 200 ps maximum static phase offset window

The MPC9600 is a fully LVCMOS 2.5 V or 3.3 V compatible PLL clock driver. The MPC9600 has the capability to generate clock signals of 50 to 200 MHz from clock sources of 16.67 to 50 MHz. The internal PLL is optimized for this frequency range and does not require external loop filter components. QFB provides an output for the external feedback path to the feedback input FB_IN. The QFB divider ratio is configurable and determines the PLL frequency multiplication factor when QFB is directly connected to FB_IN. The MPC9600 is optimized for minimizing the propagation delay between the clock input and FB_IN.

Three output banks of 7 outputs each bank can be individually configured to divide the VCO frequency by 2 or by 4. Combining the feedback and output divider ratios, the MPC9600 is capable to multiply the input frequency by 2, 3, 4 and 6.

The reference clock is selectable either LVPECL or LVCMOS. The LVPECL reference clock feature allows the designer to use LVPECL fanout buffers for the inner branches of the clock distribution tree. All control inputs accept LVCMOS compatible levels. The outputs provide low impedance LVCMOS outputs capable of driving parallel terminated 50 Ω transmission to $V_{TT}=V_{CC}/2$. For series terminated lines the MPC9600 can drive two lines per output giving the device an effective total fanout of 1:42. With guaranteed maximum output-to-output skew of 150 ps, the MPC9600 PLL clock driver meets the synchronization requirements of the most demanding systems.

The $V_{CCA}$ analog power pin doubles as a PLL bypass select line for test purpose. When the $V_{CCA}$ is driven to GND the reference clock will bypass the PLL.

The device is packaged in a 48-lead LQFP package to provide optimum combination of board density and performance.

**Rev 2**

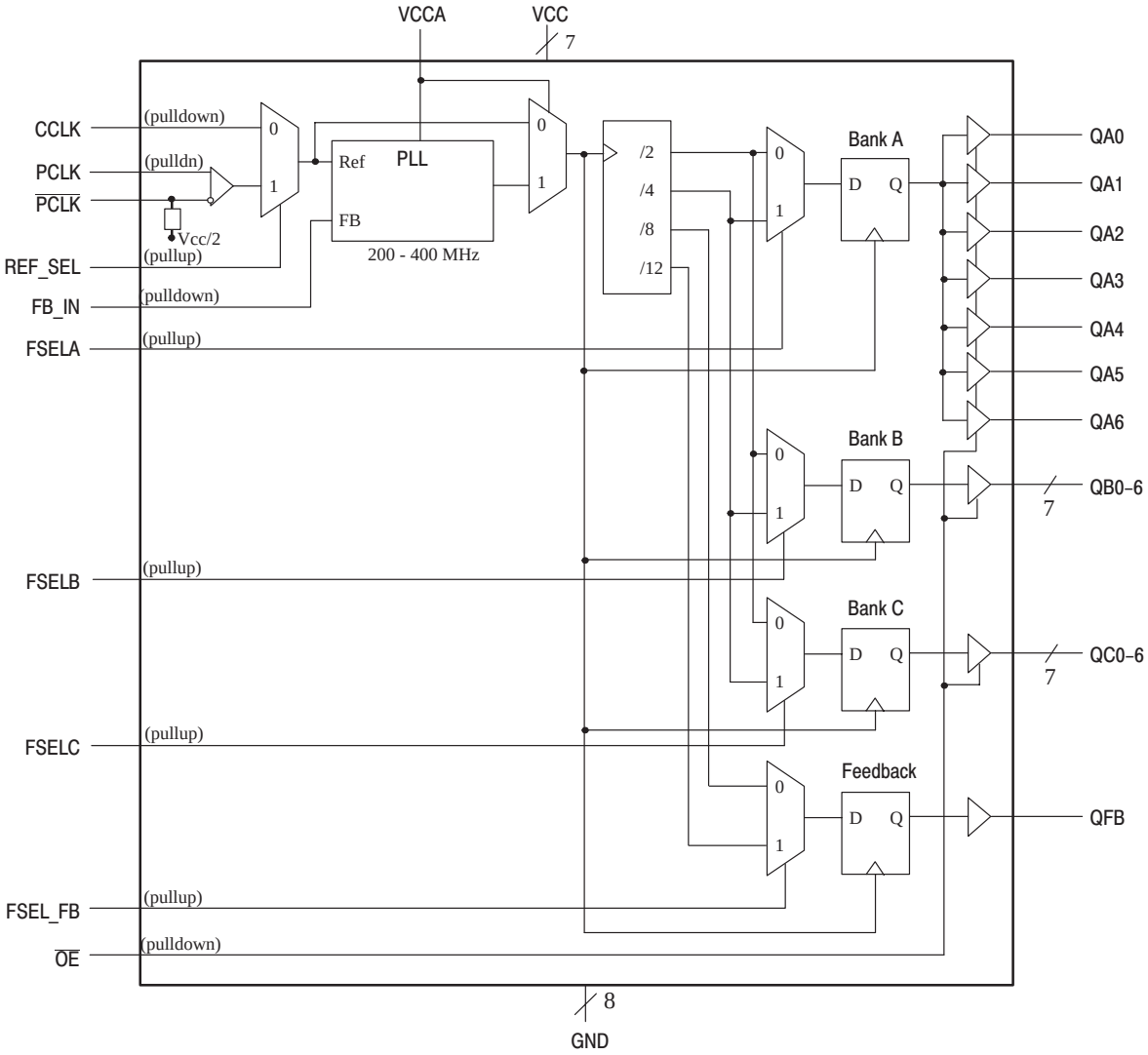



**Figure 1. MPC9600 Logic Diagram**

**PIN CONFIGURATION**

| Pin | I/O | Type | Description |
|---|---|---|---|
| PCLK, $\overline{\text{PCLK}}$ | Input | PECL | Differential reference clock frequency input |
| CCLK | Input | LVCMOS | Reference clock input |
| FB_IN | Input | LVCMOS | PLL feedback clock input |
| QAn | Output | LVCMOS | Bank A outputs |
| QBn | Output | LVCMOS | Bank B outputs |
| QCn | Output | LVCMOS | Bank C outputs |
| QFB | Output | LVCMOS | Differential feedback output |
| REF_SEL | Input | LVCMOS | Reference clock input select |
| FSELA | Input | LVCMOS | Selection of bank A output frequency |
| FSELB | Input | LVCMOS | Selection of bank B output frequency |
| FSELC | Input | LVCMOS | Selection of bank C output frequency |
| FSEL_FB | Input | LVCMOS | Selection of feedback frequency |
| $\overline{\text{OE}}$ | Input | LVCMOS | Output enable |
| VCCA | | Power supply | Analog power supply and PLL bypass. An external VCC filter is recommended for VCCA |
| VCC | | Power supply | Core power supply |
| GND | | Ground | Ground |

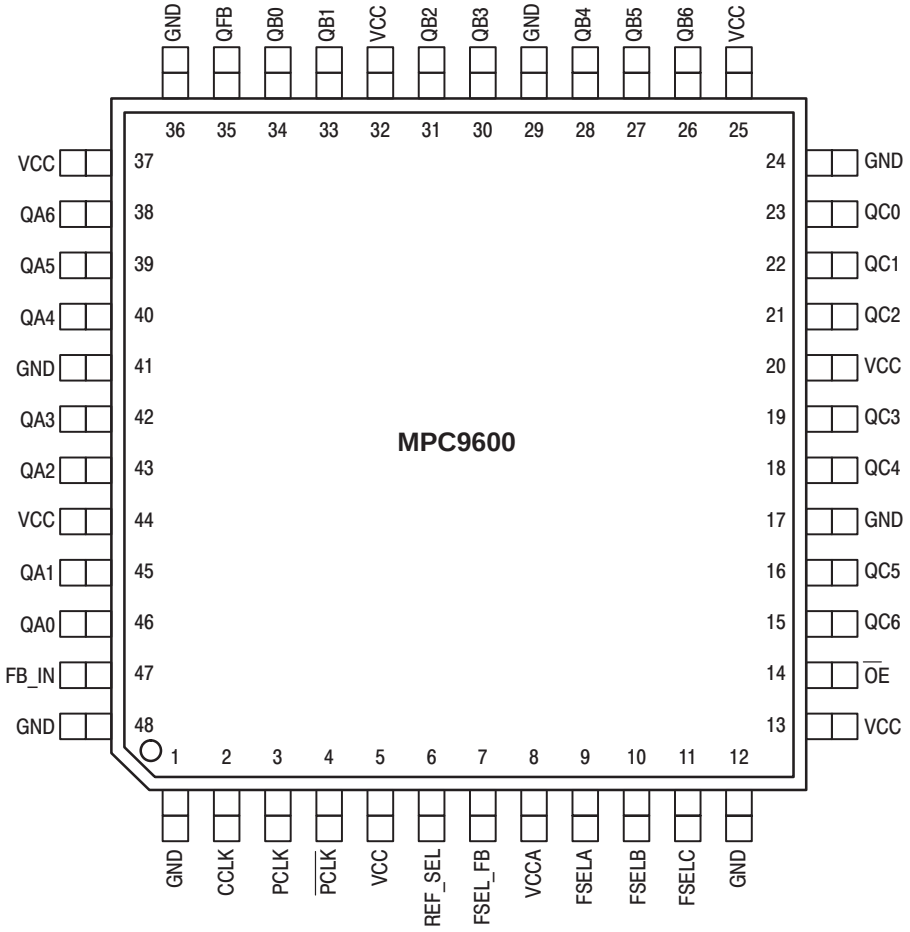



**Figure 2. 48 Lead Package Pinout** (Top View)

**FUNCTION TABLE (CONTROLS)**

| Control Pin | 0 | 1 |
|---|---|---|
| REF_SEL | CCLK | PCLK |
| VCCA | PLL Bypass[1] | PLL Power |
| OE | Outputs Enabled | Outputs Disabled (except QFB) |
| FSELA | Output Bank A at VCO/2 | Output Bank A at VCO/4 |
| FSELB | Output Bank B at VCO/2 | Output Bank B at VCO/4 |
| FSELC | Output Bank C at VCO/2 | Output Bank C at VCO/4 |
| FSEL_FB | Feedback Output at VCO/8 | Feedback Output at VCO/12 |

1. $V_{CCA}$ = GND, PLL off and bypassed for static test and diagnosis



**Table 1: ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 4.6 | V |
| $V_{IN}$ | DC Input Voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $V_{OUT}$ | DC Output Voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | DC Input Current | | ±20 | mA |
| $I_{OUT}$ | DC Output Current | | ±50 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

**Table 2: GENERAL SPECIFICATIONS**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output Termination Voltage | | $V_{CC}$ ÷ 2 | | V | |
| MM | ESD Protection (Machine Model) | 400 | | | V | |
| HBM | ESD Protection (Human Body Model) | 4000 | | | V | |
| CDM | ESD Protection (Charged Device Model) | 1500 | | | V | |
| LU | Latch–Up Immunity | 200 | | | mA | |
| $C_{PD}$ | Power Dissipation Capacitance | | 10 | | pF | Per output |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | Inputs |

**Table 3: DC CHARACTERISTICS** ($V_{CC}$ = 3.3 V ±5%, $T_A$ = –40° to +85°C)

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | | | | 0.8 | V | LVCMOS |
| $V_{PP}$ | Peak-to-peak Input Voltage (DC) | PCLK, $\overline{PCLK}$ | 250 | | | mV | LVPECL |
| $V_{CMR}$[a] | Common Mode Range (DC) | PCLK, $\overline{PCLK}$ | 1.0 | | $V_{CC}$-0.6 | V | LVPECL |
| $V_{OH}$ | Output High Voltage | | 2.4 | | | V | $I_{OH}$=-24 mA[b] |
| $V_{OL}$ | Output Low Voltage | | | | 0.55<br>0.30 | V<br>V | $I_{OL}$= 24mA<br>$I_{OL}$= 12mA |
| $Z_{OUT}$ | Output Impedance | | | 14 – 17 | | Ω | |
| $I_{IN}$ | Input Leakage Current | | | | ±150 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CCA}$ | Maximum PLL Supply Current | | | 2.0 | 5.0 | mA | $V_{CCA}$ Pin |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | | 1.0 | mA | All $V_{CC}$ Pins |

a. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (DC) specification.

b. The MPC9600 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

**Table 4: DC CHARACTERISTICS** ($V_{CC}$ = 2.5 V ±5%, $T_A$ = –40° to +85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | | | 0.7 | V | LVCMOS |
| $V_{PP}$ | Peak-to-peak input voltage (DC) PCLK, $\overline{PCLK}$ | 250 | | | mV | LVPECL |
| $V_{CMR}$[a] | Common Mode Range (DC) PCLK, $\overline{PCLK}$ | 1.0 | | $V_{CC}$-0.6 | V | LVPECL |
| $V_{OH}$ | Output High Voltage | 1.8 | | | V | $I_{OH}$=-15 mA[b] |
| $V_{OL}$ | Output Low Voltage | | | 0.6 | V | $I_{OL}$= 15 mA |
| $Z_{OUT}$ | Output Impedance | | 17 – 20 | | Ω | |
| $I_{IN}$ | Input Leakage Current | | | ±150 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CCA}$ | Maximum PLL Supply Current | | 3.0 | 5.0 | mA | $V_{CCA}$ Pin |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (DC) specification.
b. The MPC9600 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50 Ω series terminated transmission lines per output.

**Table 5: AC CHARACTERISTICS** ($V_{CC}$ = 3.3 V ±5% or $V_{CC}$ = 2.5 V ±5%, $T_A$ = –40° to +85°C)[a]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency | | | | | |
| | ÷8 feedback (FSEL_FB=0) | 25 | | 50 | MHz | PLL locked |
| | ÷12 feedback (FSEL_FB=1) | 16.67 | | 33 | MHz | PLL locked |
| | Static test mode (VCCA = GND) | 0 | | 500 | MHz | VCCA = GND |
| $f_{VCO}$ | VCO Frequency | 200 | | 400 | MHz | |
| $f_{MAX}$ | Maximum Output Frequency | | | | | |
| | ÷2 outputs (FSELx=0) | 100 | | 200 | MHz | PLL locked |
| | ÷4 outputs (FSELx=1) | 50 | | 100 | MHz | PLL locked |
| $f_{refDC}$ | Reference Input Duty Cycle | 25 | | 75 | % | |
| $V_{PP}$ | Peak-to-peak Input Voltage PCLK, $\overline{PCLK}$ | 500 | | 1000 | mV | LVPECL |
| $V_{CMR}$b | Common Mode Range | | | | | |
| | PCLK, $\overline{PCLK}$ (VCC = 3.3 V ±5%) | 1.2 | | $V_{CC}$-0.8 | V | LVPECL |
| | PCLK, $\overline{PCLK}$ (VCC = 2.5 V ±5%) | 1.2 | | $V_{CC}$-0.6 | V | LVPECL |
| $t_r$, $t_f$ | CCLK Input Rise/Fall Time | | | 1.0 | ns | see Figure 12 |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) | | | | | |
| | CCLK to FB_IN | –60 | +40 | +140 | ps | PLL locked |
| | PECL_CLK to FB_IN | +30 | +130 | +230 | ps | PLL locked |
| $t_{sk(o)}$ | Output-to-output Skew | | | | | |
| | all outputs, single frequency | | 70 | 150 | ps | Measured at |
| | all outputs, multiple frequency | | 70 | 150 | ps | coincident rising edge |
| | within QAx output bank | | 30 | 75 | ps | |
| | within QBx outputs | | 40 | 125 | ps | |
| | within QCx outputs | | 30 | 75 | ps | |
| DC | Output Duty Cycle | 45 | 50 | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.1 | | 1.0 | ns | see Figure 12 |
| $t_{PLZ, HZ}$ | Output Disable Time | | | 10 | ns | |
| $t_{PZL, ZH}$ | Output Enable Time | | | 10 | ns | |
| BW | PLL Closed Loop Bandwidth | | | | | –3 dB point of |
| | ÷8 feedback (FSEL_FB=0) | | 1.0 – 10 | | MHz | PLL transfer |
| | ÷12 feedback (FSEL_FB=1) | | 0.6 – 4.0 | | MHz | characteristic |

**Table 5: AC CHARACTERISTICS** ($V_{CC}$ = 3.3 V ±5% or $V_{CC}$ = 2.5 V ±5%, $T_A$ = –40° to +85°C)[a]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $t_{JIT(CC)}$ | Cycle-to-cycle Jitter[c]<br>All outputs in ÷2 configuration<br>All outputs in ÷4 configuration | | <br>40<br>40 | <br>130<br>180 | <br>ps<br>ps | See application section for other configurations |
| $t_{JIT(PER)}$ | Period Jitter[c]<br>All outputs in ÷2 configuration<br>All outputs in ÷4 configuration | | <br>25<br>20 | <br>70<br>100 | <br>ps<br>ps | See application section for other configurations |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter (1 σ) $V_{CC}$ = 3.3V<br>$V_{CC}$ = 2.5V | | | 17[d]<br>15[c] | ps<br>ps | RMS value at $f_{VCO}$=400MHz |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 5.0 | ms | |

a. AC characteristics are applicable over the entire ambient temperature and supply voltage range and are production tested. AC characteristics apply for parallel output termination of 50 Ω to $V_{TT}$.
b. $V_{CMR}$ (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ or $V_{PP}$ impacts static phase offset $t_{(\varnothing)}$.
c. Cycle–to–cycle and period jitter depends on output divider configuration.
d. See applications section for max I/O phase jitter versus frequency.

## APPLICATIONS INFORMATION

### Programming the MPC9600

The MPC9600 clock driver outputs can be configured into several divider modes. Additionally the external feedback of the device allows for flexibility in establishing various input to output frequency relationships. The selectable feedback divider of the three output groups allows the user to configure the device for 1:2, 1:3, 1:4 and 1:6 input:output frequency ratios. The use of even dividers ensure that the output duty cycle is always 50%. Table 6 illustrates the various output configurations, the table describes the outputs using the input clock frequency CLK as a reference.

The feedback divider division settings establish the output relationship, in addition, it must be ensured that the VCO will be stable given the frequency of the outputs desired. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL supports output frequencies from 50 MHz to 200 MHz while the VCO frequency range is specified from 200 MHz to 400 MHz and should not be exceeded for stable operation.

**Table 6: Output Frequency Relationship[a] for QFB connected to FB_IN**

| Configuration Inputs | | | | Input Frequency Range CLK [MHz] | Output Frequency Ratio and Range | | |
|---|---|---|---|---|---|---|---|
| FSEL_FB | FSELA | FSELB | FSELC | | Ratio, QAx [MHz] | Ratio, QBx [MHz] | Ratio, QCx [MHz] |
| 0 | 0 | 0 | 0 | 25.0–50.0 | 4•CLK (100–200) | 4•CLK (100–200) | 4•CLK (100–200) |
| 0 | 0 | 0 | 1 | | 4•CLK (100–200) | 4•CLK (100–200) | 2•CLK (50.0–100) |
| 0 | 0 | 1 | 0 | | 4•CLK (100–200) | 2•CLK (50.0–100) | 4•CLK (100–200) |
| 0 | 0 | 1 | 1 | | 4•CLK (100–200) | 2•CLK (50.0–100) | 2•CLK (50.0–100) |
| 0 | 1 | 0 | 0 | | 2•CLK (50.0–100) | 4•CLK (100–200) | 4•CLK (100–200) |
| 0 | 1 | 0 | 1 | | 2•CLK (50.0–100) | 4•CLK (100–200) | 2•CLK (50.0–100) |
| 0 | 1 | 1 | 0 | | 2•CLK (50.0–100) | 2•CLK (50.0–100) | 4•CLK (100–200) |
| 0 | 1 | 1 | 1 | | 2•CLK (50.0–100) | 2•CLK (50.0–100) | 2•CLK (50.0–100) |
| 1 | 0 | 0 | 0 | 16.67–33.33 | 6•CLK (100–200) | 6•CLK (100–200) | 6•CLK (100–200) |
| 1 | 0 | 0 | 1 | | 6•CLK (100–200) | 6•CLK (100–200) | 3•CLK (50.0–100) |
| 1 | 0 | 1 | 0 | | 6•CLK (100–200) | 3•CLK (50.0–100) | 6•CLK (100–200) |
| 1 | 0 | 1 | 1 | | 6•CLK (100–200) | 3•CLK (50.0–100) | 3•CLK (50.0–100) |
| 1 | 1 | 0 | 0 | | 3•CLK (50.0–100) | 6•CLK (100–200) | 6•CLK (100–200) |
| 1 | 1 | 0 | 1 | | 3•CLK (50.0–100) | 6•CLK (100–200) | 3•CLK (50.0–100) |
| 1 | 1 | 1 | 0 | | 3•CLK (50.0–100) | 3•CLK (50.0–100) | 6•CLK (100–200) |
| 1 | 1 | 1 | 1 | | 3•CLK (50.0–100) | 3•CLK (50.0–100) | 3•CLK (50.0–100) |

a. Output frequency relationship with respect to input reference frequency CLK. The VCO frequency range is always 200–400.

### Typical and Maximum Period Jitter Specification

| Device Configuration | QA0 to QA6 | | QB0 to QB6 | | QC0 to QC6 | |
|---|---|---|---|---|---|---|
| | Typ | Max | Typ | Max | Typ | Max |
| All output banks in ÷2 or ÷4 divider configuration[a] | | | | | | |
| ÷2 (FSELA=0 and FESLB=0 and FSELC=0) | 25 | 50 | 50 | 70 | 25 | 50 |
| ÷4 (FSELA=1 and FESLB=1 and FSELC=1) | 20 | 70 | 50 | 100 | 20 | 70 |
| Mixed ÷2/÷4 divider configurations[b] | | | | | | |
| for output banks in ÷2 divider configurations | 80 | 130 | 100 | 150 | 80 | 130 |
| for output banks in ÷4 divider configurations | 25 | 70 | 60 | 100 | 25 | 70 |

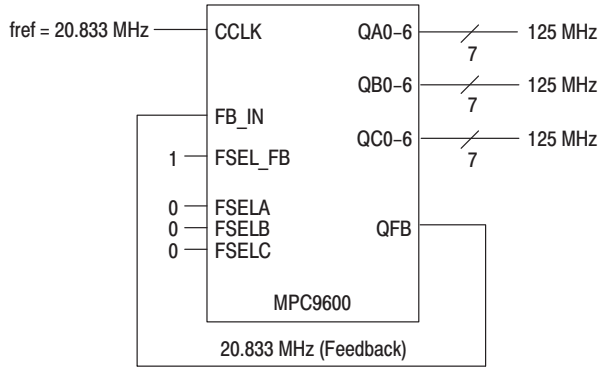
a. In this configuration, all MPC9600 outputs generate the same clock frequency. See Figure 1 for an example configuration.
b. Multiple frequency generation. Jitter data are specified for each output divider sepeerately. See Figure 2 for an example.

### Typical and Maximum Cycle–to–cycle Jitter Specification

| Device Configuration | QA0 to QA6 | | QB0 to QB6 | | QC0 to QC6 | |
|---|---|---|---|---|---|---|
| | Typ | Max | Typ | Max | Typ | Max |
| All output banks in ÷2 or ÷4 divider configuration[a] | | | | | | |
| ÷2 (FSELA=0 and FESLB=0 and FSELC=0) | 40 | 90 | 80 | 130 | 40 | 90 |
| ÷4 (FSELA=1 and FESLB=1 and FSELC=1) | 40 | 110 | 120 | 180 | 40 | 110 |
| Mixed ÷2/÷4 divider configurations[b] | | | | | | |
| for output banks in ÷2 divider configurations | 150 | 250 | 200 | 280 | 150 | 250 |
| for output banks in ÷4 divider configurations | 30 | 110 | 120 | 180 | 30 | 110 |

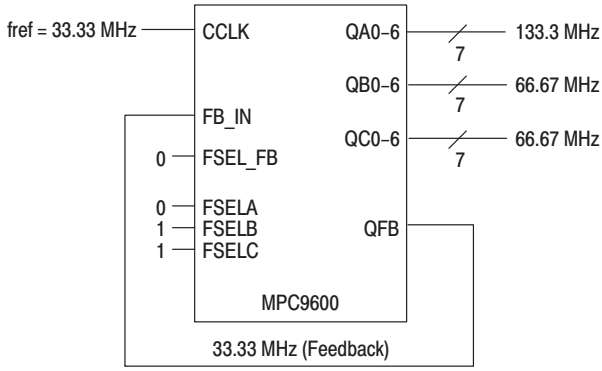
a. In this configuration, all MPC9600 outputs generate the same clock frequency.
b. Multiple frequency generation. Jitter data are specified for each output divider sepeerately.

**Figure 3. Configuration for 125 MHz clocks**




| Frequency range | Min | Max |
|---|---|---|
| Input | 16.67 MHz | 33.33 MHz |
| QA outputs | 100 MHz | 200 MHz |
| QB outputs | 100 MHz | 200 MHz |
| QC outputs | 100 MHz | 200 MHz |

**Figure 4. Configuration for 133.3/66.67 MHz clocks**




| Frequency range | Min | Max |
|---|---|---|
| Input | 25 MHz | 50 MHz |
| QA outputs | 100 MHz | 200 MHz |
| QB outputs | 100 MHz | 200 MHz |
| QC outputs | 100 MHz | 200 MHz |

**Power Supply Filtering**

The MPC9600 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the $V_{CCA}$ (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC9600 provides separate power supplies for the output buffers ($V_{CC}$) and the phase-locked loop ($V_{CCA}$) of the device.The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the $V_{CCA}$ pin for the MPC9600. Figure 5 illustrates a typical power supply filter scheme. The MPC9600 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor $R_F$. From the data sheet the $I_{CCA}$ current (the current sourced through the $V_{CCA}$ pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325 V ($V_{CC}$=3.3 V or $V_{CC}$=2.5 V) must be maintained on the $V_{CCA}$ pin. The resistor $R_F$ shown in Figure 5 "$V_{CCA}$ Power Supply Filter" must have a resistance of 9-10 Ω ($V_{CC}$=2.5 V) to meet the voltage drop criteria.

The minimum values for $R_F$ and the filter capacitor $C_F$ are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 5 "$V_{CCA}$ Power Supply Filter", the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

$R_F$ = 9–10 Ω for $V_{CC}$ = 2.5 V or $V_{CC}$ = 3.3 V
$C_F$ = 22 μF for $V_{CC}$ = 2.5 V or $V_{CC}$ = 3.3 V

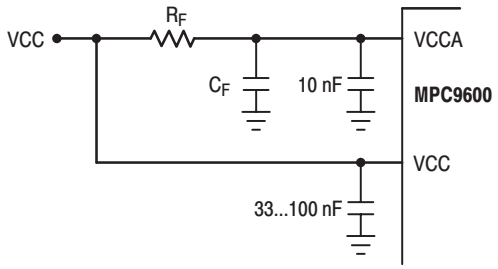



**Figure 5. $V_{CCA}$ Power Supply Filter**

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9600 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

### Using the MPC9600 in zero–delay applications

Nested clock trees are typical applications for the MPC9600. For these applications the MPC9600 offers a differential LVPECL clock input pair as a PLL reference. This allows for the use of differential LVPECL primary clock distribution devices such as the Motorola MC100ES6111 or MC100ES6226, taking advantage of its superior low-skew performance. Clock trees using LVPECL for clock distribution and the MPC9600 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers.

The external feedback option of the MPC9600 PLL allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge and virtually eliminates the propagation delay through the device.

The remaining insertion delay (skew error) of the MPC9600 in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset (SPO or $t_{(\varnothing)}$), I/O jitter ($t_{JIT(\varnothing)}$, phase or long-term jitter), feedback path delay and the output-to-output skew ($t_{SK(O)}$ relative to the feedback output.

### Calculation of part-to-part skew

The MPC9600 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs (CCLK or PCLK) of two or more MPC9600 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

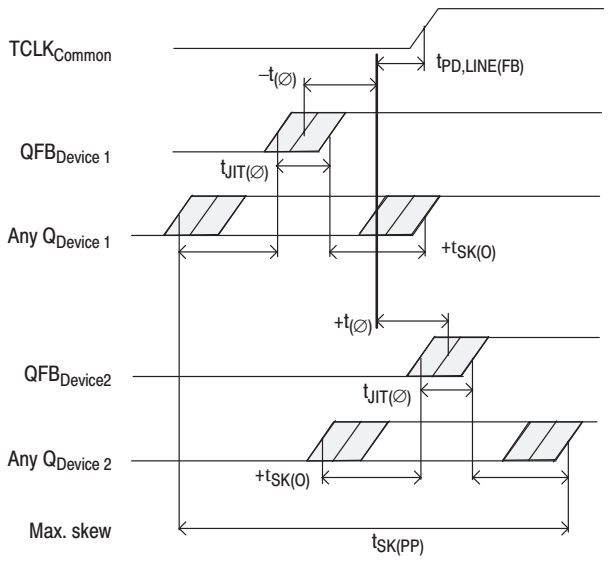



**Figure 6. MPC9600 max. device-to-device skew**

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

**Table 8: Confidence Facter CF**

| CF | Probability of clock edge within the distribution |
|---|---|
| ± 1σ | 0.68268948 |
| ± 2σ | 0.95449988 |
| ± 3σ | 0.99730007 |
| ± 4σ | 0.99993663 |
| ± 5σ | 0.99999943 |
| ± 6σ | 0.99999999 |

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of -261 ps to 341 ps relative to CCLK ($V_{CC}$=3.3V and $f_{VCO}$ = 200 MHz):

$$t_{SK(PP)} = [–60ps...140ps] + [–150ps...150ps] + [(17ps \cdot –3)...(17ps \cdot 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [–261ps...341ps] + t_{PD,\ LINE(FB)}$$

Above equation uses the maximum I/O jitter number shown in the AC characteristic table for $V_{CC}$=3.3V (17 ps RMS). I/O jitter is frequency dependant with a maximum at the lowest VCO frequency (200 MHz for the MPC9600). Applications using a higher VCO frequency exhibit less I/O jitter than the AC characteristic limit. The I/O jitter characteristics in Figure 7 can be used to derive a smaller I/O jitter number at the specific VCO frequency, resulting in tighter timing limits in zero-delay mode and for part-to-part skew $t_{SK(PP)}$.

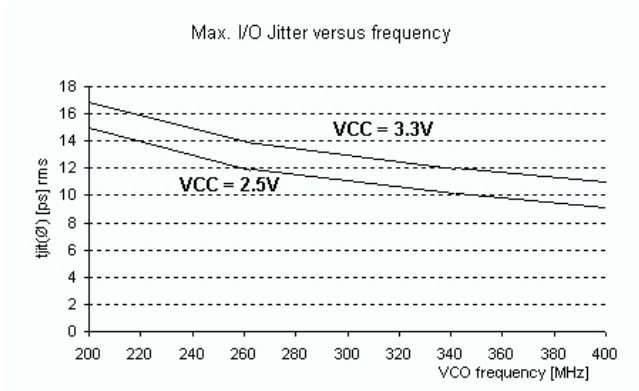



**Figure 7. Max. I/O Jitter versus VCO frequency for $V_{CC}$=2.5V and $V_{CC}$=3.3V**

### Driving Transmission Lines

The MPC9600 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}$÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output

of the MPC9600 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 8 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9600 clock driver is effectively doubled due to its capability to drive multiple lines.

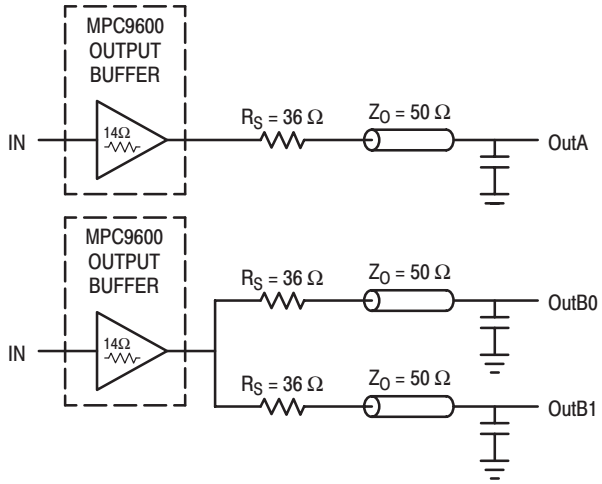



**Figure 8. Single versus Dual Transmission Lines**

The waveform plots in Figure 9 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9600 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9600. The output waveform in Figure 9 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S ( Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\ \Omega \parallel 50\ \Omega$$
$$R_S = 36\ \Omega \parallel 36\ \Omega$$
$$R_0 = 14\ \Omega$$

$$V_L = 3.0 ( 25 \div (18+17+25)$$
$$= 1.31\ V$$

At the load end the voltage will double due to the near unity reflection coefficient, to 2.6 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

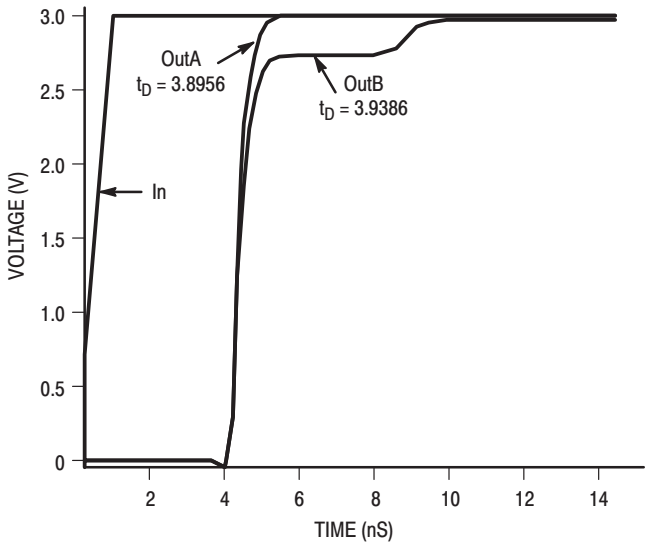
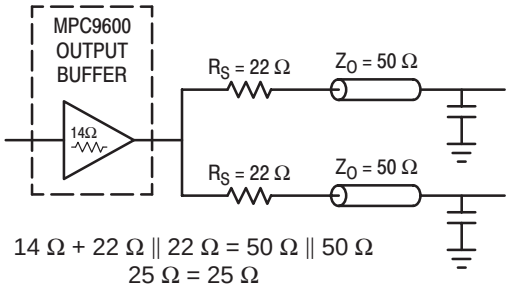



**Figure 9. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 10 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




$$14\ \Omega + 22\ \Omega \parallel 22\ \Omega = 50\ \Omega \parallel 50\ \Omega$$
$$25\ \Omega = 25\ \Omega$$

**Figure 10. Optimized Dual Line Termination**

**The Following Figures Illustrate the Measurement Reference for the MPC9600 Clock Driver Circuit**

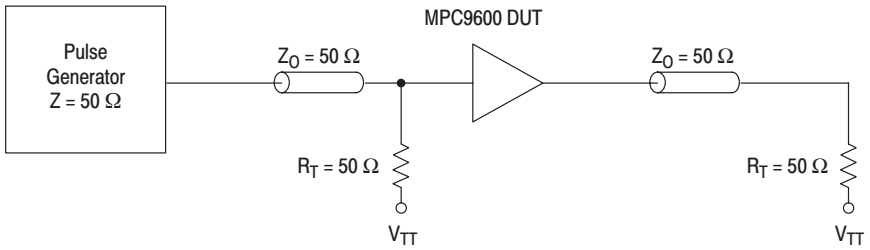



**Figure 11. CCLK MPC9600 AC test reference**

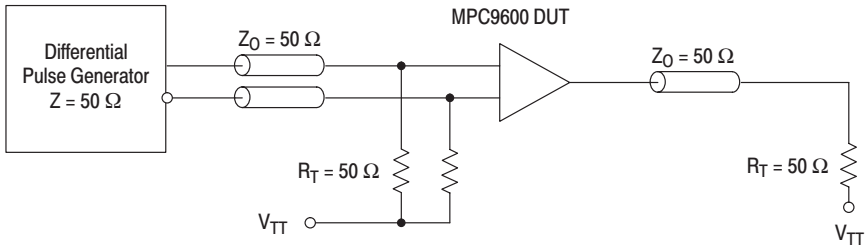



**Figure 12. PCLK MPC9600 AC test reference**

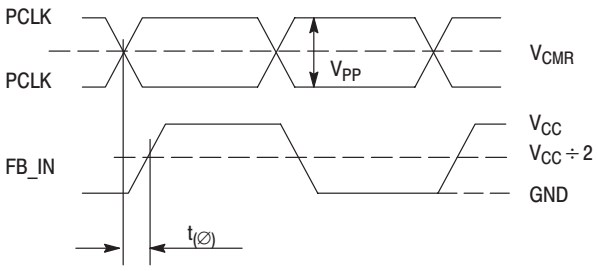



**Figure 13. Propagation delay $t_{(\varnothing)}$, static phase offset) test reference**

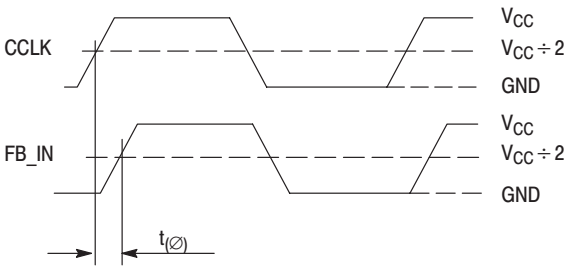
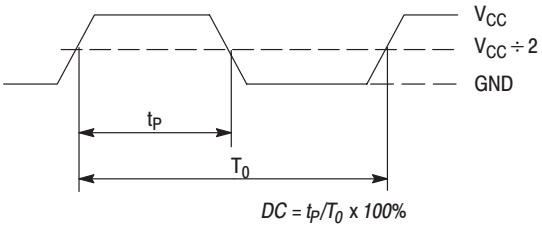
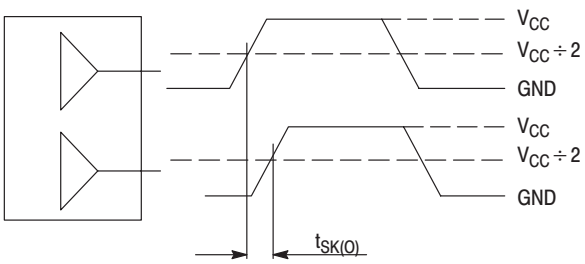



**Figure 14. Propagation delay $t_{(\varnothing)}$ test reference**



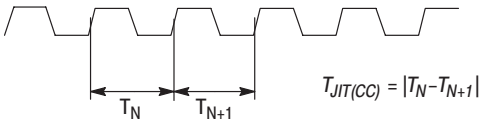

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 15. Output Duty Cycle (DC)**



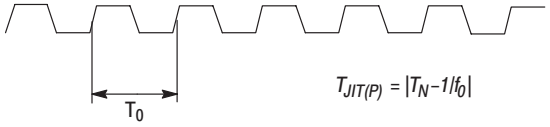

The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 16. Output–to–output Skew $t_{SK(O)}$**




The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

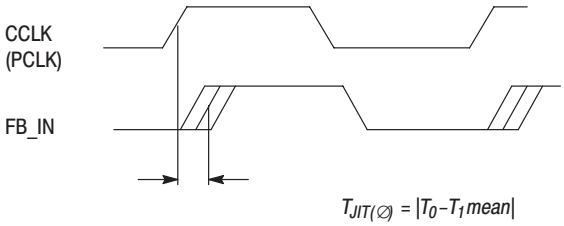
**Figure 17. Cycle–to–cycle Jitter**




The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

**Figure 18. Period Jitter**






The deviation in $t_0$ for a controlled edge with respect to a $t_0$ mean in a random sample of cycles

**Figure 19. I/O Jitter**

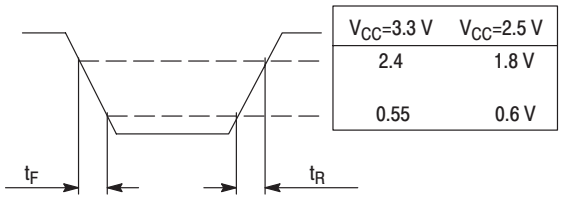



**Figure 20. Output Transition Time Test Reference**

**Order Number: MPC972/D**
**Rev 6, 09/2001**

# Low Voltage PLL Clock Driver



The MPC972 is a 3.3 V compatible, PLL based clock driver device targeted for high performance CISC or RISC processor based systems. With output frequencies of up to 125 MHz and skews of 550 ps the MPC972 is ideally suited for most synchronous systems. The device offers twelve low skew outputs plus a feedback and sync output for added flexibility and ease of system implementation.

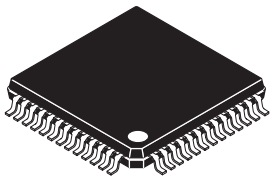
- Fully Integrated PLL
- Output Frequency up to 125 MHz
- Compatible with **PowerPC**™ and Pentium™ Microprocessors
- LQFP Packaging
- 3.3 V $V_{CC}$
- ± 100 ps Typical Cycle–to–Cycle Jitter

The MPC972 features an extensive level of frequency programmability between the 12 outputs as well as the input vs output relationships. Using the select lines output frequency ratios of 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 5:1, 5:2, 5:3, 6:1 and 6:5 between outputs can be realized by pulsing low one clock edge prior to the coincident edges of the Qa and Qc outputs. The Sync output will indicate when the coincident rising edges of the above relationships will occur. The selectability of the feedback frequency is independent of the output frequencies, this allows for very flexible programming of the input reference vs output frequency relationship. The output frequencies can be either odd or even multiples of the input reference. In addition the output frequency can be less than the input frequency for applications where a frequency needs to be reduced by a non–binary factor. The Power–On Reset ensures proper programming if the frequency select pins are set at power up. If the fselFB2 pin is held high, it may be necessary to apply a reset after power–up to ensure synchronization between the QFB output and the other outputs. The internal power–on reset is designed to provide this function, but with power–up conditions being dependent, it is difficult to guarantee. All other conditions of the fsel pins will automatically synchronize during PLL lock acquisition.

**MPC972**

**See Upgrade Product – MPC9772**

**LOW VOLTAGE PLL CLOCK DRIVER**



**SCALE 2:1**

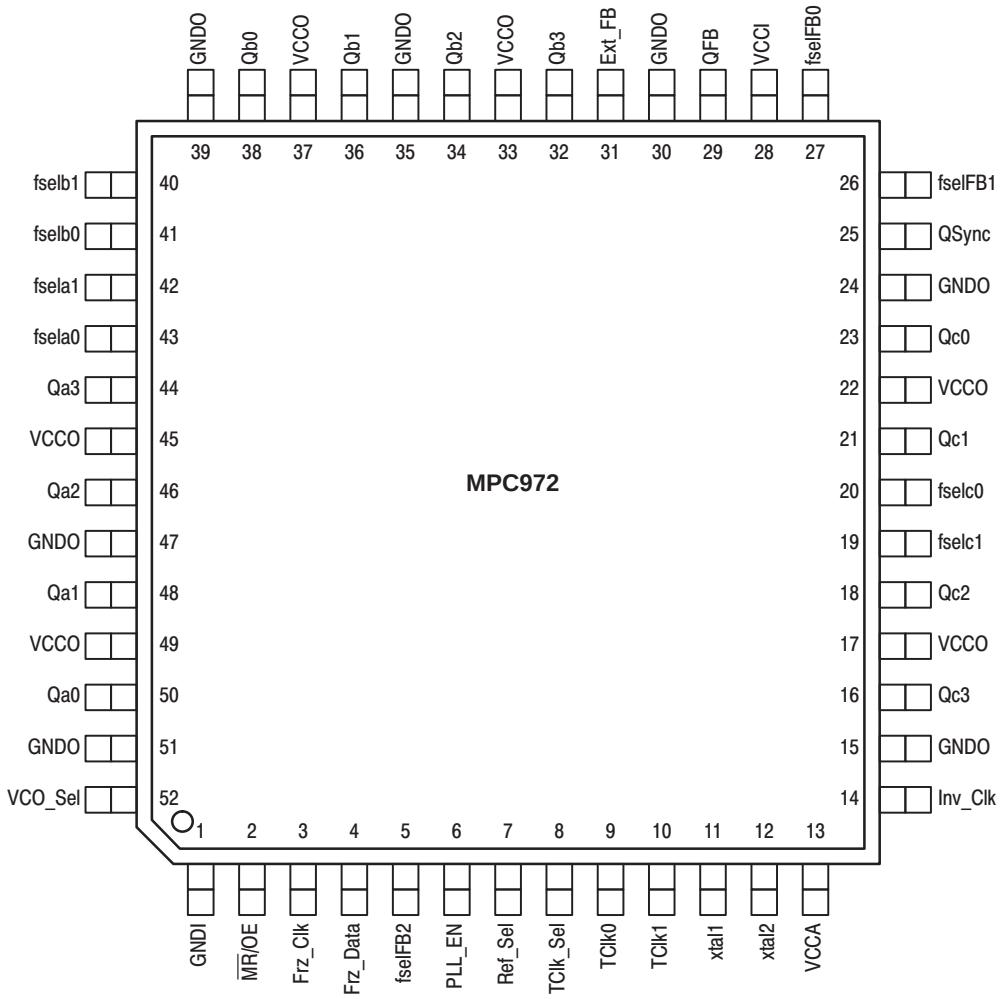
**FA SUFFIX**
52–LEAD LQFP PACKAGE
CASE 848D-03

The MPC972 offers a very flexible output enable/disable scheme. This enable/disable scheme helps facilitate system debug as well as provide unique opportunities for system power down schemes to meet the requirements of “green” class machines. The MPC972 allows for the enabling of each output independently via a serial input port. When disabled or “frozen” the outputs will be locked in the “LOW” state, however the internal state machines will continue to run. Therefore when “unfrozen” the outputs will activate synchronous and in phase with those outputs which were not frozen. The freezing and unfreezing of outputs occurs only when they are already in the “LOW” state, thus the possibility of runt pulse generation is eliminated. A power-on reset will ensure that upon power up all of the outputs will be active. Note that all of the control inputs on the MPC972 have internal pull–up resistors.

The MPC972 is fully 3.3 V compatible and requires no external loop filter components. All inputs accept LVCMOS/LVTTL compatible levels while the outputs provide LVCMOS levels with the capability to drive 50 Ω transmission lines. For series terminated lines each MPC972 output can drive two 50 Ω lines in parallel thus effectively doubling the fanout of the device.

The MPC972 can consume significant power in some configurations. Users are encouraged to review Application Note AN1545/D in the Advanced Clock Drivers Device Data book (DL207/D) for a discussion on the thermal issues with the MPC family of clock drivers.


**Rev 6**




All inputs have internal pull–up resistors (appr. 50 K) except for the xtal1 and xtal2 pins.

**Figure 1. 52–Lead Pinout** (Top View)

**FUNCTION TABLE 1**

| fsela1 | fsela0 | Qa | fselb1 | fselb0 | Qb | fselc1 | fselc0 | Qc |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | ÷4 | 0 | 0 | ÷4 | 0 | 0 | ÷2 |
| 0 | 1 | ÷6 | 0 | 1 | ÷6 | 0 | 1 | ÷4 |
| 1 | 0 | ÷8 | 1 | 0 | ÷8 | 1 | 0 | ÷6 |
| 1 | 1 | ÷12 | 1 | 1 | ÷10 | 1 | 1 | ÷8 |

**FUNCTION TABLE 2**

| *fselFB2 | fselFB1 | fselFB0 | QFB |
|---|---|---|---|
| 0 | 0 | 0 | ÷4 |
| 0 | 0 | 1 | ÷6 |
| 0 | 1 | 0 | ÷8 |
| 0 | 1 | 1 | ÷10 |
| 1 | 0 | 0 | ÷8 |
| 1 | 0 | 1 | ÷12 |
| 1 | 1 | 0 | ÷16 |
| 1 | 1 | 1 | ÷20 |

*If the fselFB2 is 1, it may be necessary to apply a reset after power up to ensure synchronization between QFB and the other inputs.

**FUNCTION TABLE 3**

| Control Pin | Logic ‘0’ | Logic ‘1’ |
|---|---|---|
| VCO_Sel | VCO/2 | VCO |
| Ref_Sel | TCLK | Xtal (PECL) |
| TCLK_Sel | TCLK0 | TCLK1 |
| PLL_En | Bypass PLL | Enable PLL |
| $\overline{MR}$/OE | Master Reset/Output Hi–Z | Enable Outputs |
| Inv_Clk | Non–Inverted Qc2, Qc3 | Inverted Qc2, Qc3 |

2

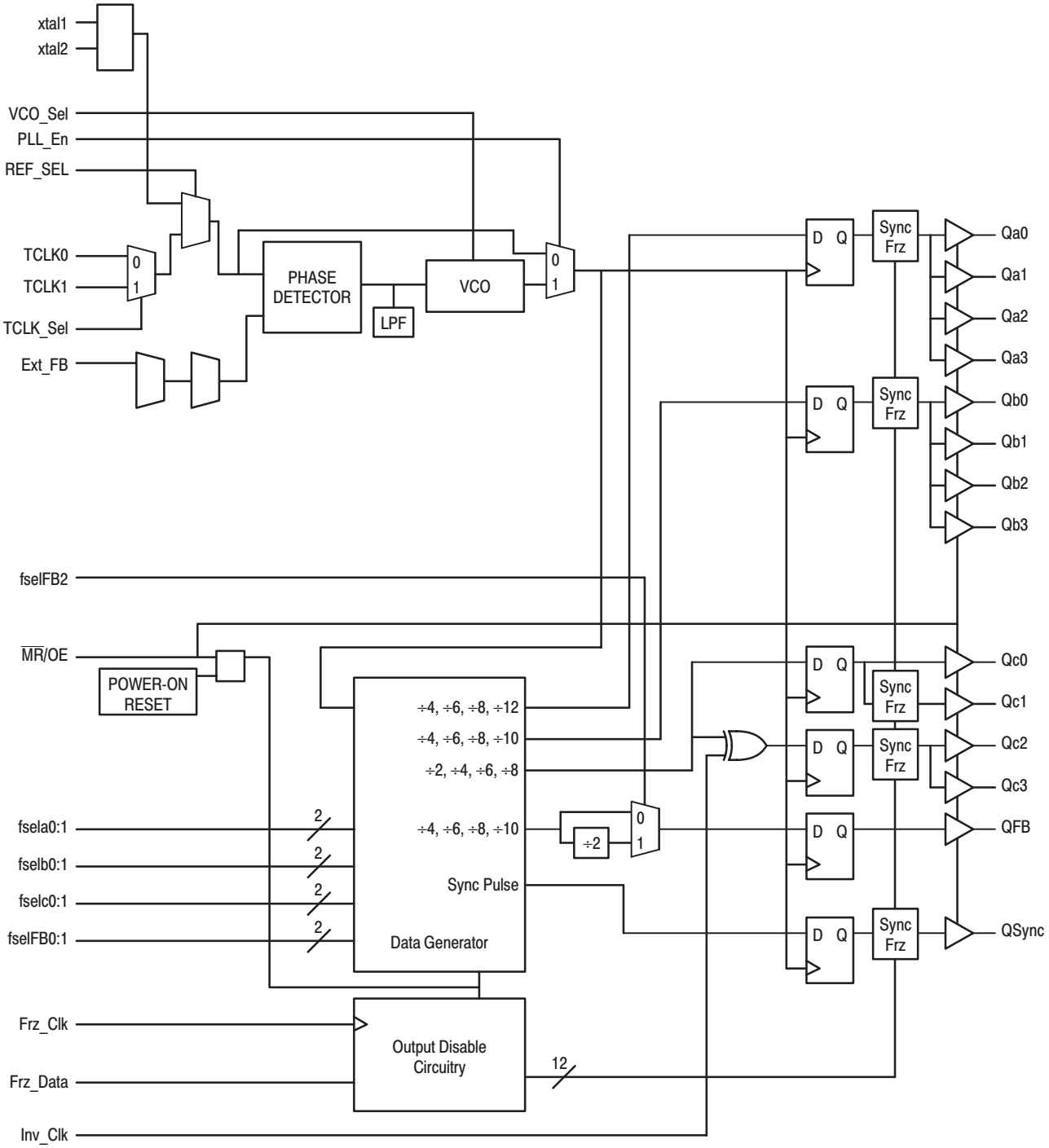



**Figure 2. Logic Diagram**

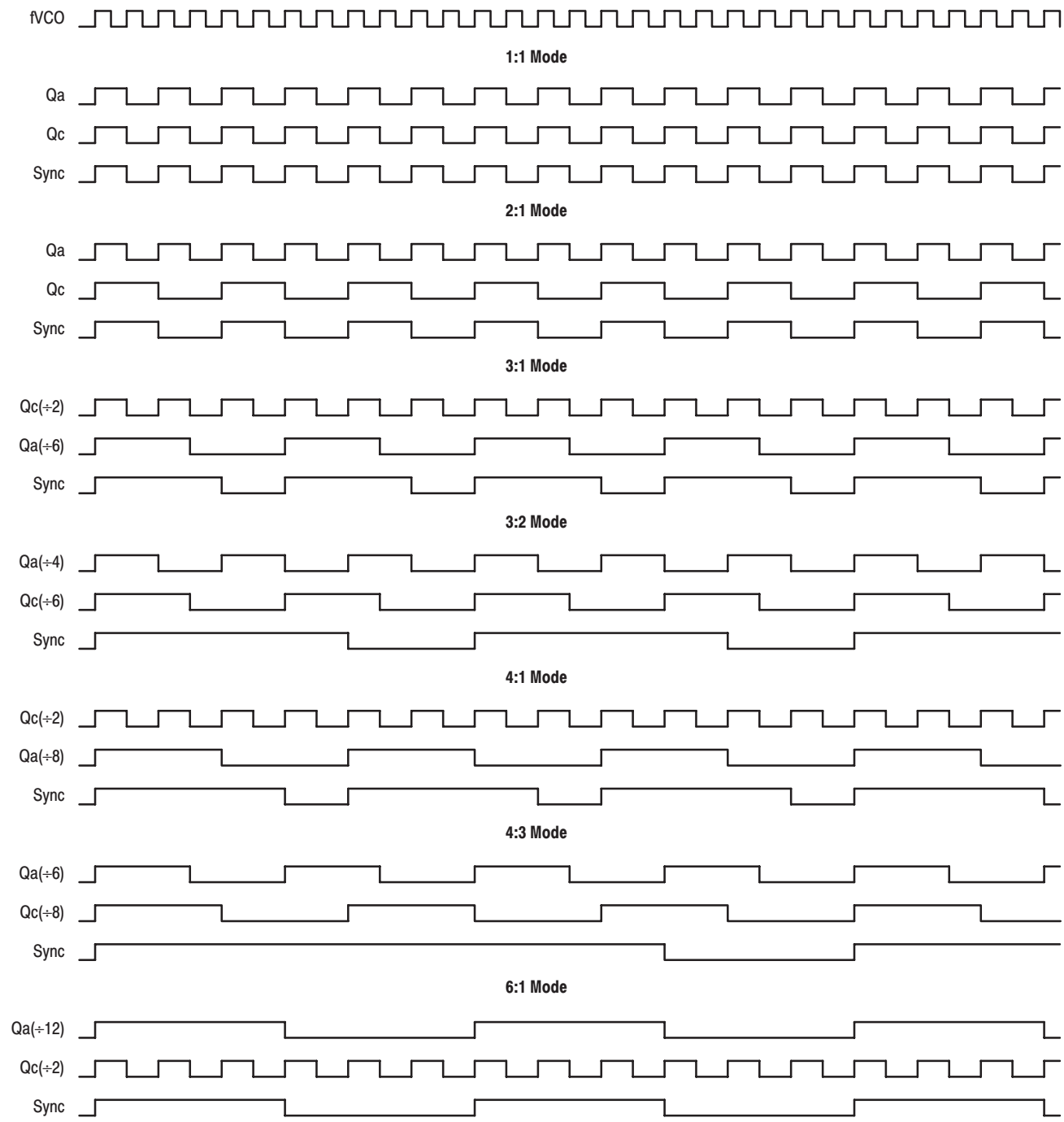



**Figure 3. Timing Diagrams**

**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 4.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | Input Current | | ±20 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

2

**THERMAL CHARACTERISTICS**

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to long–term reliability is addressed in the Motorola application note AN1545.

**DC CHARACTERISTICS** (Note 3.; $T_A$ = 0° to 70°C; $V_{CC}$ = 3.3 V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{CCA}$ | Analog $V_{CC}$ Voltage | 2.935 | | $V_{CC}$ | V | |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | 3.6 | V | |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | $I_{OH}$ = –20 mA (Note 1.) |
| $V_{OL}$ | Output LOW Voltage | | | 0.5 | V | $I_{OL}$ = 20 mA (Note 1.) |
| $I_{IN}$ | Input Current | | | ±120 | µA | Note 2. |
| $I_{CC}$ | Maximum Quiescent Supply Current | | 190 | 215 | mA | All VCC PIns |
| $I_{CCA}$ | Analog $V_{CC}$ Current | | 15 | 20 | mA | |
| $C_{IN}$ | Input Capacitance | | | 4 | pF | |
| $C_{pd}$ | Power Dissipation Capacitance | | 25 | | pF | Per Output |

1. The MPC972 outputs can drive series or parallel terminated 50 Ω (or 50 Ω to $V_{CC}$/2) transmission lines on the incident edge (see Applications Info section).
2. Inputs have pull–up/pull–down resistors which affect input current.
3. Special thermal handling may be required in some configurations.

**PLL INPUT REFERENCE CHARACTERISTICS** ($T_A$ = 0° to 70°C)

| Symbol | Characteristic | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $t_r$, $t_f$ | TCLK Input Rise/Falls | | 3.0 | ns | |
| $f_{ref}$ | Reference Input Frequency | Note 1. | 100<br>Note 1. | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | 25 | 75 | % | |
| $t_{xtal}$ | Crystal Oscillator Frequency | 10 | 25 | MHz | Note 2. |

1. Maximum input reference frequency is limited by the VCO lock range and the feedback divider or 100MHz, minimum input reference frequency is limited by the VCO lock range and the feedback divider.
2. See Applications Info section for more crystal information.

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C; $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.15 | | 1.2 | ns | 0.8 to 2.0V, Note 1. |
| $t_{pw}$ | Output Duty Cycle | | $t_{CYCLE}/2$ –750 | $t_{CYCLE}/2$ ±500 | $t_{CYCLE}/2$ +750 | ps | Note 1. |
| $t_{pd}$ | SYNC to Feedback Propagation Delay | TCLK0<br>TCLK1 | –270<br>–330 | 130<br>70 | 530<br>470 | ps | Notes 1., 2.; QFB = ÷8 |
| $t_{os}$ | Output-to-Output Skew | | | | 550 | ps | Note 1. |
| $f_{VCO}$ | VCO Lock Range | | 200 | | 480 | MHz | |
| $f_{max}$ | Maximum Output Frequency | Q (÷2)<br>Q (÷4)<br>Q (÷6)<br>Q (÷8) | | | 125<br>120<br>80<br>60 | MHz | Note 1. |
| $t_{jitter}$ | Cycle–to–Cycle Jitter (Peak–to–Peak) | | | ±100 | | ps | Note 1. |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time | | 2 | | 8 | ns | Note 1. |
| $t_{PZL}$, $t_{PZH}$ | Output ENable TIme | | 2 | | 10 | ns | Note 1. |
| $t_{lock}$ | Maximum PLL Lock Time | | | | 10 | ms | |
| $f_{MAX}$ | Maximum Frz_Clk Frequency | | | | 20 | MHz | |

1. 50Ω transmission line terminated into $V_{CC}/2$.
2. $t_{pd}$ is specified for a 50MHz input reference. The window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The $t_{pd}$ does not include jitter.

## APPLICATIONS INFORMATION

**Programming the MPC972**

The MPC972 is one of the most flexible frequency programming devices in the Motorola timing solution portfolio. With three independent banks of four outputs as well as an independent PLL feedback output the total number of possible configurations is too numerous to tabulate. Table 1 tabulates the various selection possibilities for the three banks of outputs. The divide numbers presented in the table represent the divider applied to the output of the VCO for that bank of outputs. To determine the relationship between the three banks the three divide ratios would be compared. For instance if a frequency relationship of 5:3:2 was desired the following selection could be made. The Qb outputs could be set to ÷10, the Qa outputs to ÷6 and the Qc outputs to ÷4. With this output divide selection the desired 5:3:2 relationship would be generated. For situations where the VCO will run at relatively low frequencies the PLL may not be stable for the desired divide ratios. For these circumstances the VCO_Sel pin allows for an extra ÷2 to be added into the clock path. When asserted this pin will maintain the desired output relationships, but will provide an enhanced lock range for the PLL. Once the output frequency relationship is set and the VCO is in its stable range the feedback output would be programmed to match the input reference frequency.

The MPC972 offers only an external feedback to the PLL. A separate feedback output is provided to optimize the flexibility of the device. If in the example above the input reference frequency was equal to the lowest output frequency the feedback output would be set in the ÷10 mode. If the input needed to be half the lowest frequency output the fselFB2 input could be asserted to halve the feedback frequency. This action multiplies the output frequencies by two relative to the input reference frequency. With 7 unique feedback divide capabilities there is a tremendous amount of flexibility. Again assume the above 5:3:2 relationship is needed with the highest frequency output equal to 100 MHz. If one was also constrained because the only reference frequency available was 50 MHz the setup in Figure 6 could be used. The MPC972 provides the 100, 66 and 40 MHz outputs all synthesized from the 50 MHz source. With its multitude of divide ratio capabilities the MPC972 can generate almost any frequency from a standard, common frequency already present in a design. Figure 7 and Figure 8 illustrate a few more examples of possible MPC972 configurations.

The MPC972 has one more programming feature added to its arsenal. The Inv_Clk input pin when asserted will invert the Qc2 and Qc3 outputs. This inversion will not affect the output–output skew of the device. This inversion allows for the development of 180° phase shifted clocks. This output could also be used as a feedback output to the MPC972 or a second PLL device to generate early or late clocks for a specific design. Figure 9 illustrates the use of two MPC972's to generate two banks of clocks with one bank divided by 2 and delayed by 180° relative to the first.

**SYNC Output Description**

In situations where output frequency relationships are not integer multiples of each other there is a need for a signal for system synchronization purposes. The SYNC output of the MPC972 is designed to specifically address this need. The MPC972 monitors the relationship between the Qa and the Qc banks of outputs. It provides a low going pulse, one period in duration, one period prior to the coincident rising edges of the Qa and Qc outputs. The duration and the placement of the pulse is dependent on the higher of the Qa and Qc output frequencies. The timing diagrams in the data sheet show the various waveforms for the SYNC output. Note that the SYNC output is defined for all possible combinations of the Qa and Qc outputs even though under some relationships the lower frequency clock could be used as a synchronizing signal.



**Table 1. Programmable Output Frequency Relationships** (VCO_Sel = '1')

| fsela1 | fsela0 | Qa | fselb1 | fselb0 | Qb | fselc1 | fselc0 | Qc |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | VCO/4 | 0 | 0 | VCO/4 | 0 | 0 | VCO/2 |
| 0 | 1 | VCO/6 | 0 | 1 | VCO/6 | 0 | 1 | VCO/4 |
| 1 | 0 | VCO/8 | 1 | 0 | VCO/8 | 1 | 0 | VCO/6 |
| 1 | 1 | VCO/12 | 1 | 1 | VCO/10 | 1 | 1 | VCO/8 |

**Table 2. Programmable Output Frequency Relationships** (VCO_Sel = '1')

| fselFB2 | fselFB1 | fselFB0 | QFB |
|---|---|---|---|
| 0 | 0 | 0 | VCO/4 |
| 0 | 0 | 1 | VCO/6 |
| 0 | 1 | 0 | VCO/8 |
| 0 | 1 | 1 | VCO/10 |
| 1 | 0 | 0 | VCO/8 |
| 1 | 0 | 1 | VCO/12 |
| 1 | 1 | 0 | VCO/16 |
| 1 | 1 | 1 | VCO/20 |

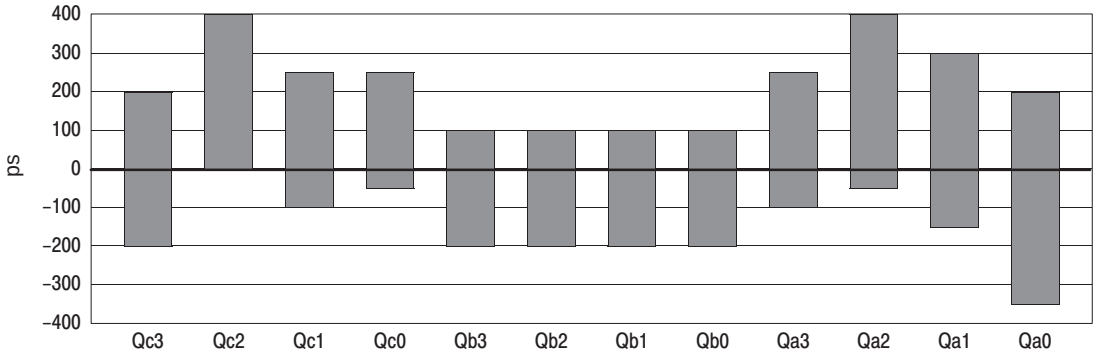



**Figure 4. Typical Skews Relative to QFB**

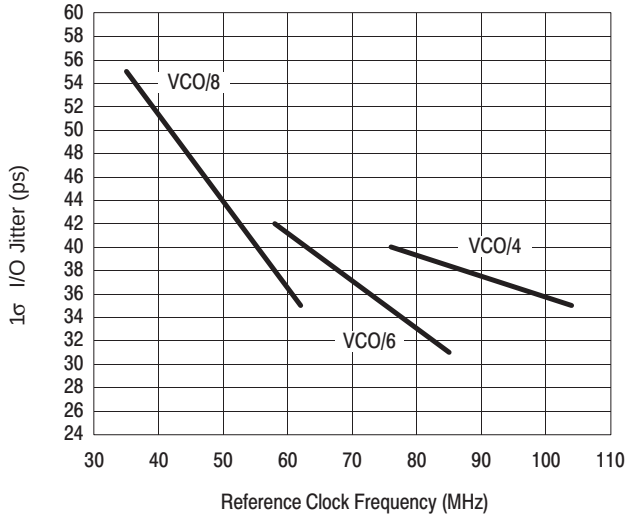



**Figure 5. Typical Phase Jitter versus Reference Frequency**
I/O Jitter

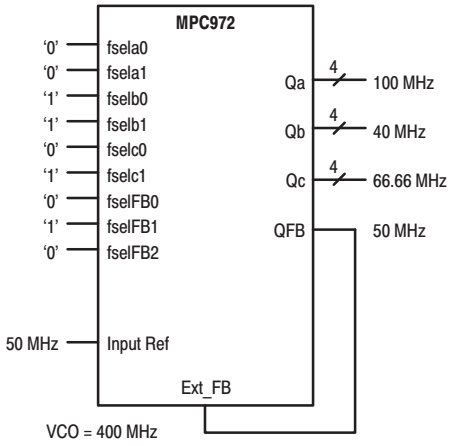



**Figure 6. Programming Configuration Example**

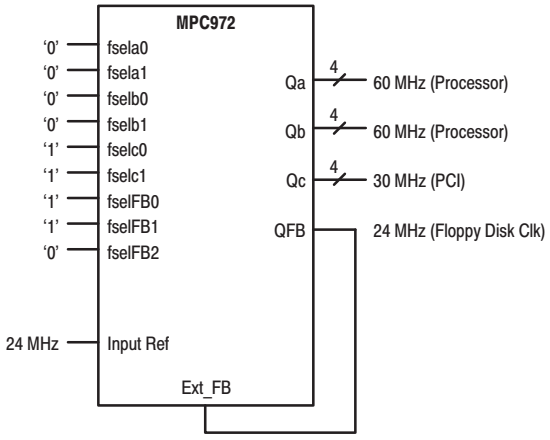



**Figure 7. Generating Pentium Clocks from Floppy Clock**

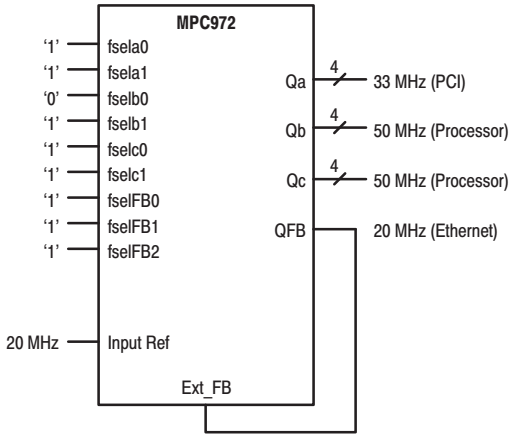



**Figure 8. Generating MPC604 Clocks from Ethernet Clocks**

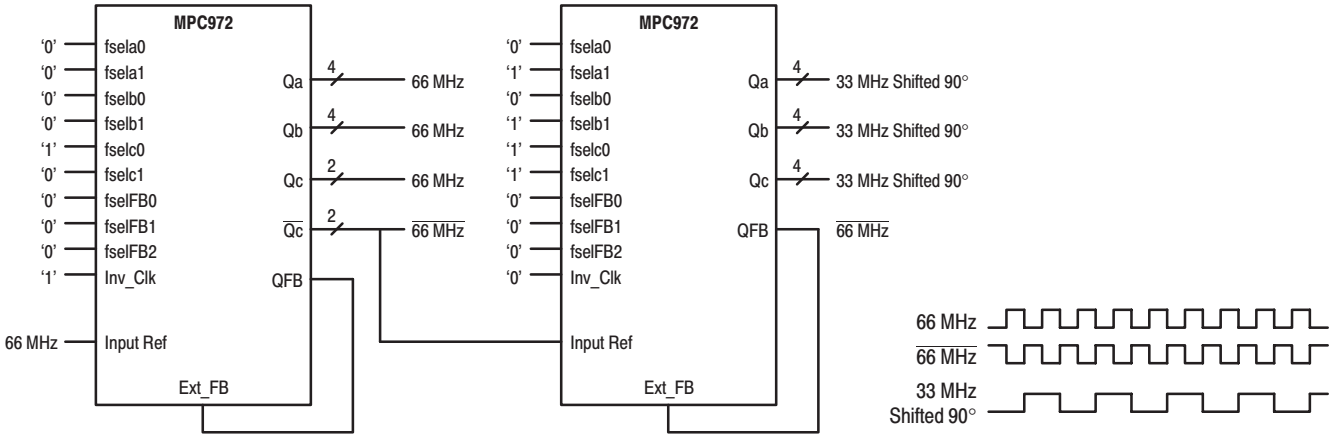



**Figure 9. Phase Delay Using Multiple MPC972's**

**Using the On–Board Crystal Oscillator**

The MPC972 features an on–board crystal oscillator to allow for seed clock generation as well as final distribution. The on–board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC972 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required.

The oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on–board capacitors. Because the design is a series resonant design for the optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most of the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC972 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implementations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

**3. Crystal Recommendations**

| Parameter | Value |
|---|---|
| Crystal Cut | Fundamental AT Cut |
| Resonance | Series Resonance* |
| Frequency Tolerance | ±75 ppm at 25°C |
| Frequency/Temperature Stability | ±150 pm 0 to 70°C |
| Operating Range | 0 to 70°C |
| Shunt Capacitance | 5–7 pF |
| Equivalent Series Resistance (ESR) | 50 to 80 Ω Max |
| Correlation Drive Level | 100 μW |
| Aging | 5 ppm/Yr (First 3 Years) |

* See accompanying text for series versus parallel resonant discussion.

The MPC972 is a clock driver which was designed to generate outputs with programmable frequency relationships and not a synthesizer with a fixed input frequency. As a result the crystal input frequency is a function of the desired output frequency. For a design which utilizes the external feedback to the PLL the selection of the crystal frequency is straight forward; simply chose a crystal which is equal in frequency to the fed back signal.

**Recommended External Reset Timing**

For MPC972 applications requiring synchronization of the output clock to the input clock and if fselFB2 = 1, the assertion of $\overline{MR}$ is recommended. The timing of asserting $\overline{MR}$ should be as shown in Figure 10. The power supply should be at or above the minimum specified voltage and the reference clock input (refclk) should be present a minimum of t1 prior to the reset pulse being applied to the $\overline{MR}$ pin.

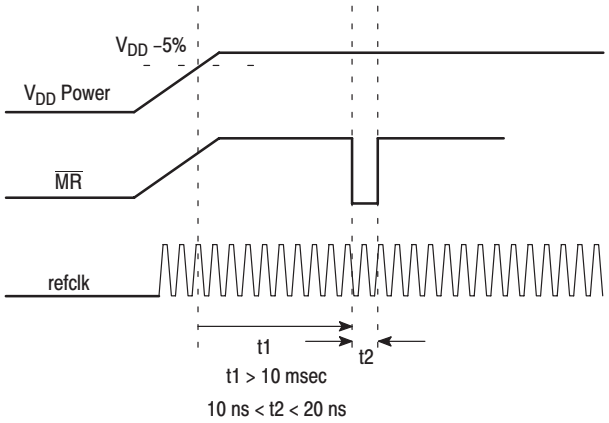



**Figure 10. Assertion of $\overline{MR}$**

**Power Supply Filtering**

The MPC972 is a mixed analog/digital product and exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC972 provides separate power supplies for the output buffers ($V_{CCO}$) and the internal PLL ($V_{CCA}$) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the $V_{CCA}$ pin for the MPC972.

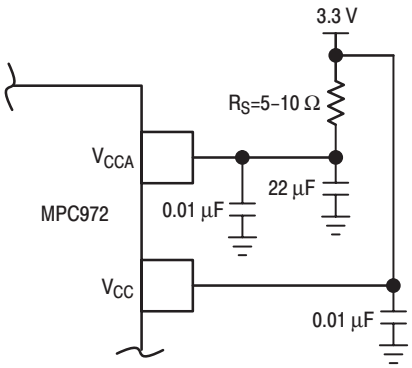



**Figure 11. Power Supply Filter**

Figure 11 illustrates a typical power supply filter scheme. The MPC972 is most susceptible to noise with spectral content in the 1 KHz to 1 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the $V_{CCA}$ pin of the

MPC972. From the data sheet the $I_{VCCA}$ current (the current sourced through the $V_{CCA}$ pin) is typically 15 mA (20 mA maximum), assuming that a minimum of 2.935 V must be maintained on the $V_{CCA}$ pin very little DC voltage drop can be tolerated when a 3.3 V $V_{CC}$ supply is used. The resistor shown in Figure 11 must have a resistance of 5–10 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

Although the MPC972 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Driving Transmission Lines**

The MPC972 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC}$/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC972 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 12 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC972 clock driver is effectively doubled due to its capability to drive multiple lines.

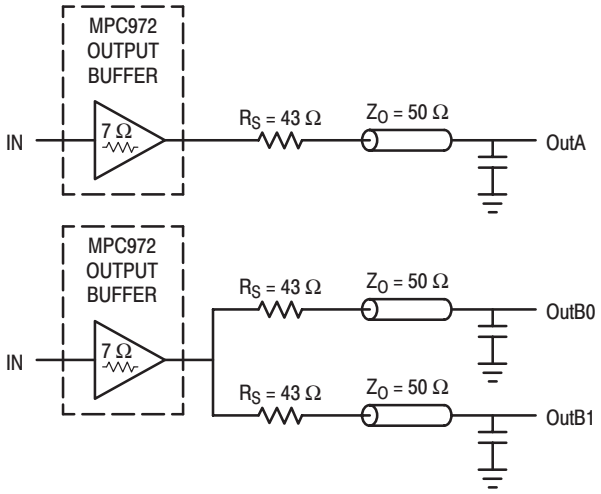



**Figure 12. Single versus Dual Transmission Lines**

The waveform plots of Figure 13 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC972 output buffers is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC972. The output waveform in Figure 13 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS ( Zo / Rs + Ro + Zo) = 3.0 (25/53.5) = 1.40 V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 14 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

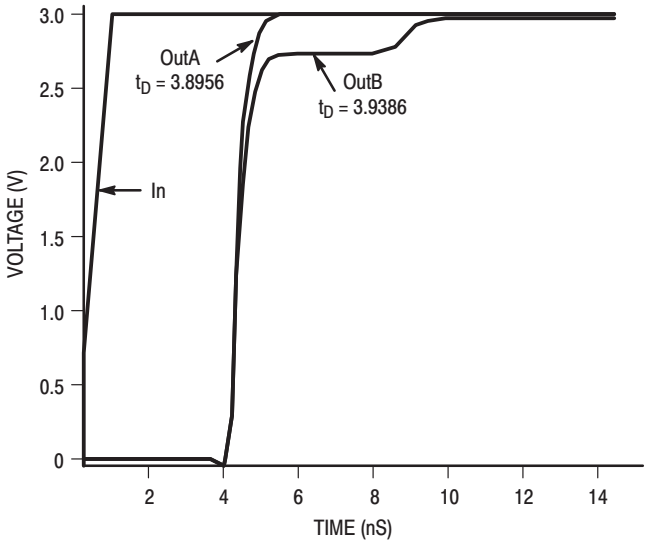
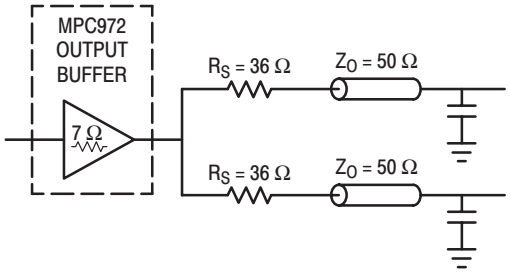



**Figure 13. Single versus Dual Waveforms**




7 Ω + 36 Ω || 36 Ω = 50 Ω || 50 Ω
25 Ω = 25 Ω

**Figure 14. Optimized Dual Line Termination**

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

**Using the Output Freeze Circuitry**

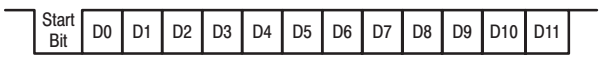
With the recent advent of a “green” classification for computers the desire for unique power management among system designers is keen. The individual output enable control of the MPC972 allows designers, under software control, to implement unique power management schemes into their designs. Although useful, individual output control at the expense of one pin per output is too high, therefore a simple serial interface was derived to economize on the control pins.

The freeze control logic provides a mechanism through which the MPC972 clock outputs may be frozen (stopped in the logic ‘0’ state):

The freeze mechanism allows serial loading of the 12–bit Serial Input Register, this register contains one programmable freeze enable bit for 12 of the 14 output clocks. The Qc0 and QFB outputs cannot be frozen with the serial port, this avoids any potential lock up situation should an error occur in the loading of the Serial Input Register. The user may program an output clock to freeze by writing logic ‘0’ to the respective freeze enable bit. Likewise, the user may programmably unfreeze an output clock by writing logic ‘1’ to the respective enable bit.

The freeze logic will never force a newly–frozen clock to a logic ‘0’ state before the time at which it would normally transition there. The logic simply keeps the frozen clock at logic ‘0’ once it is there. Likewise, the freeze logic will never force a newly–unfrozen clock to a logic ‘1’ state before the time at which it would normally transition there. The logic re–enables the unfrozen clock during the time when the respective clock would normally be in a logic ‘0’ state, eliminating the possibility of ‘runt’ clock pulses.

The user may write to the Serial Input register through the Frz_Data input by supplying a logic ‘0’ start bit followed serially by 12 NRZ freeze enable bits. The period of each Frz_Data bit equals the period of the free–running Frz_Clk signal. The Frz_Data serial transmission should be timed so the MPC972 can sample each Frz_Data bit with the rising edge of the free–running Frz_Clk signal.




D0–D3 are the control bits for Qa0–Qa3, respectively
D4–D7 are the control bits for Qb0–Qb3, respectively
D8–D10 are the control bits for Qc1–Qc3, respectively
D11 is the control bit for QSync

**Figure 15. Freeze Data Input Protocol**

**Order Number: MPC973/D**
**Rev. 2, 09/2001**

# Low Voltage PLL Clock Driver



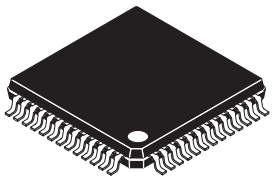
The MPC973 is a 3.3 V compatible, PLL based clock driver device targeted for high performance CISC or RISC processor based systems. With output frequencies of up to 125 MHz and skews of 550 ps the MPC973 is ideally suited for most synchronous systems. The device offer twelve low skew outputs plus a feedback and sync output for added flexibility and ease of system implementation.

- Fully Integrated PLL
- Output Frequency up to 125 MHz
- Compatible with **PowerPC**™ and Pentium™ Microprocessors
- LQFP Packaging
- 3.3 V $V_{CC}$
- ± 100ps Typical Cycle–to–Cycle Jitter

**MPC973**

**See Upgrade Product – MPC9773**

**LOW VOLTAGE PLL CLOCK DRIVER**



**SCALE 2:1**

**FA SUFFIX**
52–LEAD LQFP PACKAGE
CASE 848D-03

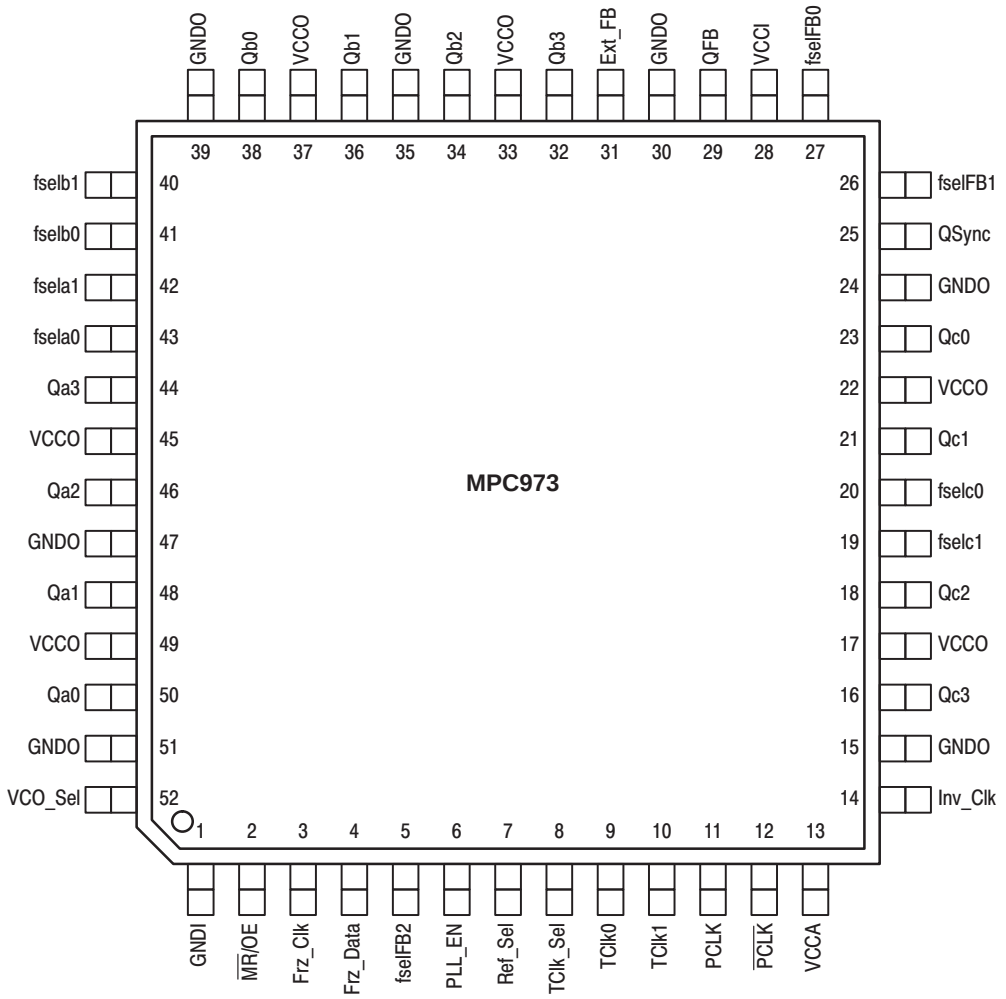
The MPC973 features an extensive level of frequency programmability between the 12 outputs as well as the input vs output relationships. Using the select lines output frequency ratios of 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 5:1, 5:2, 5:3, 6:1 and 6:5 between outputs can be realized by pulsing low one clock edge prior to the coincident edges of the Qa and Qc outputs. The Sync output will indicate when the coincident rising edges of the above relationships will occur. The selectability of the feedback frequency is independent of the output frequencies, this allows for very flexible programming of the input reference vs output frequency relationship. The output frequencies can be either odd or even multiples of the input reference. In addition the output frequency can be less than the input frequency for applications where a frequency needs to be reduced by a non–binary factor. The Power–On Reset ensures proper programming if the frequency select pins are set at power up. If the fselFB2 pin is held high, it may be necessary to apply a reset after power–up to ensure synchronization between the QFB output and the other outputs. The internal power–on reset is designed to provide this function, but with power–up conditions being dependent, it is difficult to guarantee. All other conditions of the fsel pins will automatically synchronize during PLL lock acquisition.

The MPC973 offers a very flexible output enable/disable scheme. This enable/disable scheme helps facilitate system debug as well as provide unique opportunities for system power down schemes to meet the requirements of “green” class machines. The MPC973 allows for the enabling of each output independently via a serial input port. When disabled or “frozen” the outputs will be locked in the “LOW” state, however the internal state machines will continue to run. Therefore when “unfrozen” the outputs will activate synchronous and in phase with those outputs which were not frozen. The freezing and unfreezing of outputs occurs only when they are already in the “LOW” state, thus the possibility of runt pulse generation is eliminated. A power-on reset will ensure that upon power up all of the outputs will be active. Note that all of the control inputs on the MPC973 have internal pull–up resistors.

The MPC973 is fully 3.3 V compatible and requires no external loop filter components. All inputs accept LVCMOS/LVTTL compatible levels while the outputs provide LVCMOS levels with the capability to drive 50 Ω transmission lines. For series terminated lines each MPC973 output can drive two 50 Ω lines in parallel thus effectively doubling the fanout of the device.

The MPC973 can consume significant power in some configurations. Users are encouraged to review Application Note AN1545/D in the Advanced Clock Drivers Device Data book (DL207/D) for a discussion on the thermal issues with the MPC family of clock drivers.


**Rev 2**




All inputs have internal pull–up resistors (appr. 50 K) except for the xtal1 and xtal2 pins.

**Figure 1. 52–Lead Pinout** (Top View)

**FUNCTION TABLE 1**

| fsela1 | fsela0 | Qa | fselb1 | fselb0 | Qb | fselc1 | fselc0 | Qc |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | ÷4 | 0 | 0 | ÷4 | 0 | 0 | ÷2 |
| 0 | 1 | ÷6 | 0 | 1 | ÷6 | 0 | 1 | ÷4 |
| 1 | 0 | ÷8 | 1 | 0 | ÷8 | 1 | 0 | ÷6 |
| 1 | 1 | ÷12 | 1 | 1 | ÷10 | 1 | 1 | ÷8 |

**FUNCTION TABLE 2**

| *fselFB2 | fselFB1 | fselFB0 | QFB |
|---|---|---|---|
| 0 | 0 | 0 | ÷4 |
| 0 | 0 | 1 | ÷6 |
| 0 | 1 | 0 | ÷8 |
| 0 | 1 | 1 | ÷10 |
| 1 | 0 | 0 | ÷8 |
| 1 | 0 | 1 | ÷12 |
| 1 | 1 | 0 | ÷16 |
| 1 | 1 | 1 | ÷20 |

* If the fselFB2 is 1, it may be necessary to apply a reset after power up to ensure synchronization between QFB and the other inputs.

**FUNCTION TABLE 3**

| Control Pin | Logic ‘0’ | Logic ‘1’ |
|---|---|---|
| VCO_Sel | VCO/2 | VCO |
| Ref_Sel | TCLK | Xtal (PECL) |
| TCLK_Sel | TCLK0 | TCLK1 |
| PLL_En | Bypass PLL | Enable PLL |
| $\overline{MR}$/OE | Master Reset/Output Hi–Z | Enable Outputs |
| Inv_Clk | Non–Inverted Qc2, Qc3 | Inverted Qc2, Qc3 |

2

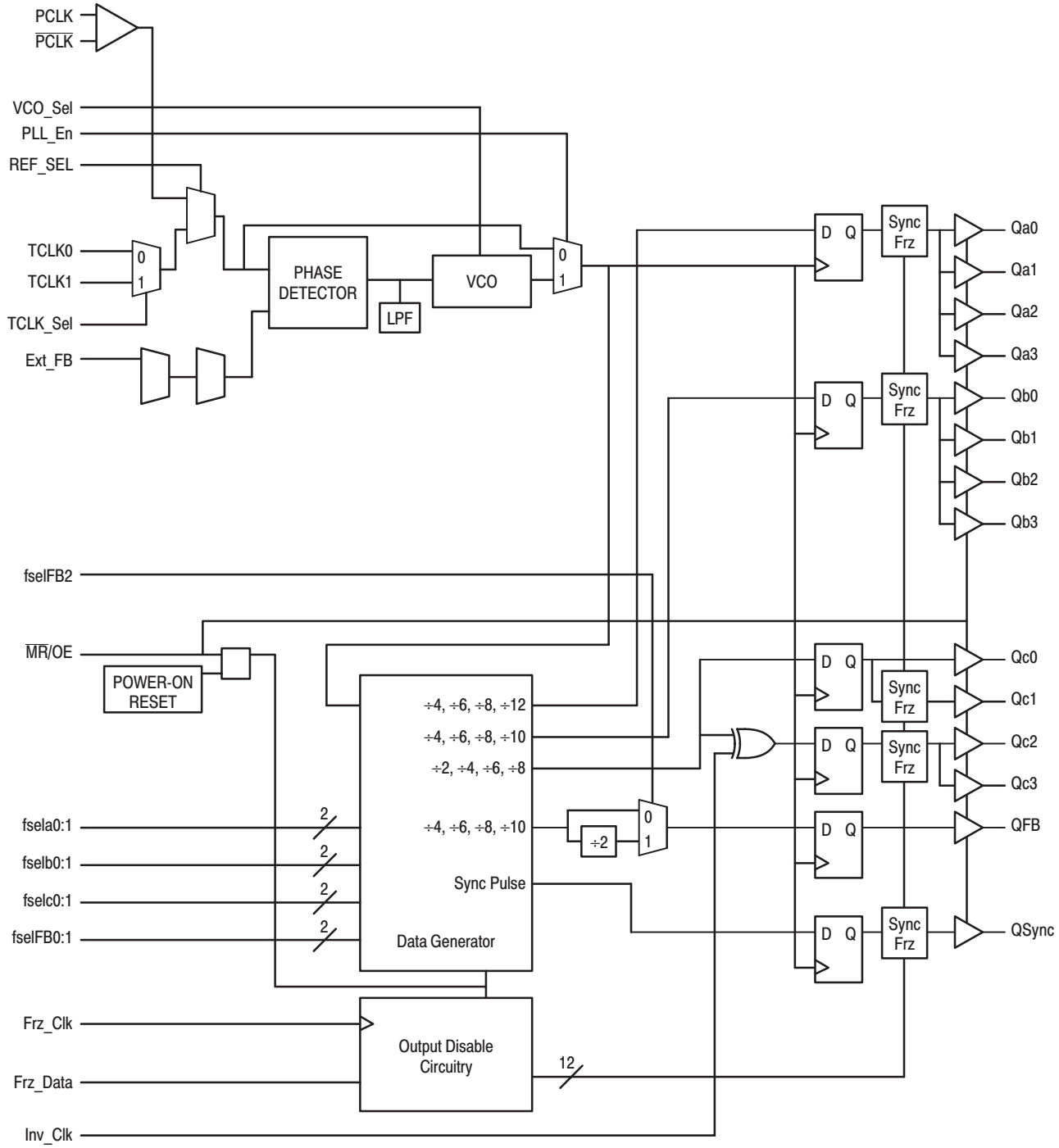



**Figure 2. Logic Diagram**

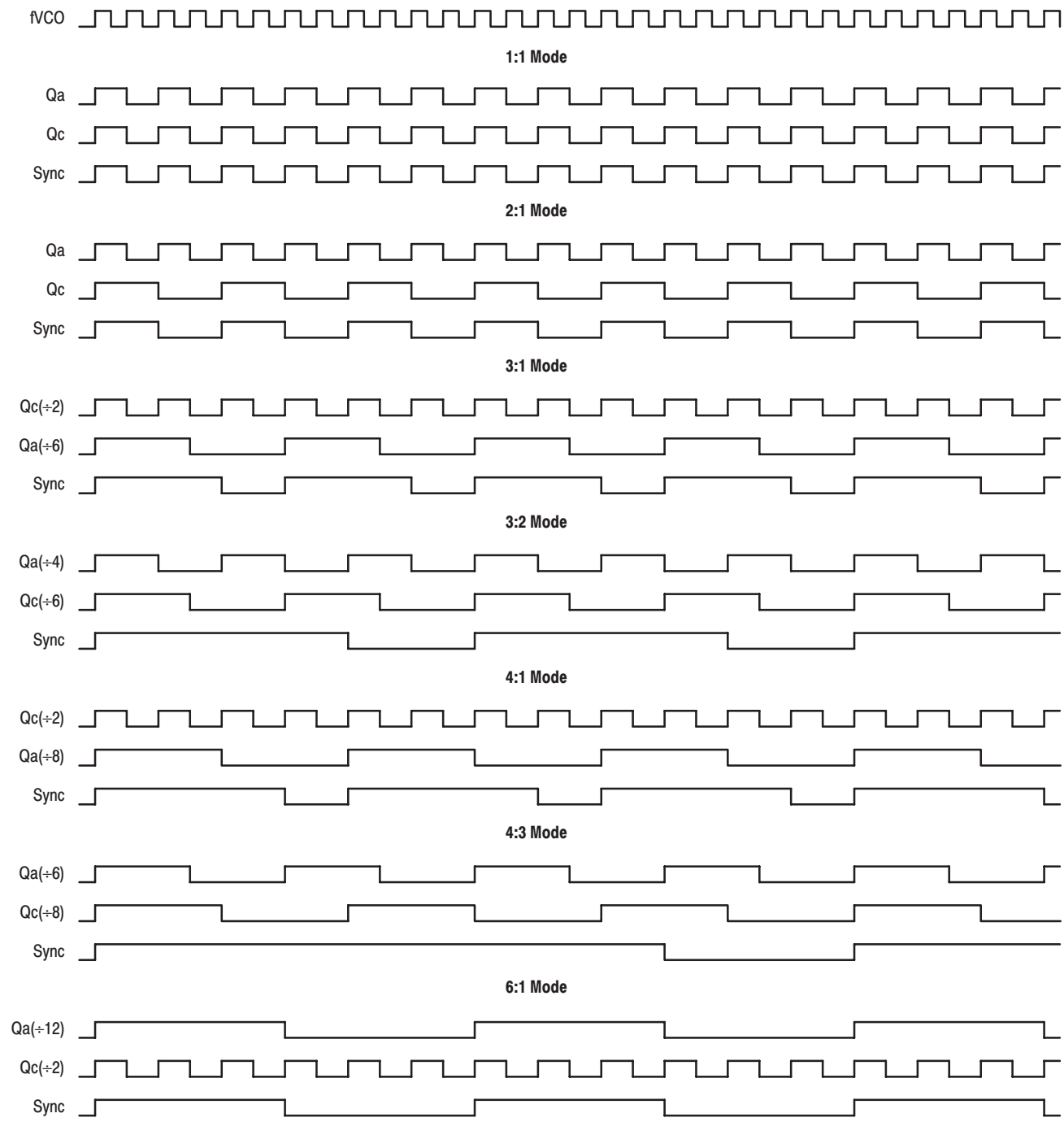



**Figure 3. Timing Diagrams**

**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 4.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | Input Current | | ±20 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

2

**THERMAL CHARACTERISTICS**

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

**DC CHARACTERISTICS** (Note 4.; $T_A$ = 0° to 70°C; $V_{CC}$ = 3.3 V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{CCA}$ | Analog $V_{CC}$ Voltage | 2.935 | | $V_{CC}$ | V | |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | 3.6 | V | |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | |
| $V_{PP}$ | Peak–to–Peak Input Voltage PCLK | 300 | | 1000 | mV | |
| $V_{CMR}$ | Common Mode Range PCLK | $V_{CC}$–2.0 | | $V_{CC}$–0.6 | | Note 1. |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | $I_{OH}$ = –20 mA (Note 2.) |
| $V_{OL}$ | Output LOW Voltage | | | 0.5 | V | $I_{OL}$ = 20 mA (Note 2.) |
| $I_{IN}$ | Input Current | | | ±120 | µA | Note 3. |
| $I_{CC}$ | Maximum Quiescent Supply Current | | 190 | 215 | mA | All VCC PIns |
| $I_{CCA}$ | Analog $V_{CC}$ Current | | 15 | 20 | mA | |
| $C_{IN}$ | Input Capacitance | | | 4 | pF | |
| $C_{pd}$ | Power Dissipation Capacitance | | 25 | | pF | Per Output |

1. $V_{CMR}$ is the difference from the most positive side of the differential input signal. Normal operation is obtained when the “High” input is within the $V_{CMR}$ range and the input lies within the $V_{PP}$ specification.
2. The MPC973 outputs can drive series or parallel terminated 50 Ω (or 50 Ω to $V_{CC}$/2) transmission lines on the incident edge (see Applications Info section).
3. Inputs have pull–up/pull–down resistors which affect input current.
4. Special thermal handling may be required in some configurations.

**PLL INPUT REFERENCE CHARACTERISTICS** ($T_A$ = 0° to 70°C)

| Symbol | Characteristic | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $t_r$, $t_f$ | TCLK Input Rise/Falls | | 3.0 | ns | |
| $f_{ref}$ | Reference Input Frequency | Note 5. | 100<br>Note 5. | MHz | Note 5. |
| $f_{refDC}$ | Reference Input Duty Cycle | 25 | 75 | % | |

5. Maximum input reference frequency is limited by the VCO lock range and the feedback divider or 100MHz, minimum input reference frequency is limited by the VCO lock range and the feedback divider.

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C; $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.15 | | 1.2 | ns | 0.8 to 2.0V, Note 6. |
| $t_{pw}$ | Output Duty Cycle | | $t_{CYCLE}/2$ –750 | $t_{CYCLE}/2$ ±500 | $t_{CYCLE}/2$ +750 | ps | Note 6. |
| $t_{pd}$ | SYNC to Feedback Propagation Delay | TCLK0<br>TCLK1<br>PCLK | –70<br>–130<br>–225 | 130<br>70<br>–25 | 330<br>270<br>175 | ps | Notes 6., 7.; QFB = ÷8 |
| $t_{os}$ | Output-to-Output Skew | | | | 550 | ps | Note 6. |
| $f_{VCO}$ | VCO Lock Range | | 200 | | 480 | MHz | |
| $f_{max}$ | Maximum Output Frequency | Q (÷2)<br>Q (÷4)<br>Q (÷6)<br>Q (÷8) | | | 125<br>120<br>80<br>60 | MHz | Note 6. |
| $t_{jitter}$ | Cycle–to–Cycle Jitter (Peak–to–Peak) | | | ±100 | | ps | Note 6. |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time | | 2 | | 8 | ns | Note 6. |
| $t_{PZL}$, $t_{PZH}$ | Output ENable TIme | | 2 | | 10 | ns | Note 6. |
| $t_{lock}$ | Maximum PLL Lock Time | | | | 10 | ms | |
| $f_{MAX}$ | Maximum Frz_Clk Frequency | | | | 20 | MHz | |

6. 50Ω transmission line terminated into $V_{CC}/2$.
7. $t_{pd}$ is specified for a 50MHz input reference. The window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The $t_{pd}$ does not include jitter.

## APPLICATIONS INFORMATION

**Programming the MPC973**

The MPC973 is the most flexible frequency programming device in the Motorola timing solution portfolio. With three independent banks of four outputs as well as an independent PLL feedback output the total number of possible configurations is too numerous to tabulate. Table 1 tabulates the various selection possibilities for the three banks of outputs. The divide numbers presented in the table represent the divider applied to the output of the VCO for that bank of outputs. To determine the relationship between the three banks the three divide ratios would be compared. For instance if a frequency relationship of 5:3:2 was desired the following selection could be made. The Qb outputs could be set to ÷10, the Qa outputs to ÷6 and the Qc outputs to ÷4. With this output divide selection the desired 5:3:2 relationship would be generated. For situations where the VCO will run at relatively low frequencies the PLL may not be stable for the desired divide ratios. For these circumstances the VCO_Sel pin allows for an extra ÷2 to be added into the clock path. When asserted this pin will maintain the desired output relationships, but will provide an enhanced lock range for the PLL. Once the output frequency relationship is set and the VCO is in its stable range the feedback output would be programmed to match the input reference frequency.

The MPC973 offers only an external feedback to the PLL. A separate feedback output is provided to optimize the flexibility of the device. If in the example above the input reference frequency was equal to the lowest output frequency the feedback output would be set in the ÷10 mode. If the input needed to be half the lowest frequency output the fselFB2 input could be asserted to halve the feedback frequency. This action multiplies the output frequencies by two relative to the input reference frequency. With 7 unique feedback divide capabilities there is a tremendous amount of flexibility. Again assume the above 5:3:2 relationship is needed with the highest frequency output equal to 100 MHz. If one was also constrained because the only reference frequency available was 50MHz the setup in figure 8 could be used. The MPC973 provides the 100, 66 and 40MHz outputs all synthesized from the 50 MHz source. With its multitude of divide ratio capabilities the MPC973 can generate almost any frequency from a standard, common frequency already present in a design. Figures 9 and 10 illustrate a few more examples of possible MPC973 configurations.

The MPC973 has one more programming feature added to its arsenal. The Inv_Clk input pin when asserted will invert the Qc2 and Qc3 outputs. This inversion will not affect the output–output skew of the device. This inversion allows for the development of 180° phase shifted clocks. This output could also be used as a feedback output to the MPC973 or a second PLL device to generate early or late clocks for a specific design. Figure 11 illustrates the use of two MPC973's to generate two banks of clocks with one bank divided by 2 and delayed by 180° relative to the first.

**Using the MPC973 as a Zero Delay Buffer**

The external feedback of the MPC973 clock driver allows for its use as a zero delay buffer. By using one of the outputs as a feedback to the PLL the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The reference frequency affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs. Because the static phase offset is a function of the reference clock the Tpd of the MPC973 is a function of the configuration used.

When used as a zero delay buffer the MPC973 will likely be in a nested clock tree application. For these applications the MPC973 offers a LVPECL clock input as a PLL reference. This allows the user to use LVPECL as the primary clock distribution device to take advantage of its far superior skew performance. The MPC973 then can lock onto the LVPECL reference and translate with near zero delay to low skew LVCMOS outputs. Clock trees implemented in this fashion will show significantly tighter skews than trees developed from CMOS fanout buffers.

To calculate the overall uncertainty between the input reference clock and the output clocks the following approach should be used. Figure 4 through 7 contains performance information to assist in calculating the overall uncertainty. Data presented in Figures 4 through 7 is representative data but is not guaranteed under all conditions. Since the overall skew performance is a function of the input reference frequency all of the graphs provide relavent data with respect to the input reference frequency.

The overall uncertainty can be broken down into three parts; the static phase offset variation (Tpd), the I/O phase jitter and the output skew. If we assume that we have a 75 MHz reference clock, from the graphs we can pull the following information for static phase offset (SPO) and I/O jitter: the SPO variation will be 300 ps (–100 ps to +200 ps assuming a TCLK is used) and the I/O jitter will be ±105 ps (assuming a VCO/6 configuration and a ±3 sigma for min and max). The nominal delay from Figure 5 is 50 ps so that the propagation delay between the reference clock and the feedback clock is 50 ps ±255 ps.

Figure 4 can now be used to establish the uncertainty between the reference clock and all of the outputs for the MPC973. Figure 4 provides the skew of the MC973 outputs with respect to the feedback output. From Figure 4, if all of the outputs are used the propagation delay of the device will range from –555 ps (50 ps – 255 ps – 350 ps) to +705 ps (50 ps + 255 ps + 400 ps) for a total uncertainty of 1.26 ns. This 1.26ns uncertainty would hold true if multiple 973's are used in parallel in the application given that the skew between the reference clock for the devices were zero. Notice from the data in Figure 4 that if a subset of the outputs were used significant reductions in uncertainty could be obtained.

**SYNC Output Description**

In situations where output frequency relationships are not integer multiples of each other there is a need for a signal for system synchronization purposes. The SYNC output of the MPC973 is designed to specifically address this need. The MPC973 monitors the relationship between the Qa and the Qc banks of outputs. It provides a low going pulse, one period in duration, one period prior to the coincident rising edges of the Qa and Qc outputs. The duration and the placement of the pulse is dependent on the higher of the Qa and Qc output frequencies. The timing diagrams in the data sheet show the various waveforms for the SYNC output. Note that the SYNC output is defined for all possible combinations of the Qa and Qc outputs even though under some relationships the lower frequency clock could be used as a synchronizing signal.

**1. Programmable Output Frequency Relationships** (VCO_Sel='1')

| fsela1 | fsela0 | Qa | fselb1 | fselb0 | Qb | fselc1 | fselc0 | Qc |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | VCO/4 | 0 | 0 | VCO/4 | 0 | 0 | VCO/2 |
| 0 | 1 | VCO/6 | 0 | 1 | VCO/6 | 0 | 1 | VCO/4 |
| 1 | 0 | VCO/8 | 1 | 0 | VCO/8 | 1 | 0 | VCO/6 |
| 1 | 1 | VCO/12 | 1 | 1 | VCO/10 | 1 | 1 | VCO/8 |

**2. Programmable Output Frequency Relationships** (VCO_Sel='1')

| fselFB2 | fselFB1 | fselFB0 | QFB |
|---|---|---|---|
| 0 | 0 | 0 | VCO/4 |
| 0 | 0 | 1 | VCO/6 |
| 0 | 1 | 0 | VCO/8 |
| 0 | 1 | 1 | VCO/10 |
| 1 | 0 | 0 | VCO/8 |
| 1 | 0 | 1 | VCO/12 |
| 1 | 1 | 0 | VCO/16 |
| 1 | 1 | 1 | VCO/20 |

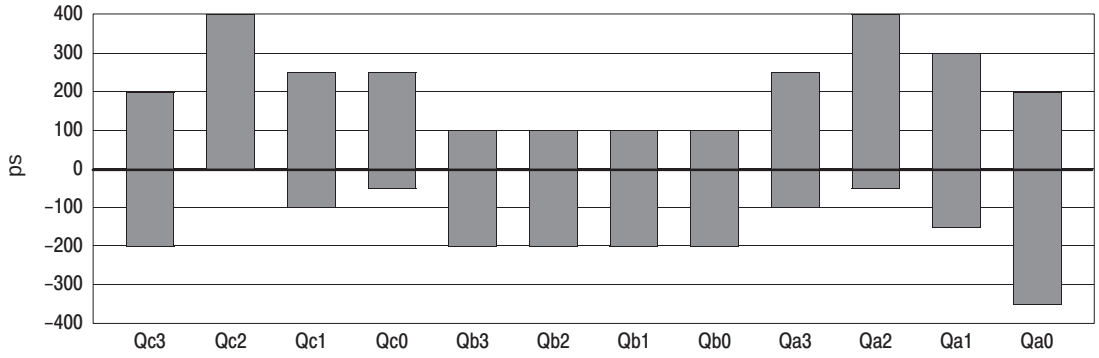



**Figure 4. Typical Skews Relative to QFB**

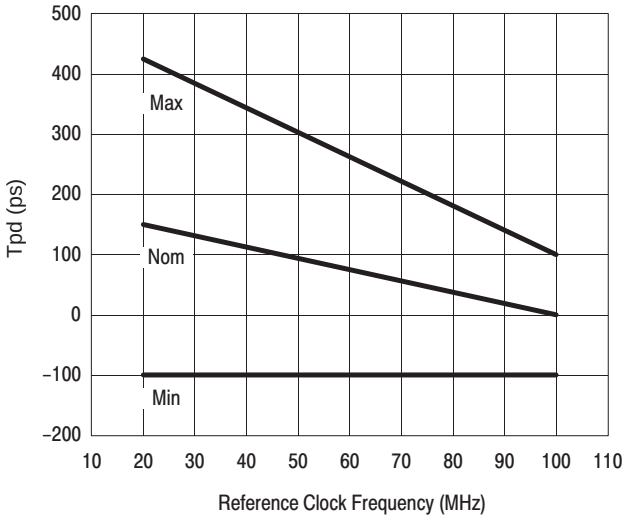



**Figure 5. Typical Static Phase Offset versus Reference Frequency**
$T_{pd}$ versus TCLK

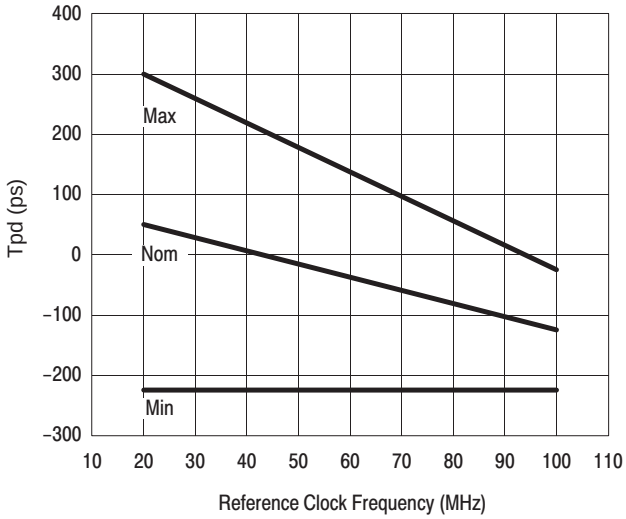



**Figure 6. Typical Static Phase Offset versus Reference Frequency**
$T_{pd}$ versus PCLK

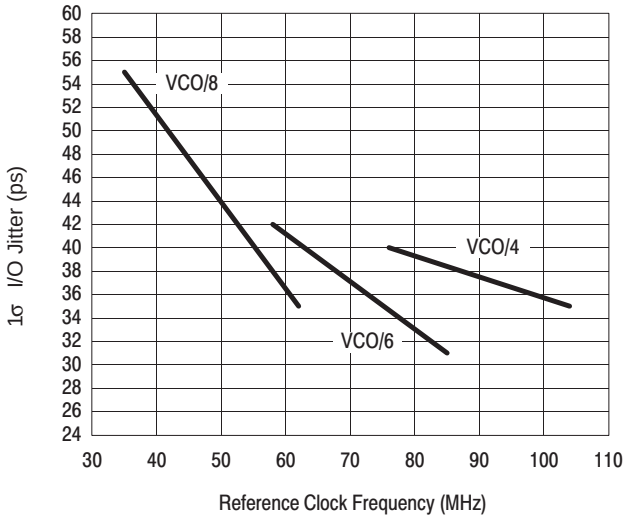



**Figure 7. Typical Phase Jitter versus Reference Frequency**
I/O Jitter

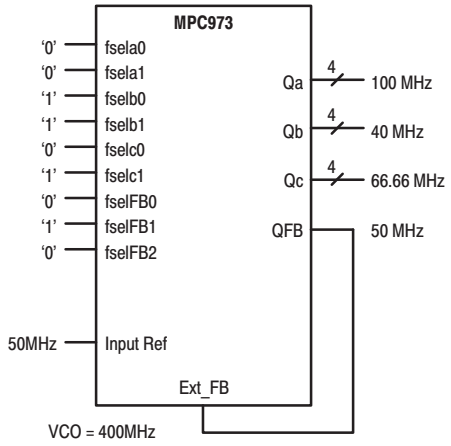



**Figure 8. Programming Configuration Example**

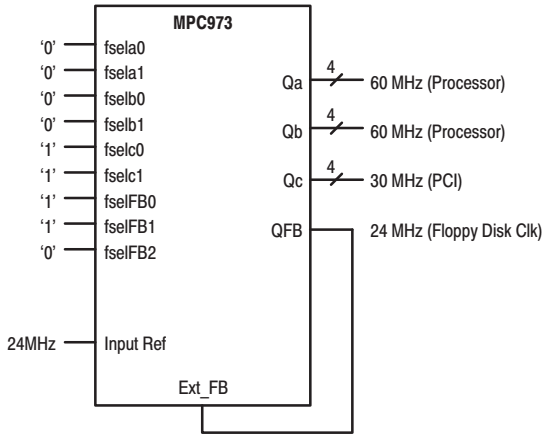



**Figure 9. Generating Pentium Clocks from Floppy Clock**

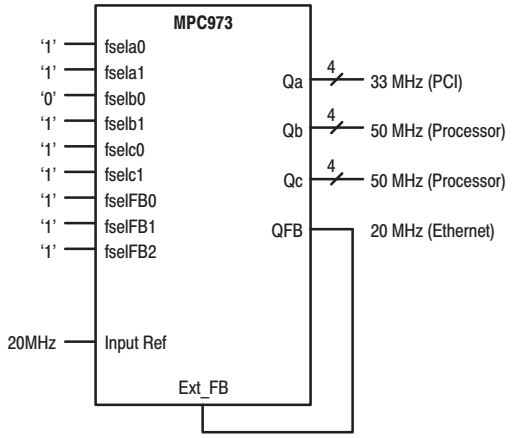



**Figure 10. Generating MPC604 Clocks from Ethernet Clocks**

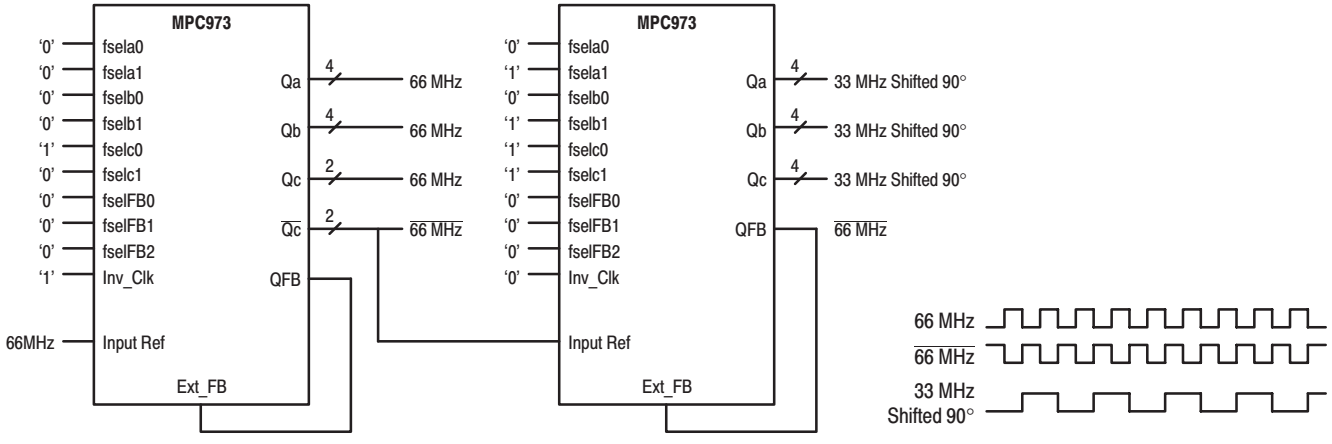



**Figure 11. Phase Delay Using Multiple MPC973's**

**Recommended External Reset Timing**

For MPC973 applications requiring synchronization of the output clock to the input clock and if fselFB2 = 1, the assertion of the $\overline{MR}$ is recommended. The timing of asserting $\overline{MR}$ should be as shown in Figure 12. The power supply should be at or above the minimum specified voltage and the reference clock input (refclk) should be present a minimum of t1 prior to the reset pulse being applied to the $\overline{MR}$ pin.

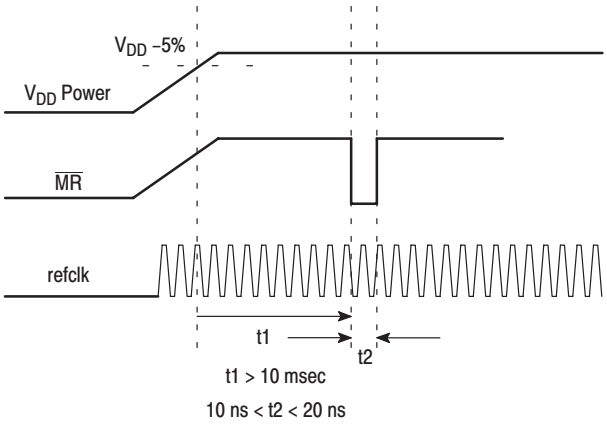



**Figure 12. Assertion of $\overline{MR}$**

**Power Supply Filtering**

The MPC973 is a mixed analog/digital product and exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC973 provides separate power supplies for the output buffers ($V_{CCO}$) and the internal PLL ($V_{CCA}$) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the $V_{CCA}$ pin for the MPC973.

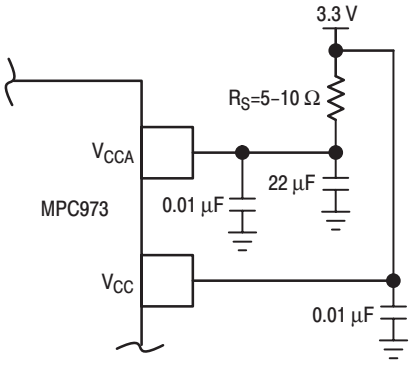



**Figure 13. Power Supply Filter**

Figure 13 illustrates a typical power supply filter scheme. The MPC973 is most susceptible to noise with spectral content in the 1 KHz to 1 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the $V_{CCA}$ pin of the MPC973. From the data sheet the $I_{VCCA}$ current (the current sourced through the $V_{CCA}$ pin) is typically 15 mA (20 mA maximum), assuming that a minimum of 2.935 V must be maintained on the $V_{CCA}$ pin very little DC voltage drop can be tolerated when a 3.3 V $V_{CC}$ supply is used. The resistor shown in Figure 13 must have a resistance of 5–10 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

Although the MPC973 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Driving Transmission Lines**

The MPC973 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated

transmission lines can be used. The parallel technique terminates the signal at the end of the line with a
50 Ω resistance to $V_{CC}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC973 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 14 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC973 clock driver is effectively doubled due to its capability to drive multiple lines.



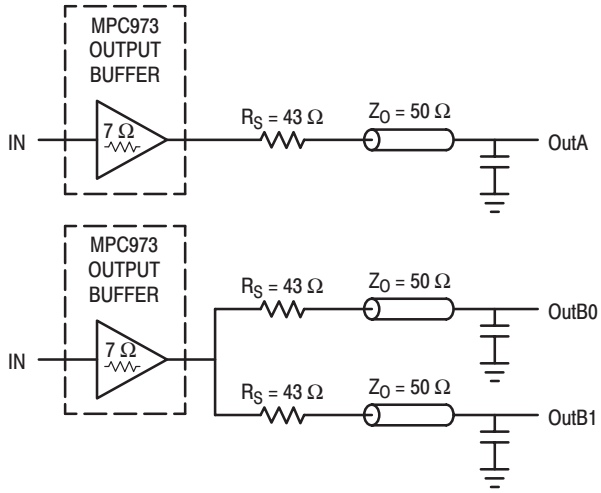



**Figure 14. Single versus Dual Transmission Lines**

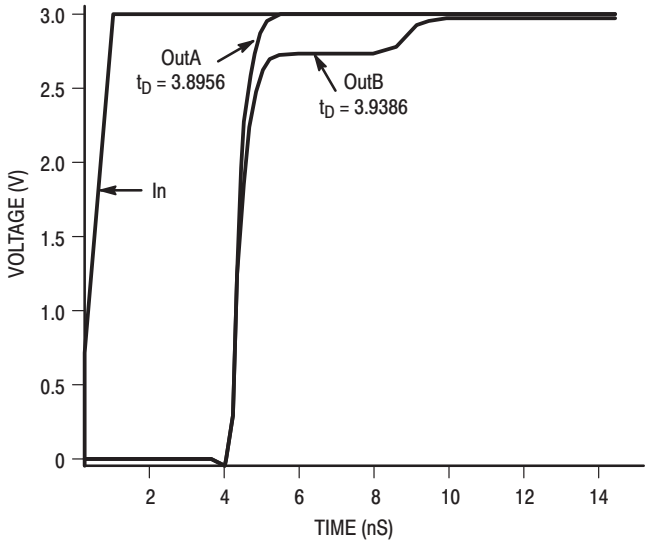
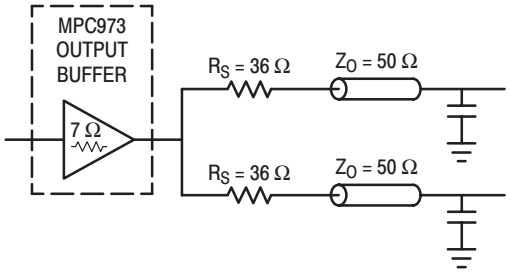



**Figure 15. Single versus Dual Waveforms**




7 Ω + 36 Ω || 36 Ω = 50 Ω || 50 Ω
25 Ω = 25 Ω

**Figure 16. Optimized Dual Line Termination**

The waveform plots of Figure 15 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC973 output buffers is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC973. The output waveform in Figure 15 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

VL = VS ( Zo / Rs + Ro +Zo) = 3.0 (25/53.5) = 1.40 V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 15 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

**Using the Output Freeze Circuitry**

With the recent advent of a “green” classification for computers the desire for unique power management among system designers is keen. The individual output enable control of the MPC973 allows designers, under software control, to implement unique power management schemes into their designs. Although useful, individual output control at the expense of one pin per output is too high, therefore a simple serial interface was derived to economize on the control pins.

The freeze control logic provides a mechanism through which the MPC973 clock outputs may be frozen (stopped in the logic ‘0’ state):

The freeze mechanism allows serial loading of the 12–bit Serial Input Register, this register contains one program– mable freeze enable bit for 12 of the 14 output clocks. The Qc0 and QFB outputs cannot be frozen with the serial port, this avoids any potential lock up situation should an error occur in the loading of the Serial Input Register. The user may program an output clock to freeze by writing logic ‘0’ to the respective freeze enable bit. Likewise, the user may programmably unfreeze an output clock by writing logic ‘1’ to the respective enable bit.

The freeze logic will never force a newly–frozen clock to a logic ‘0’ state before the time at which it would normally

transition there. The logic simply keeps the frozen clock at logic ‘0’ once it is there. Likewise, the freeze logic will never force a newly–unfrozen clock to a logic ‘1’ state before the time at which it would normally transition there. The logic re–enables the unfrozen clock during the time when the respective clock would normally be in a logic ‘0’ state, eliminating the possibility of ‘runt’ clock pulses.

The user may write to the Serial Input register through the Frz_Data input by supplying a logic ‘0’ start bit followed serially by 12 NRZ freeze enable bits. The period of each Frz_Data bit equals the period of the free–running Frz_Clk signal. The Frz_Data serial transmission should be timed so the MPC973 can sample each Frz_Data bit with the rising edge of the free–running Frz_Clk signal.


D0–D3 are the control bits for Qa0–Qa3, respectively
D4–D7 are the control bits for Qb0–Qb3, respectively
D8–D10 are the control bits for Qc1–Qc3, respectively
D11 is the control bit for QSync

**Figure 17. Freeze Data Input Protocol**

2

# 3.3V PLL Clock Driver

**MPC974**

**See Upgrade Product – MPC9774**

**LOW VOLTAGE PLL CLOCK DRIVER**

**FA SUFFIX**
52–LEAD LQFP PACKAGE
CASE 848D-03

2

The MPC974 is a fully integrated PLL based clock generator and clock distribution chip which operates from a 3.3V supply. The MPC974 is ideally suited for high speed, timing critical designs which need a high level of clock fanout. The device features 15 high drive LVCMOS outputs, each output has the capability of driving a 50Ω parallel terminated transmission line or two 50Ω series terminated transmission lines on the incident edge.

- Fully Integrated PLL
- Two Reference Clock Inputs for Redundant Clock Applications
- High Impedance Output Control
- Logic Enable on the Outputs
- 3.3V $V_{CC}$ Supply
- Output Frequency Configurable
- LQFP Packaging
- ±100ps Typical Cycle–to–Cycle Jitter

The MPC974 features 3 independent frequency programmable banks of outputs. The frequency programmability offers the capability of establishing output frequency relationships of 1:1, 2:1, 3:1, 3:2 and 3:2:1. In addition, the device features a separate feedback output which allows for a wide variety of input/output frequency multiplication alternatives. The VCO_Sel pin provides an extended VCO lock range for added flexibility and general purpose usage.

The TCLK0 and TCLK1 inputs provide a method for dynamically switching the PLL between two different clock sources. The PLL has been optimized to provide small deviations in output pulse width and well controlled, slow transition back to lock when the inputs are switched between two references that are equal in frequency but out of phase with each other. This feature makes the MPC974 a solution for fault tolerant applications which require redundant clock sources.

For designs in which fault tolerance is critical, other products may provide more control over the clock switch functions. For these features please refer to the MPC993 datasheet.

All of the control pins are LVTTL/LVCMOS level inputs. The Fsel pins control the VCO divide ratios that are applied to the various output banks and the feedback output. The $\overline{MR}$ input will reset the internal flip flops and place the outputs in high impedance when driven LOW. The OE pin will force all of the outputs except the feedback output LOW to allow for acquiring phase lock prior to providing clocks to the rest of the system. Note that the OE pin is not synchronized to the internal clock. As a result, the initial pulse after de–assertion of the OE pin may be distorted. The PLL_En pin allows the PLL to be bypassed for board level functional test. When bypassed the signal on the selected TCLK will be routed around the PLL and will drive the internal dividers directly.

The MPC974 is packaged in the 52–lead LQFP package to provide optimum electrical performance as well as minimize board space requirements. The device is specified for 3.3V $V_{CC}$.

**Rev 3**

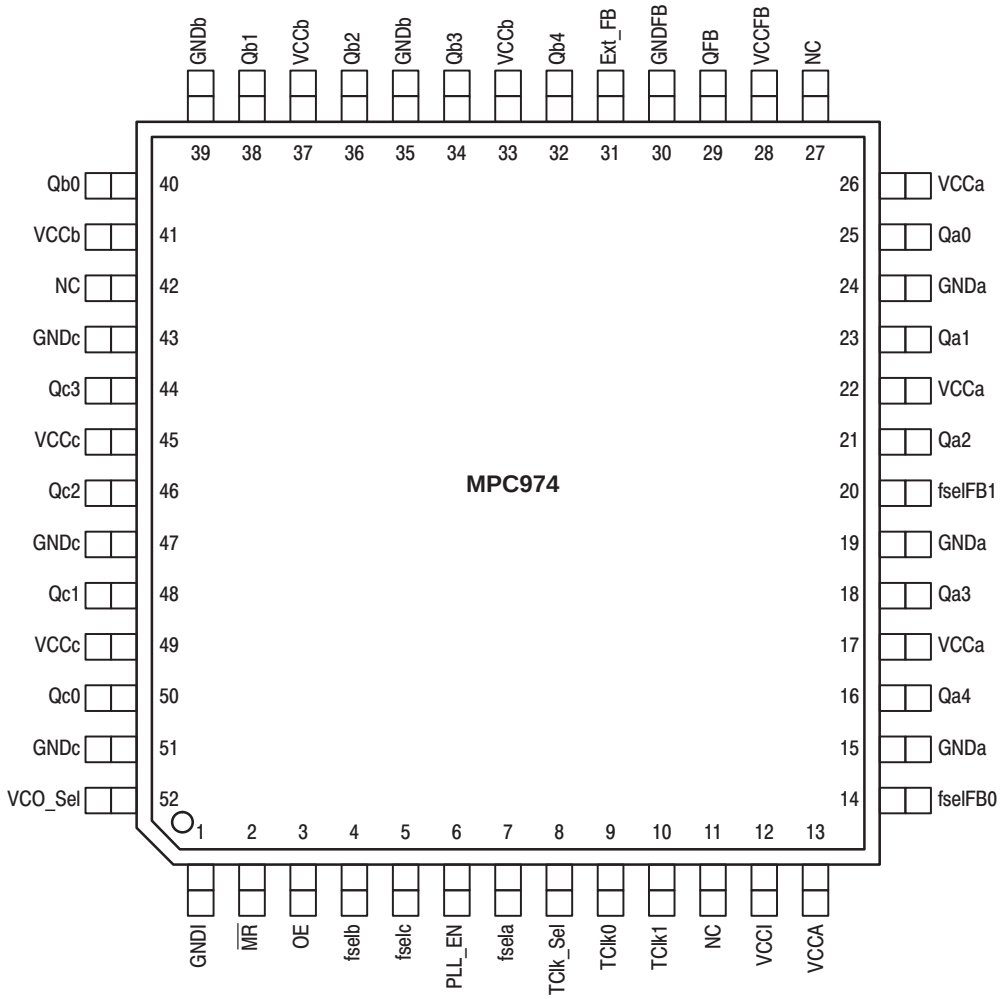



**Figure 1. 52–Lead Pinout** (Top View)

**FUNCTION TABLE 1**

| fsela | Qa | fselb | Qb | fselc | Qc |
|---|---|---|---|---|---|
| 0 | ÷2 | 0 | ÷2 | 0 | ÷4 |
| 1 | ÷4 | 1 | ÷4 | 1 | ÷6 |

**FUNCTION TABLE 2**

| fselFB0 | fselFB1 | QFB |
|---|---|---|
| 0 | 0 | ÷4 |
| 0 | 1 | ÷6 |
| 1 | 0 | ÷8 |
| 1 | 1 | ÷12 |

**FUNCTION TABLE 3**

| VCO_Sel | fVCO |
|---|---|
| 0 | VCO/2 |
| 1 | VCO/4 |

**FUNCTION TABLE 4**

| Control Pin | Logic ‘0’ | Logic ‘1’ |
|---|---|---|
| $\overline{MR}$ | Master Reset/Output High Z | – |
| PLL_EN | Bypass PLL | Enable PLL |
| TClk_Sel | TCLK0 | TCLK1 |
| OE | Qa, Qb, Qc Logic LOW | All Outputs Enabled |

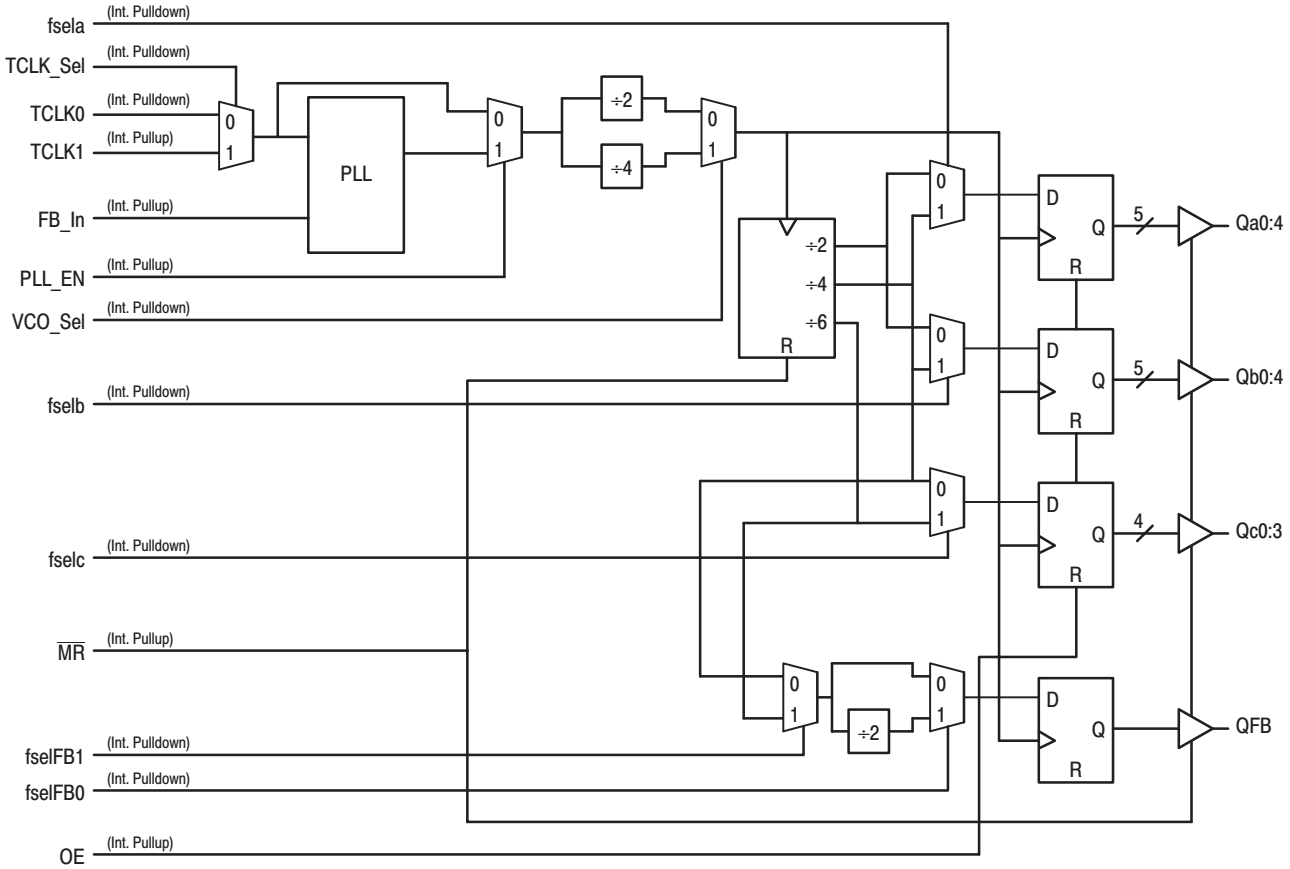



**Figure 2. Logic Diagram**

**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 5.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | Input Current | | 8 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

**THERMAL CHARACTERISTICS**

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | $V_{CC}$ | V | |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | $I_{OH}$ = –20mA (Note 1.) |
| $V_{OL}$ | Output LOW Voltage | | | 0.5 | V | $I_{OL}$ = 20mA (Note 1.) |
| $I_{IN}$ | Input Current | | | ±100 | µA | Note 2. |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | 120 | mA | |
| $C_{IN}$ | Input Capacitance | | | 8 | pF | |
| $C_{pd}$ | Power Dissipation Capacitance | | 25 | | pF | Per Output |

1. The MPC974 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}$/2) transmission lines on the incident edge (see Applications Info section).
2. Inputs have either pull–up or pull–down resistors which affect input current.

**PLL INPUT REFERENCE CHARACTERISTICS** ($T_A$ = 0 to 70°C)

| Symbol | Characteristic | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $t_r$, $t_f$ | TCLK Input Rise/Falls | | 3.0 | ns | |
| $f_{ref}$ | Reference Input Frequency | Note 3. | Note 3. | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | 25 | 75 | % | |

3. Input reference frequency is limited by the divider selection and the VCO lock range.

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.15 | | 1.5 | ns | 0.8 to 2.0V, Note 4. |
| $t_{pw}$ | Output Duty Cycle | $t_{CYCLE}/2$ –800 | $t_{CYCLE}/2$ ±500 | $t_{CYCLE}/2$ +800 | ps | Note 4. |
| $f_{VCO}$ | PLL VCO Lock Range fseln, fselFBn = ÷4 to ÷12 | 200 | | 500 | MHz | Note 5. |
| $t_{pd}$ | SYNC to Feedback Propagation Delay | –250 | | 100 | ps | Notes 4., 6. |
| $t_{os}$ | Output-to-Output Skew | | | 350 | ps | Note 4. |
| $f_{max}$ | Maximum Output Frequency Q (÷2)<br>Q (÷4)<br>Q (÷6) | | | 125<br>63<br>42 | MHz | VCO_Sel = 0 |
| $t_{PZL}$ | Output Enable Time | 2 | | 10 | ns | Note 4. |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time | 2 | | 10 | ns | Note 4. |
| $t_{jitter}$ | Cycle–to–Cycle Jitter (Peak–to–Peak) | | ±100 | | ps | Note 4. |
| $t_{lock}$ | Maximum PLL Lock Time | | | 10 | ms | |

4. 50Ω transmission lines terminated to $V_{CC}$/2.
5. The PLL will be unstable if the total divide between the VCO and the feedback pin is less < 8. VCO_SEL = '0', fsela or fselb = '0' cannot be used for the PLL feedback signal.
6. $t_{pd}$ is specified for 50MHz input reference. The window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The $t_{pd}$ does not include jitter.

## APPLICATIONS INFORMATION

### Programming the MPC974

The MPC974 clock driver outputs can be configured into several frequency relationships, in addition the external feedback option allows for a great deal of flexibility in establishing unique input–to–output frequency relationships. The output dividers for the four output groups allows the user to configure the outputs into 1:1, 2:1, 3:2 and 3:2:1 frequency ratios. The use of even dividers ensures that the output duty cycle is always 50%. Function Table 1 illustrates the various output configurations, the table describes the outputs using the VCO frequency as a reference. As an example for a 3:2:1 relationship the Qa outputs would be set at VCO/2, the Qb's and Qc's at VCO/4 and the Qd's at VCO/6. These settings will provide output frequencies with a 3:2:1 relationship.

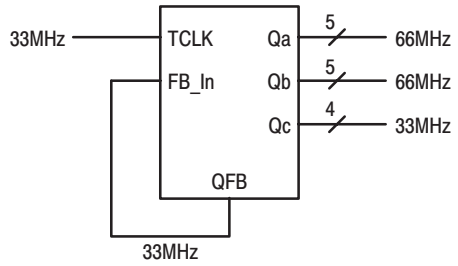
The division settings establish the output relationship, but one must still ensure that the VCO will be stable given the frequency of the outputs desired. The VCO lock range can be found in the specification tables. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL is such that for output frequencies between 10 and 125MHz the MPC974 can generally be configured into a stable region.

The relationship between the input reference and the output frequency is also very flexible. The separate PLL feedback output allows for a wide range of output vs input frequency relationships. Function Table 1 can be used to identify the potential relationships available. Figure 3 illustrates several programming possibilities, although not exhaustive it is representative of the potential applications.

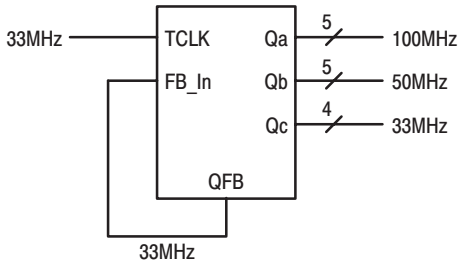
### Using the MPC974 as a Zero Delay Buffer

The external feedback option of the MPC974 clock driver allows for its use as a zero delay buffer. By using one of the outputs as a feedback to the PLL the propagation delay through the device is near zero. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The static phase offset is a function of the input reference frequency of the MPC974. The Tpd of the device is specified in the specification tables.

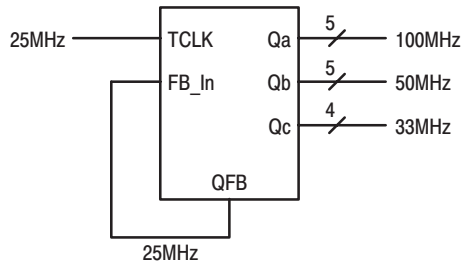
To minimize part–to–part skew the external feedback option again should be used. The PLL in the MPC974 decouples the delay of the device from the propagation delay variations of the internal gates. From the specification table one sees a Tpd variation of only ±150ps, thus for multiple devices under identical configurations the part–to–part skew will be around 850ps (300ps for Tpd variation plus 350ps output–to–output skew plus 200ps for jitter). To minimize this value, the highest possible reference frequencies should be used. Higher reference frequencies will minimize both the $t_{pd}$ parameter as well as the input to output jitter.



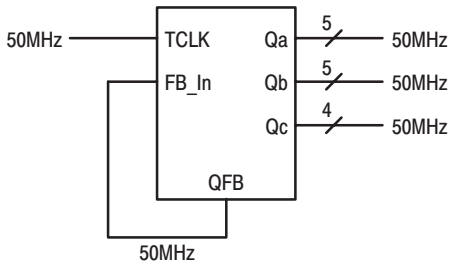

| fsela | fselb | fselc | fselFB | VCO_Sel |
|---|---|---|---|---|
| 0 | 0 | 0 | 00 | 0 |




| fsela | fselb | fselc | fselFB | VCO_Sel |
|---|---|---|---|---|
| 0 | 1 | 1 | 10 | 0 |




| fsela | fselb | fselc | fselFB | VCO_Sel |
|---|---|---|---|---|
| 0 | 1 | 1 | 01 | 0 |




| fsela | fselb | fselc | fselFB | VCO_Sel |
|---|---|---|---|---|
| 1 | 1 | 0 | 00 | 0 |

**Figure 3. MPC974 Programming Schemes**

**Power Supply Filtering**

The MPC974 is a mixed analog/digital product and exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC974 provides separate power supplies for the output buffers ($V_{CCO}$) and the internal PLL (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC974.

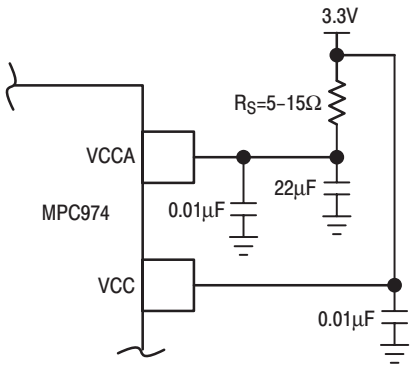



**Figure 4. Power Supply Filter**

Figure 4 illustrates a typical power supply filter scheme. The MPC974 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the VCCA pin of the MPC974. From the data sheet the $I_{VCCA}$ current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V $V_{CC}$ supply is used. The resistor shown in Figure 4 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

Although the MPC974 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Driving Transmission Lines**

The MPC974 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

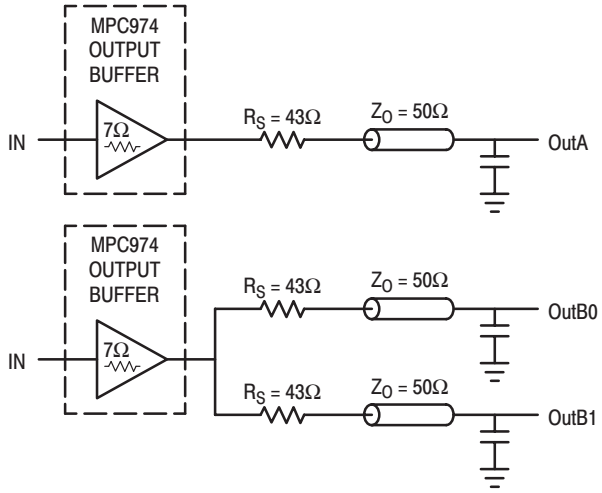



**Figure 5. Single versus Dual Transmission Lines**

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC974 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 5 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC974 clock driver is effectively doubled due to its capability to drive multiple lines.

The waveform plots of Figure 6 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC974 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC974. The output waveform in Figure 6 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

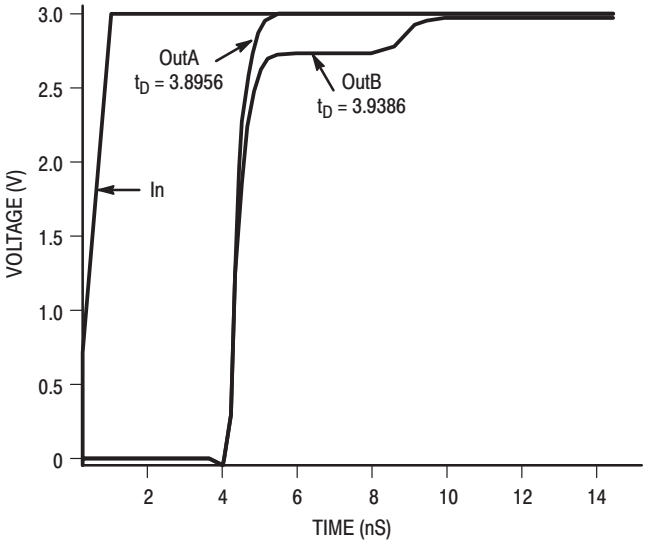


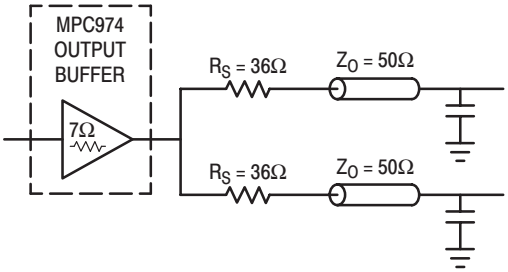

**Figure 6. Single versus Dual Waveforms**

VL = VS ( Zo / Rs + Ro +Zo) = 3.0 (25/53.5) = 1.40V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 7 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.




7Ω + 36Ω || 36Ω = 50Ω || 50Ω
25Ω = 25Ω

**Figure 7. Optimized Dual Line Termination**

**Order Number: MPC9772/D**
**Rev 0, 12/2001**

*Product Preview*

# 3.3V/2.5V 1:12 LVCMOS PLL Clock Generator

**MPC9772**

**3.3V/2.5V 1:12 LVCMOS PLL CLOCK GENERATOR**

**FA SUFFIX**
52 LEAD LQFP PACKAGE
CASE 848D

2

The MPC9772 is a 3.3V or 2.5V compatible, 1:12 PLL based clock generator targeted for high performance low-skew clock distribution in mid-range to high-performance networking, computing and telecom applications. With output frequencies up to 240 MHz and output skews less than 300 ps[1] the device meets the needs of the most demanding clock applications.

**Features**

- 1:12 PLL based low-voltage clock generator
- 2.5V or 3.3V power supply
- Generates clock signals up to 240 MHz
- Maximum output skew of 300 ps[1]
- On-chip crystal oscillator clock reference
- Two LVCMOS PLL reference clock inputs
- External PLL feedback supports zero-delay capability
- Various feedback and output dividers (see application section)
- Supports up to three individual generated output clock frequencies
- Synchronous output clock stop circuitry for each individual output for power down support
- Drives up to 24 clock lines
- Ambient temperature range 0°C to +85°C
- Pin and function compatible to the MPC972

**Functional Description**

The MPC9772 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9772 requires the connection of the PLL feedback output QFB to feedback input FB_IN to close the PLL feedback path. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. The MPC9772 features an extensive level of frequency programmability between the 12 outputs as well as the output to input relationships, for instance 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 5:1, 5:2, 5:3, 5:4, 5:6, 6:1, 8:1 and 8:3.

The QSYNC output will indicate when the coincident rising edges of the above relationships will occur. The selectability of the feedback frequency is independent of the output frequencies. This allows for very flexible programming of the input reference versus output frequency relationship. The output frequencies can be either odd or even multiples of the input reference. In addition the output frequency can be less than the input frequency for applications where a frequency needs to be reduced by a non–binary factor. The MPC9772 also supports the 180º phase shift of one of its output banks with respect to the other output banks. The QSYNC outputs reflects the phase relationship between the QA and QC outputs and can be used for the generation of system baseline timing signals.

The REF_SEL pin selects the internal crystal oscillator or the LVCMOS compatible inputs as the reference clock signal. Two alternative LVCMOS compatible clock inputs are provided for clock redundancy support. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply.

The outputs can be individually disabled (stopped in logic low state) by programming the serial CLOCK_STOP interface of the MPC9772. The MPC9772 requires an external reset signal for start-up and and for PLL recovery in the case the external feedback is interrupted.

The MPC9772 is fully 2.5V and 3.3V compatible and requires no external loop filter components. All inputs (except XTAL) accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9772 outputs can drive one or two traces giving the devices an effective fanout of 1:24. The device is pin and function compatible to the MPC972 and is packaged in a 52-lead LQFP package.

1. Final specification of this parameter is pending characterization.



**Rev 0**

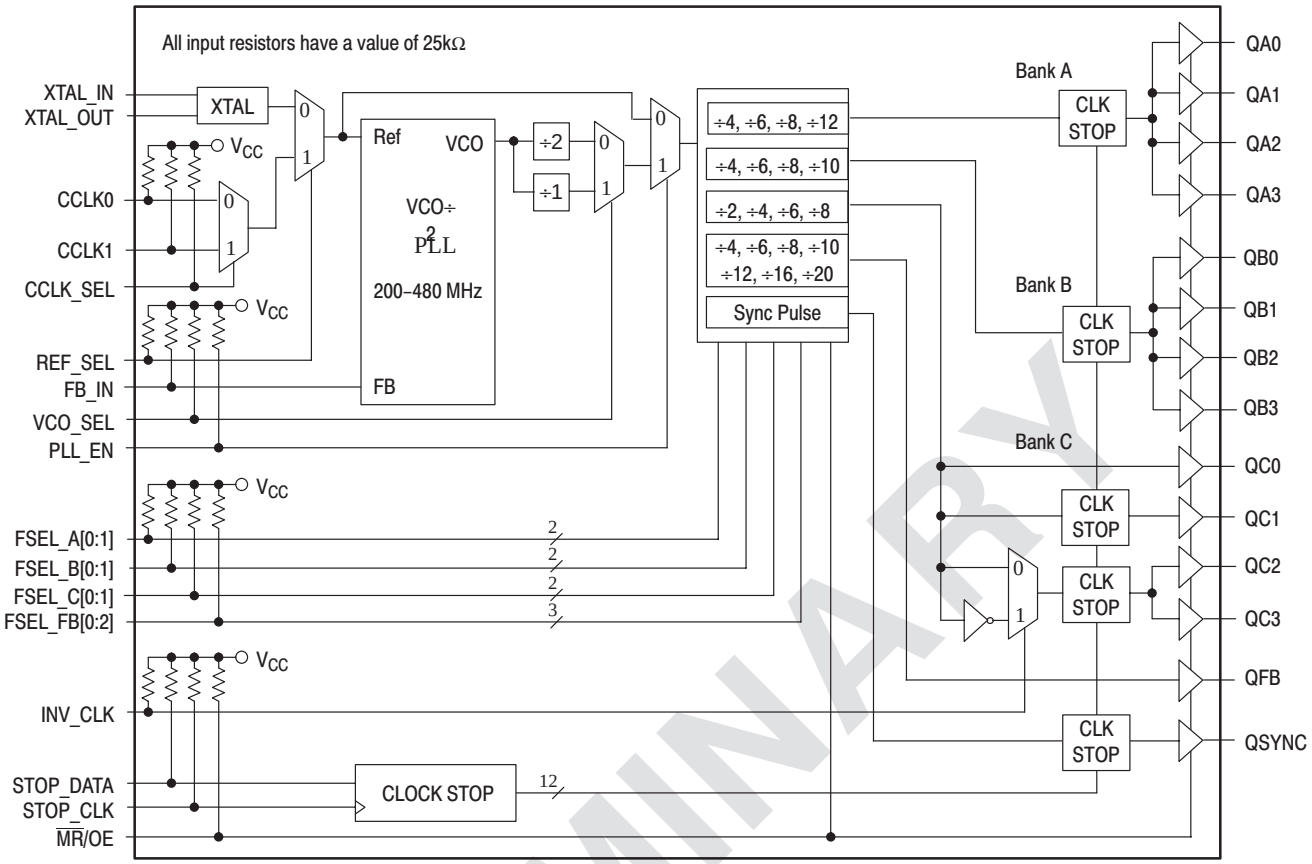



**Figure 1. MPC9772 Logic Diagram**

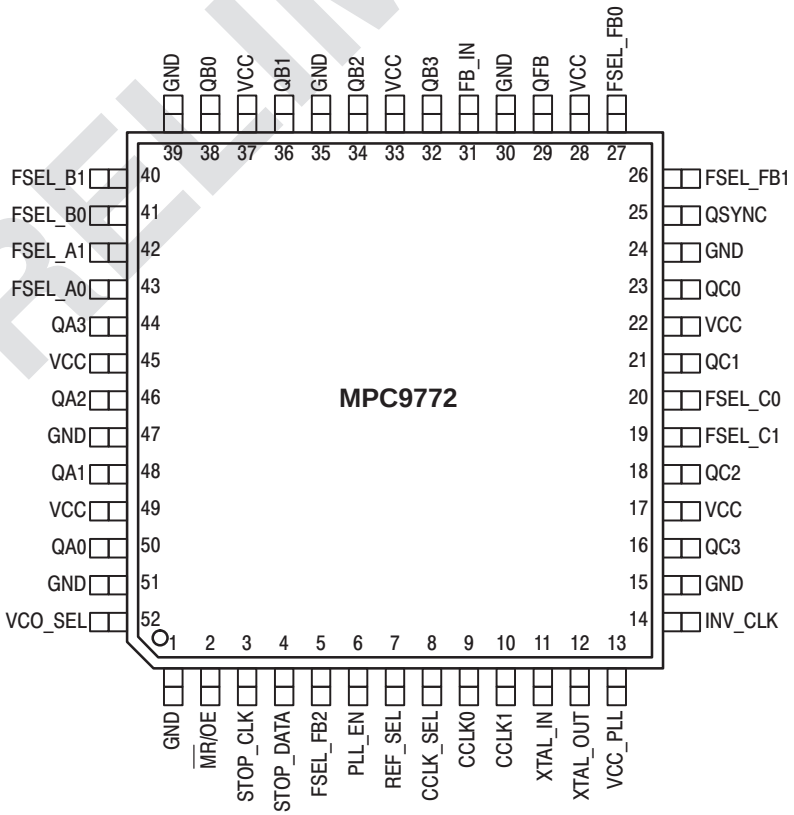



**Figure 2. MPC9772 52–Lead Package Pinout** (Top View)

**Table 1: PIN CONFIGURATION**

| Pin | I/O | Type | Function |
|---|---|---|---|
| CCLK0 | Input | LVCMOS | PLL reference clock |
| CCLK1 | Input | LVCMOS | Alternative PLL reference clock |
| XTAL_IN, XTAL_OUT | | Analog | Crystal oscillator interface |
| FB_IN | Input | LVCMOS | PLL feedback signal input, connect to an QFB |
| CCLK_SEL | Input | LVCMOS | LVCMOS clock reference select |
| REF_SEL | Input | LVCMOS | LVCMOS/PECL reference clock select |
| VCO_SEL | Input | LVCMOS | VCO operating frequency select |
| PLL_EN | Input | LVCMOS | PLL enable/PLL bypass mode select |
| $\overline{MR}$/OE | Input | LVCMOS | Output enable/disable (high-impedance tristate) and device reset |
| FSEL_A[0:1] | Input | LVCMOS | Frequency divider select for bank A outputs |
| FSEL_B[0:1] | Input | LVCMOS | Frequency divider select for bank B outputs |
| FSEL_C[0:1] | Input | LVCMOS | Frequency divider select for bank C outputs |
| FSEL_FB[0:2] | Input | LVCMOS | Frequency divider select for the QFB output |
| INV_CLK | Input | LVCMOS | Clock phase selection for outputs QC2 and QC3 |
| STOP_CLK | Input | LVCMOS | Clock input for clock stop circuitry |
| STOP_DATA | Input | LVCMOS | Configuration data input for clock stop circuitry |
| QA[0-3] | Output | LVCMOS | Clock outputs (Bank A) |
| QB[0-3] | Output | LVCMOS | Clock outputs (Bank B) |
| QC[0-3] | Output | LVCMOS | Clock outputs (Bank C) |
| QFB | Output | LVCMOS | PLL feedback output. Connect to FB_IN. |
| QSYNC | Output | LVCMOS | Synchronization pulse output |
| GND | Supply | Ground | Negative power supply |
| VCC_PLL | Supply | VCC | PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin $V_{CC\_PLL}$. Please see applications section for details. |
| VCC | Supply | VCC | Positive power supply for I/O and core. All VCC pins must be connected to the positive power supply for correct operation |

**Table 2: FUNCTION TABLE (Configuration Controls)**

| Control | Default | 0 | 1 |
|---|---|---|---|
| REF_SEL | 1 | Selects CCLKx as the PLL reference clock | Selects the crystal oscillator as the PLL reference clock |
| CCLK_SEL | 1 | Selects CCLK0 | Selects CCLK1 |
| VCO_SEL | 1 | Selects VCO÷1. (high VCO frequency range) | Selects VCO÷2. The VCO frequency is scaled by a factor of 2 (low VCO frequency range). |
| PLL_EN | 1 | Test mode with the PLL bypassed. The reference clock is substituted for the internal VCO output. MPC9772 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable. | Normal operation mode with PLL enabled. |
| INV_CLK | 1 | QC2 and QC3 are in phase with QC0 and QC1 | QC2 and QC3 are inverted (180° phase shift) with respect to QC0 and QC1 |
| $\overline{MR}$/OE | 1 | Outputs disabled (high-impedance state) and reset of the device. During reset/output disable the PLL feedback loop is open and the internal VCO is tied to its lowest frequency. The MPC9772 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLKx). | Outputs enabled (active) |
| VCO_SEL, FSEL_A[0:1], FSEL_B[0:1], FSEL_C[0:1], FSEL_FB[0:2] control the operating PLL frequency range and input/output frequency ratios. See Table 3 to Table 6 and the applications section for supported frequency ranges and output to input frequency ratios. | | | |

**Table 3: Output Divider Bank A ($N_A$)**

| VCO_SEL | FSEL_A1 | FSEL_A0 | QA[0:3] |
|---|---|---|---|
| 0 | 0 | 0 | VCO÷8 |
| 0 | 0 | 1 | VCO÷12 |
| 0 | 1 | 0 | VCO÷16 |
| 0 | 1 | 1 | VCO÷24 |
| 1 | 0 | 0 | VCO÷4 |
| 1 | 0 | 1 | VCO÷6 |
| 1 | 1 | 0 | VCO÷8 |
| 1 | 1 | 1 | VCO÷12 |

**Table 4: Output Divider Bank B ($N_B$)**

| VCO_SEL | FSEL_B1 | FSEL_B0 | QB[0:3] |
|---|---|---|---|
| 0 | 0 | 0 | VCO÷8 |
| 0 | 0 | 1 | VCO÷12 |
| 0 | 1 | 0 | VCO÷16 |
| 0 | 1 | 1 | VCO÷20 |
| 1 | 0 | 0 | VCO÷4 |
| 1 | 0 | 1 | VCO÷6 |
| 1 | 1 | 0 | VCO÷8 |
| 1 | 1 | 1 | VCO÷10 |

**Table 5: Output Divider Bank C ($N_C$)**

| VCO_SEL | FSEL_C1 | FSEL_C0 | QC[0:3] |
|---|---|---|---|
| 0 | 0 | 0 | VCO÷4 |
| 0 | 0 | 1 | VCO÷8 |
| 0 | 1 | 0 | VCO÷12 |
| 0 | 1 | 1 | VCO÷16 |
| 1 | 0 | 0 | VCO÷2 |
| 1 | 0 | 1 | VCO÷4 |
| 1 | 1 | 0 | VCO÷6 |
| 1 | 1 | 1 | VCO÷8 |

**Table 6: Output Divider PLL Feedback (M)**

| VCO_SEL | FSEL_FB2 | FSEL_FB1 | FSEL_FB0 | QFB |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | VCO÷8 |
| 0 | 0 | 0 | 1 | VCO÷12 |
| 0 | 0 | 1 | 0 | VCO÷16 |
| 0 | 0 | 1 | 1 | VCO÷20 |
| 0 | 1 | 0 | 0 | VCO÷16 |
| 0 | 1 | 0 | 1 | VCO÷24 |
| 0 | 1 | 1 | 0 | VCO÷32 |
| 0 | 1 | 1 | 1 | n/a |
| 1 | 0 | 0 | 0 | VCO÷4 |
| 1 | 0 | 0 | 1 | VCO÷6 |
| 1 | 0 | 1 | 0 | VCO÷8 |
| 1 | 0 | 1 | 1 | VCO÷10 |
| 1 | 1 | 0 | 0 | VCO÷8 |
| 1 | 1 | 0 | 1 | VCO÷12 |
| 1 | 1 | 1 | 0 | VCO÷16 |
| 1 | 1 | 1 | 1 | VCO÷20 |

**Table 7: GENERAL SPECIFICATIONS**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output Termination Voltage | | $V_{CC} \div 2$ | | V | |
| MM | ESD Protection (Machine Model) | 200 | | | V | |
| HBM | ESD Protection (Human Body Model) | 2000 | | | V | |
| LU | Latch–Up Immunity | 200 | | | mA | |
| $C_{PD}$ | Power Dissipation Capacitance | | 12 | | pF | Per output |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | Inputs |

2

**Table 8: ABSOLUTE MAXIMUM RATINGS[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage Temperature | -65 | 125 | °C | |

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 9: DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = 0° to 85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{CC\_PLL}$ | PLL Supply Voltage | 2.325 | | $V_{CC}$ | V | LVCMOS |
| $V_{IH}$ | Input High Voltage | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | | | 0.8 | V | LVCMOS |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$=-24 mA[a] |
| $V_{OL}$ | Output Low Voltage | | | 0.55<br>0.30 | V<br>V | $I_{OL}$= 24 mA<br>$I_{OL}$= 12 mA |
| $Z_{OUT}$ | Output Impedance | | 14 - 17 | | Ω | |
| $I_{IN}$ | Input Current[b] | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CC\_PLL}$ | Maximum PLL Supply Current | | 3.0 | 5.0 | mA | $V_{CC\_PLL}$ Pin |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a. The MPC9772 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

b. Inputs have pull–down resistors affecting the input current.

**Table 10: AC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = 0° to 85°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input reference frequency | ÷4 feedback | 50.0 | | 120.0 | MHz | PLL locked |
| | | ÷6 feedback | 33.3 | | 80.0 | MHz | |
| | | ÷8 feedback | 25.0 | | 60.0 | MHz | |
| | | ÷10 feedback | 20.0 | | 48.0 | MHz | |
| | | ÷12 feedback | 16.6 | | 40.0 | MHz | |
| | | ÷16 feedback | 12.5 | | 30.0 | MHz | |
| | | ÷24 feedback | 8.33 | | 20.0 | MHz | |
| | | ÷32 feedback | 6.25 | | 15 | MHz | |
| | Input reference frequency in PLL bypass mode[c] | | | | TBD | MHz | PLL bypass |
| $f_{VCO}$ | VCO frequency range[d] | | 200 | | 480 | MHz | |
| $f_{XTAL}$ | Crystal interface frequency range[e] | | 10 | | 25 | MHz | |
| $f_{MAX}$ | Output Frequency | ÷2 output | 100.0 | | 240.0 | MHz | PLL locked |
| | | ÷4 output | 50.0 | | 120.0 | MHz | |
| | | ÷6 output | 33.3 | | 80.0 | MHz | |
| | | ÷8 output | 25.0 | | 60.0 | MHz | |
| | | ÷10 output | 20.0 | | 48.0 | MHz | |
| | | ÷12 output | 16.6 | | 40.0 | MHz | |
| | | ÷16 output | 12.5 | | 30.0 | MHz | |
| | | ÷20 output | 10.0 | | 24.0 | MHz | |
| | | ÷24 output | 8.33 | | 20.0 | | |
| $f_{STOP\_CLK}$ | Serial interface clock frequency | | | | 20 | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | | 60 | % | |
| tr, tf | CCLKx Input Rise/Fall Time | | | | 1.0 | ns | 0.8 to 2.0V |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) CCLKx or FB_IN | | | ±150 | | ps | PLL locked |
| $t_{sk(O)}$ | Output-to-output Skew[f] | | | | 300 | ps | |
| DC | Output duty cycle | | 45 | 50 | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.55 to 2.4V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 8 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 8 | ns | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ)[g] | | TBD | | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | TBD | | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1 σ) | | TBD | | ps | |
| BW | PLL closed loop bandwidth[h] | | | | | kHz | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 10 | | ms | |

a All AC characteristics are design targets and subject to change upon device characterization.
b AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
c In bypass mode, the MPC9772 divides the input reference clock.
d The input reference frequency must match the VCO lock range divided by the total feedback divider ratio: $f_{ref} = f_{VCO} \div (M \cdot VCO\_SEL)$
e The crystal frequency range must both meet the interface frequency range and VCO lock range divided by the feedback divider ratio: $f_{XTAL(min, max)} = f_{VCO(min, max)} \div (M \cdot VCO\_SEL)$ and $10\ MHz \le f_{XTAL} \le 25\ MHz$.
f See application section for part-to-part skew calculation.
g See application section for a jitter calculation for other confidence factors than 1 σ.
h -3 dB point of PLL transfer characteristics.

**Table 11: DC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = 0° to 85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{CC\_PLL}$ | PLL Supply Voltage | 2.325 | | $V_{CC}$ | V | LVCMOS |
| $V_{IH}$ | Input High Voltage | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | –0.3 | | 0.7 | V | LVCMOS |
| $V_{OH}$ | Output High Voltage | 1.8 | | | V | $I_{OH}$=-15 mA[a] |
| $V_{OL}$ | Output Low Voltage | | | 0.6 | V | $I_{OL}$= 15 mA |
| $Z_{OUT}$ | Output Impedance | | 17 - 20 | | Ω | |
| $I_{IN}$ | Input Current | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CC\_PLL}$ | Maximum PLL Supply Current | | 2.0 | 5.0 | mA | $V_{CC\_PLL}$ Pin |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a. The MPC9772 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.

**Table 12: AC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = 0° to 85°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input reference frequency | ÷4 feedback | 50.0 | | 100.0 | MHz | PLL locked |
| | | ÷6 feedback | 33.3 | | 66.6 | MHz | |
| | | ÷8 feedback | 25.0 | | 50.0 | MHz | |
| | | ÷10 feedback | 20.0 | | 40.0 | MHz | |
| | | ÷12 feedback | 16.6 | | 33.3 | MHz | |
| | | ÷16 feedback | 12.5 | | 25.0 | MHz | |
| | | ÷24 feedback | 8.33 | | 16.6 | MHz | |
| | | ÷32 feedback | 6.25 | | 12.5 | MHz | |
| | Input reference frequency in PLL bypass mode[c] | | | | TBD | MHz | PLL bypass |
| $f_{VCO}$ | VCO frequency range[d] | | 200 | | 400 | MHz | |
| $f_{XTAL}$ | Crystal interface frequency range[e] | | 10 | | 25 | MHz | |
| $f_{MAX}$ | Output Frequency | ÷2 output | 100.0 | | 200.0 | MHz | PLL locked |
| | | ÷4 output | 50.0 | | 100.0 | MHz | |
| | | ÷6 output | 33.3 | | 66.6 | MHz | |
| | | ÷8 output | 25.0 | | 50.0 | MHz | |
| | | ÷10 output | 20.0 | | 40.0 | MHz | |
| | | ÷12 output | 16.6 | | 33.3 | MHz | |
| | | ÷16 output | 12.5 | | 25.0 | MHz | |
| | | ÷20 output | 10.0 | | 20.0 | MHz | |
| | | ÷24 output | 8.33 | | 16.6 | | |
| $f_{STOP\_CLK}$ | Serial interface clock frequency | | | | 20 | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | | 60 | % | |
| tr, tf | CCLKx Input Rise/Fall Time | | | | 1 | ns | 0.7 to 1.7V |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) CCLKx or PCLK to FB_IN | | | ±150 | | ps | PLL locked |
| $t_{sk(O)}$ | Output-to-output Skew[f] | | | | 300 | ps | |
| DC | Output duty cycle | | 45 | 50 | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.6 to 1.8V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 10 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 10 | ns | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ)[g] | | TBD | | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | TBD | | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1 σ) | | TBD | | ps | |
| BW | PLL closed loop bandwidth[h] | | | | TBD | kHz | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 10 | | ms | |

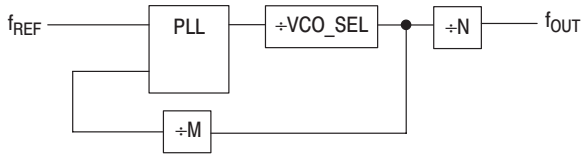
a All AC characteristics are design targets and subject to change upon device characterization.
b AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
c In bypass mode, the MPC9772 divides the input reference clock.
d The input reference frequency must match the VCO lock range divided by the total feedback divider ratio: $f_{ref} = f_{VCO} \div (M \cdot VCO\_SEL)$.
e The crystal frequency range must both meet the interface frequency range and VCO lock range divided by the feedback divider ratio: $f_{XTAL(min, max)} = f_{VCO(min, max)} \div (M \cdot VCO\_SEL)$ and $10\ MHz \le f_{XTAL} \le 25\ MHz$.
f See application section for part-to-part skew calculation.
g See application section for a jitter calculation for other confidence factors than 1 σ.
h -3 dB point of PLL transfer characteristics.

## APPLICATIONS INFORMATION

### MPC9772 Configurations

Configuring the MPC9772 amounts to properly configuring the internal dividers to produce the desired output frequencies. The output frequency can be represented by this formula:

$$f_{OUT} = f_{REF} \cdot M \div N$$




where $f_{REF}$ is the reference frequency of the selected input clock source (CCLKO, CCLK1 or XTAL interface), M is the PLL feedback divider and N is a output divider. The PLL feedback divider is configured by the FSEL_FB[2:0] and the output dividers are individually configured for each output bank by the FSEL_A[1:0], FSEL_B[1:0] and FSEL_C[1:0] inputs.

The reference frequency $f_{REF}$ and the selection of the feedback-divider M is limited by the specified VCO frequency range. $f_{REF}$ and M must be configured to match the VCO frequency range of 200 to 480[1] MHz ($V_{CC}$=3.3V) in order to achieve stable PLL operation:

$$f_{VCO,MIN} \le (f_{REF} \cdot VCO\_SEL \cdot M) \le f_{VCO,MAX}$$

The PLL post-divider VCO_SEL is either a divide-by-one or a divide-by-two and can be used to situate the VCO into the specified frequency range. This divider is controlled by the VCO_SEL pin. VCO_SEL effectively extends the usable input frequency range while it has no effect on the output to reference frequency ratio.

The output frequency for each bank can be derived from the VCO frequency and output divider:

$$f_{QA[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_A)$$
$$f_{QB[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_B)$$
$$f_{QC[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_C)$$

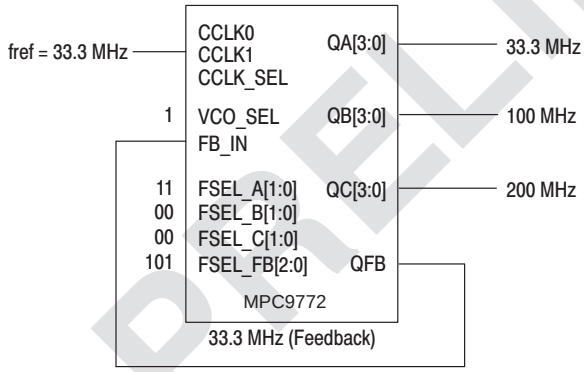
**Table 13: MPC9772 Divider**

| Divider | Function | VCO_SEL | Values |
|---|---|---|---|
| M | PLL feedback FSEL_FB[0:3] | ÷1 | 4, 6, 8, 10, 12, 16 |
| | | ÷2 | 8, 12, 16, 20, 24, 32 |
| $N_A$ | Bank A Output Divider FSEL_A[0:1] | ÷1 | 4, 6, 8, 12 |
| | | ÷2 | 8, 12, 16, 24 |
| $N_B$ | Bank B Output Divider FSEL_B[0:1] | ÷1 | 4, 6, 8, 10 |
| | | ÷2 | 8, 12, 16, 20 |
| $N_C$ | Bank C Output Divider FSEL_C[0:1] | ÷1 | 2, 4, 6, 8 |
| | | ÷2 | 4, 8, 12, 16 |

1 The VCO frequency range for 2.5V operation is specified from 200 to 400 MHz.

Table 13 shows the various PLL feedback and output dividers and Figure 3 and Figure 4 display example configurations for the MPC9772:

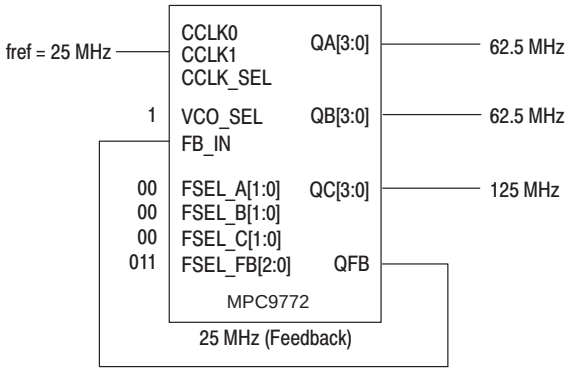
**Figure 3. Example Configuration**




MPC9772 example configuration (feedback of QFB = 33.3 MHz, $f_{VCO}$=400 MHz, VCO_SEL=÷1, M=12, $N_A$=12, $N_B$=4, $N_C$=2).

| Frequency range | Min | Max |
|---|---|---|
| Input | 16.6 MHz | 40 MHz |
| QA outputs | 16.6 MHz | 40 MHz |
| QB outputs | 50 MHz | 120 MHz |
| QC outputs | 100 MHz | 200 MHz |

**Figure 4. Example Configuration**




MPC9772 example configuration (feedback of QFB = 25 MHz, $f_{VCO}$=250 MHz, VCO_SEL=÷1, M=10, $N_A$=4, $N_B$=4, $N_C$=2).

| Frequency range | Min | Max |
|---|---|---|
| Input | 20 MHz | 48 MHz |
| QA outputs | 50 MHz | 120 MHz |
| QB outputs | 50 MHz | 120 MHz |
| QC outputs | 100 MHz | 200 MHz |

2

**MPC9772 Individual Output Disable (Clock Stop) Circuitry**

The individual clock stop (output enable) control of the MPC9772 allows designers, under software control, to implement power management into the clock distribution design. A simple serial interface and a clock stop control logic provides a mechanism through which the MPC9772 clock outputs can be individually stopped in the logic ‘0’ state: The clock stop mechanism allows serial loading of a 12–bit serial input register. This register contains one programmable clock stop bit for 12 of the 14 output clocks. The QC0 and QFB outputs cannot be stopped (disabled) with the serial port.

The user can program an output clock to stop (disable) by writing logic ‘0’ to the respective stop enable bit. Likewise, the user may programmably enable an output clock by writing logic ‘1’ to the respective enable bit. The clock stop logic enables or disables clock outputs during the time when the output would be in normally in logic low state, eliminating the possibility of short or ‘runt’ clock pulses.

The user can write to the serial input register through the STOP_DATA input by supplying a logic ‘0’ start bit followed serially by 12 NRZ disable/enable bits. The period of each STOP_DATA bit equals the period of the free–running STOP_CLK signal. The STOP_DATA serial transmission should be timed so the MPC9772 can sample each STOP_DATA bit with the rising edge of the free–running STOP_CLK signal. (see Figure 5)

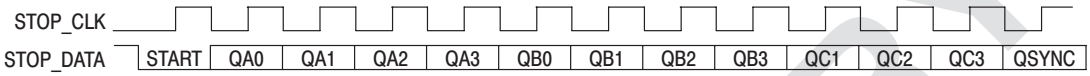



**Figure 5. Clock Stop Circuit Programming**

**SYNC Output Description**

The MPC9772 has a system synchronization pulse output QSYNC. In configurations with the output frequency relationships are not integer multiples of each other QSYNC provides a signal for system synchronization purposes. The MPC9772 monitors the relationship between the A bank and the B bank of outputs. The QSYNC output is asserted (logic low) one period in duration and one period prior to the coincident rising edges of the QA and QC outputs. The duration and the placement of the pulse is dependent QA and QC output frequencies: the QSYNC pulse width is equal to the period of the higher of the QA and QC output frequencies. Figure 6 shows various waveforms for the QSYNC output. The QSYNC output is defined for all possible combinations of the bank A and bank C outputs.



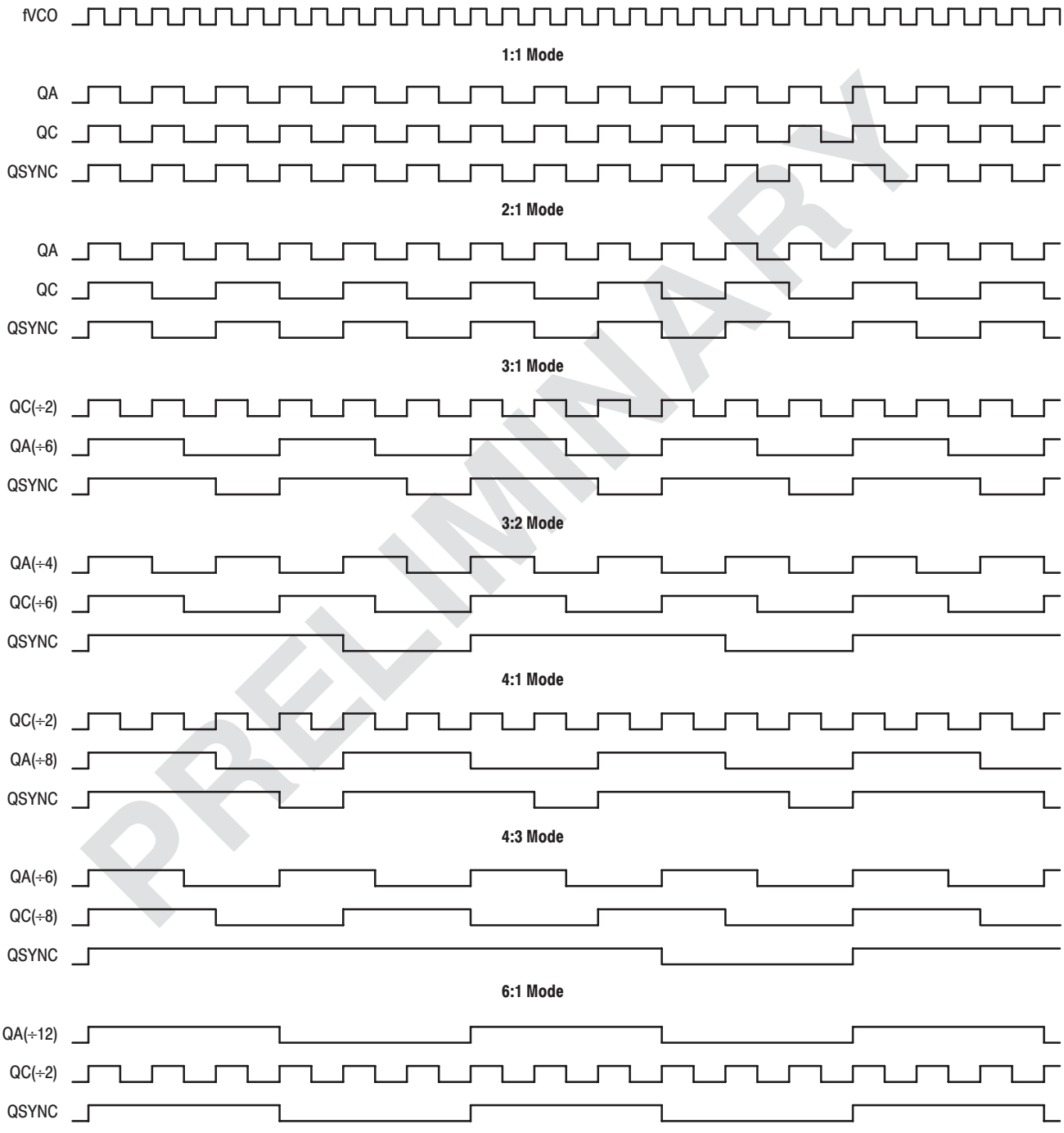



**Figure 6. QSYNC Timing Diagram**

2

**Power Supply Filtering**

The MPC9772 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the $V_{CC\_PLL}$ power supply impacts the device characteristics, for instance I/O jitter. The MPC9772 provides separate power supplies for the output buffers ($V_{CC}$) and the phase-locked loop ($V_{CC\_PLL}$) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the $V_{CCA\_PLL}$ pin for the MPC9772. Figure 7 illustrates a typical power supply filter scheme. The MPC9772 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor $R_F$. From the data sheet the $I_{CC\_PLL}$ current (the current sourced through the $V_{CC\_PLL}$ pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V ($V_{CC}$=3.3V or $V_{CC}$=2.5V) must be maintained on the $V_{CC\_PLL}$ pin. The resistor $R_F$ shown in Figure 7 "$V_{CC\_PLL}$ Power Supply Filter" must have a resistance of 9-10Ω ($V_{CC}$=2.5V) to meet the voltage drop criteria.

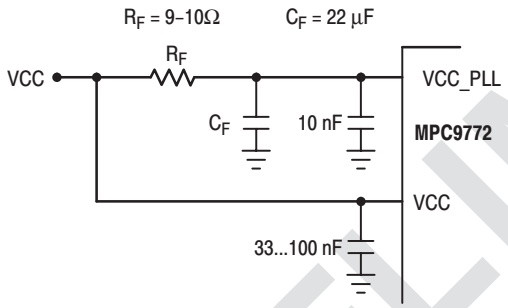



**Figure 7. $V_{CC\_PLL}$ Power Supply Filter**

The minimum values for $R_F$ and the filter capacitor $C_F$ are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 7 "$V_{CC\_PLL}$ Power Supply Filter", the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9772 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Using the MPC9772 in zero–delay applications**

Nested clock trees are typical applications for the MPC9772. Designs using the MPC9772 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC9772 clock driver allows for its use as a zero delay buffer. One example configuration is to use a ÷4 output as a feedback to the PLL and configuring all other outputs to a divide-by-4 mode. The propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

**Calculation of part-to-part skew**

The MPC9772 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9772 are connected together, the maximum overall timing uncertainty from the common CCLKx input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

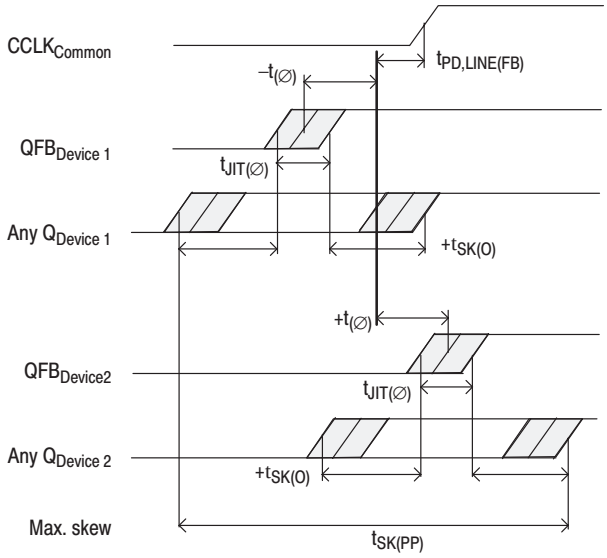



**Figure 8. MPC9772 max. device-to-device skew**

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 14.

**Table 14: Confidence Facter CF**

| CF | Probability of clock edge within the distribution |
|---|---|
| ± 1σ | 0.68268948 |
| ± 2σ | 0.95449988 |
| ± 3σ | 0.99730007 |
| ± 4σ | 0.99993663 |
| ± 5σ | 0.99999943 |
| ± 6σ | 0.99999999 |

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of -495 ps to 495 ps[1] relative to CCLK:

$t_{SK(PP)}$ = *[–300ps...300ps] + [–150ps...150ps] + [(15ps · –3)...(15ps · 3)] +* $t_{PD,\ LINE(FB)}$

$t_{SK(PP)}$ = *[–495ps...495ps] +* $t_{PD,\ LINE(FB)}$

Due to the frequency dependence of the I/O jitter, Figure 9 “Max. I/O Jitter versus frequency” can be used for a more precise timing performance analysis.

TBD
See MPC961C application section for
an example I/O jitter characteristics

**Figure 9. Max. I/O Jitter versus frequency**

**Driving Transmission Lines**

The MPC9772 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}$÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9772 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 10 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9772 clock driver is effectively doubled due to its capability to drive multiple lines.

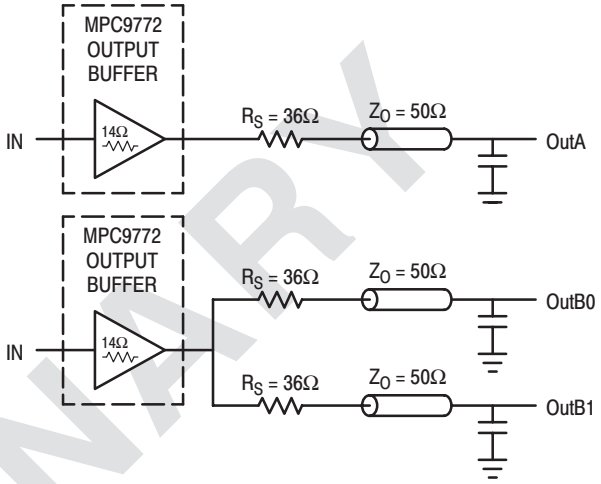



**Figure 10. Single versus Dual Transmission Lines**

The waveform plots in Figure 11 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9772 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9772. The output waveform in Figure 11 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$V_L = V_S ( Z_0 \div (R_S + R_0 + Z_0))$
$Z_0 = 50\Omega \parallel 50\Omega$
$R_S = 36\Omega \parallel 36\Omega$
$R_0 = 14\Omega$
$V_L = 3.0 ( 25 \div (18+17+25)$
$= 1.31V$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

1. Final skew data pending specification.

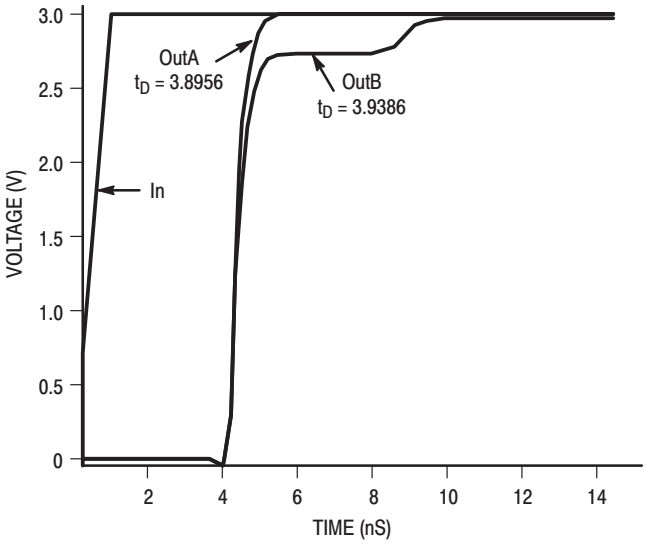



**Figure 11. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 12 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

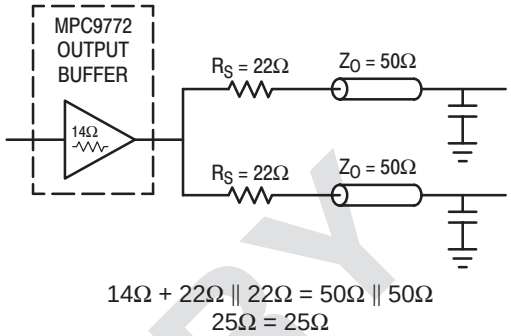



**Figure 12. Optimized Dual Line Termination**

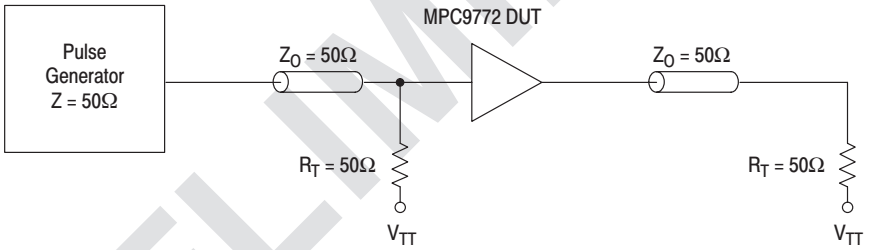
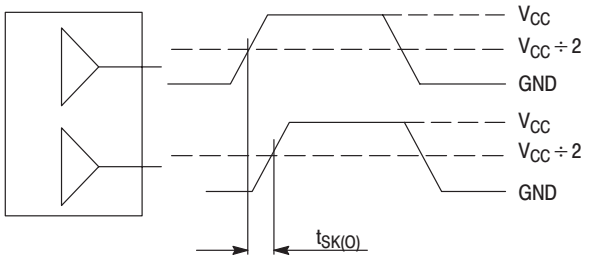



**Figure 13. CCLK MPC9772 AC test reference for $V_{cc}$ = 3.3V and $V_{cc}$ = 2.5V**




The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 14. Output–to–output Skew $t_{SK(O)}$**

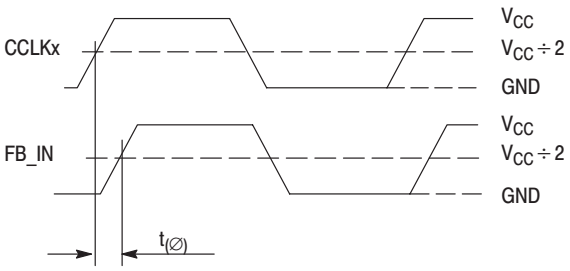
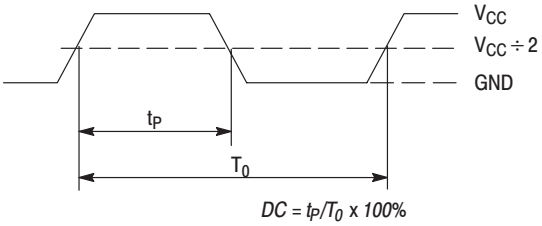
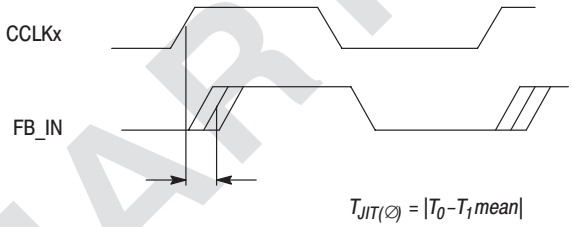



**Figure 15. Propagation delay ($t_{(\varnival)}$, static phase offset) test reference**



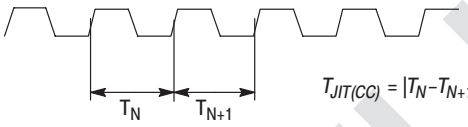

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 16. Output Duty Cycle (DC)**



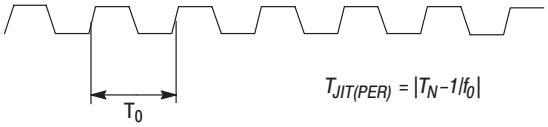

The deviation in $t_0$ for a controlled edge with respect to a $t_0$ mean in a random sample of cycles

**Figure 17. I/O Jitter**




The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

**Figure 18. Cycle–to–cycle Jitter**




The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

**Figure 19. Period Jitter**

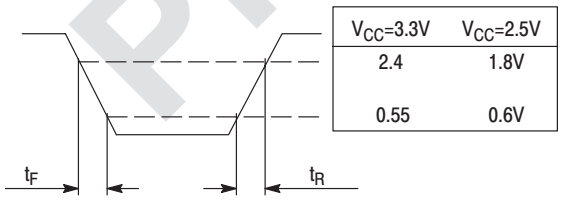



**Figure 20. Output Transition Time Test Reference**

**Order Number: MPC9773/D**
**Rev 0, 12/2001**

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*Product Preview*

# 3.3V/2.5V 1:12 LVCMOS PLL Clock Generator

**MPC9773**

**3.3V/2.5V 1:12 LVCMOS PLL CLOCK GENERATOR**

**FA SUFFIX**
52 LEAD LQFP PACKAGE
CASE 848D

The MPC9773 is a 3.3V or 2.5V compatible, 1:12 PLL based clock generator targeted for high performance low-skew clock distribution in mid-range to high-performance networking, computing and telecom applications. With output frequencies up to 240 MHz and output skews less than 300 ps[1] the device meets the needs of the most demanding clock applications.

**Features**

- 1:12 PLL based low-voltage clock generator
- 2.5V or 3.3V power supply
- Generates clock signals up to 240 MHz
- Maximum output skew of 300 ps[1]
- Differential PECL reference clock input
- Two LVCMOS PLL reference clock inputs
- External PLL feedback supports zero-delay capability
- Various feedback and output dividers (see application section)
- Supports up to three individual generated output clock frequencies
- Synchronous output clock stop circuitry for each individual output for power down support
- Drives up to 24 clock lines
- Ambient temperature range 0°C to +85°C
- Pin and function compatible to the MPC973

**Functional Description**

The MPC9773 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9773 requires the connection of the PLL feedback output QFB to feedback input FB_IN to close the PLL feedback path. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. The MPC9773 features an extensive level of frequency programmability between the 12 outputs as well as the output to input relationships, for instance 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 5:1, 5:2, 5:3, 5:4, 5:6, 6:1, 8:1 and 8:3.

The QSYNC output will indicate when the coincident rising edges of the above relationships will occur. The selectability of the feedback frequency is independent of the output frequencies. This allows for very flexible programming of the input reference versus output frequency relationship. The output frequencies can be either odd or even multiples of the input reference. In addition the output frequency can be less than the input frequency for applications where a frequency needs to be reduced by a non–binary factor. The MPC9773 also supports the 180º phase shift of one of its output banks with respect to the other output banks. The QSYNC outputs reflects the phase relationship between the QA and QC outputs and can be used for the generation of system baseline timing signals.

The REF_SEL pin selects the *1 or the LVCMOS compatible inputs as the reference clock signal. Two alternative LVCMOS compatible clock inputs are provided for clock redundancy support. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply.

The outputs can be individually disabled (stopped in logic low state) by programming the serial CLOCK_STOP interface of the MPC9773. The MPC9773 requires an external reset signal for start-up and and for PLL recovery in the case the external feedback is interrupted.

The MPC9773 is fully 2.5V and 3.3V compatible and requires no external loop filter components. All inputs (except PCLK) accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9773 outputs can drive one or two traces giving the devices an effective fanout of 1:24. The device is pin and function compatible to the MPC972 and is packaged in a 52-lead LQFP package.

1. Final specification of this parameter is pending characterization.



**Rev 0**

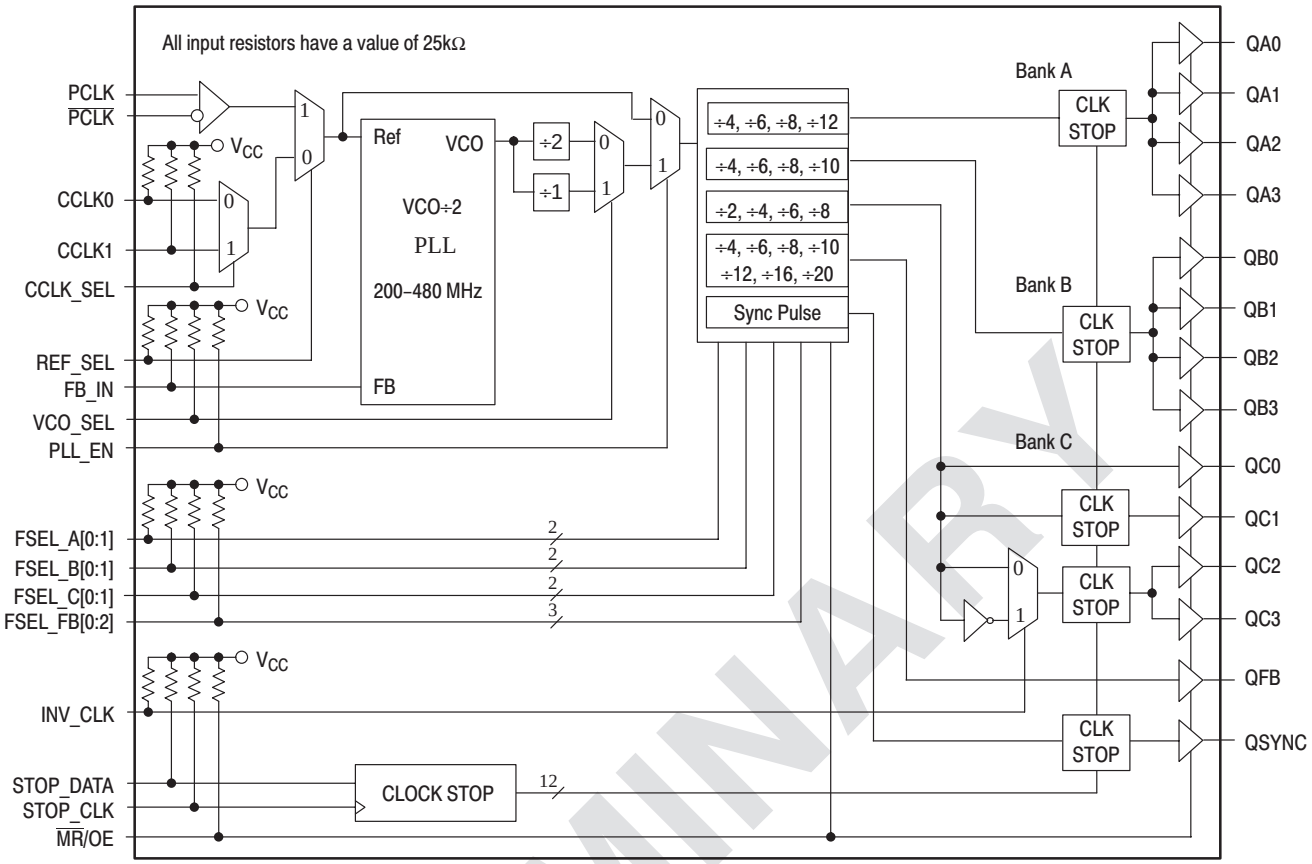


**Figure 1. MPC9773 Logic Diagram**

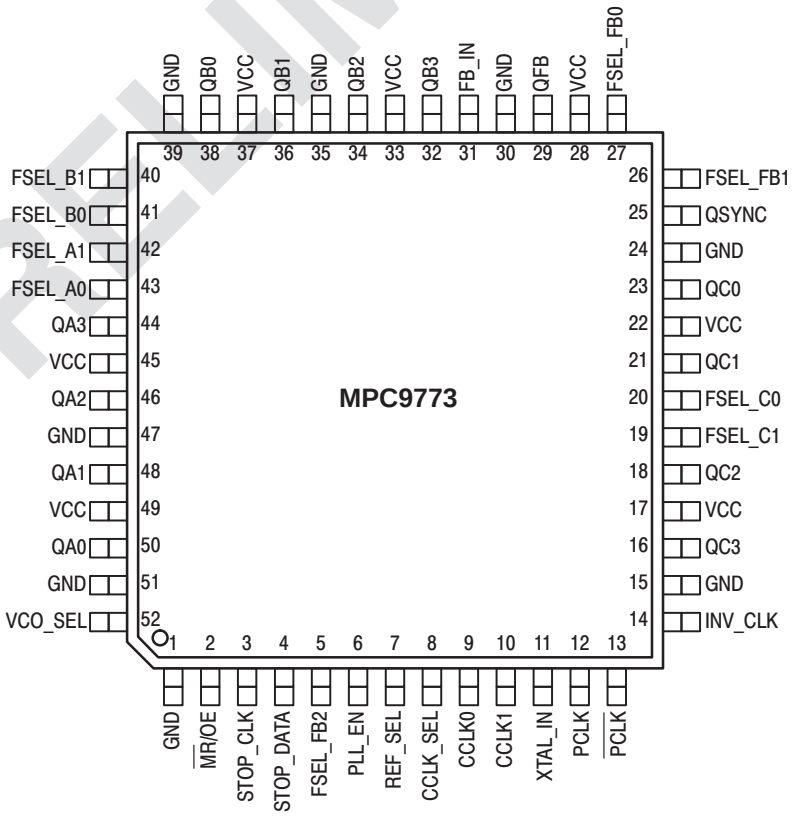


**Figure 2. MPC9773 52–Lead Package Pinout** (Top View)

**Table 1: PIN CONFIGURATION**

| Pin | I/O | Type | Function |
|---|---|---|---|
| CCLK0 | Input | LVCMOS | PLL reference clock |
| CCLK1 | Input | LVCMOS | Alternative PLL reference clock |
| PCLK, $\overline{\text{PCLK}}$ | Input | LVPECL | Differential LVPECL reference clock |
| FB_IN | Input | LVCMOS | PLL feedback signal input, connect to an QFB |
| CCLK_SEL | Input | LVCMOS | LVCMOS clock reference select |
| REF_SEL | Input | LVCMOS | LVCMOS/PECL reference clock select |
| VCO_SEL | Input | LVCMOS | VCO operating frequency select |
| PLL_EN | Input | LVCMOS | PLL enable/PLL bypass mode select |
| $\overline{\text{MR}}$/OE | Input | LVCMOS | Output enable/disable (high-impedance tristate) and device reset |
| FSEL_A[0:1] | Input | LVCMOS | Frequency divider select for bank A outputs |
| FSEL_B[0:1] | Input | LVCMOS | Frequency divider select for bank B outputs |
| FSEL_C[0:1] | Input | LVCMOS | Frequency divider select for bank C outputs |
| FSEL_FB[0:2] | Input | LVCMOS | Frequency divider select for the QFB output |
| INV_CLK | Input | LVCMOS | Clock phase selection for outputs QC2 and QC3 |
| STOP_CLK | Input | LVCMOS | Clock input for clock stop circuitry |
| STOP_DATA | Input | LVCMOS | Configuration data input for clock stop circuitry |
| QA[0-3] | Output | LVCMOS | Clock outputs (Bank A) |
| QB[0-3] | Output | LVCMOS | Clock outputs (Bank B) |
| QC[0-3] | Output | LVCMOS | Clock outputs (Bank C) |
| QFB | Output | LVCMOS | PLL feedback output. Connect to FB_IN. |
| QSYNC | Output | LVCMOS | Synchronization pulse output |
| GND | Supply | Ground | Negative power supply |
| VCC_PLL | Supply | VCC | PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin $V_{CC\_PLL}$. Please see applications section for details. |
| VCC | Supply | VCC | Positive power supply for I/O and core. All VCC pins must be connected to the positive power supply for correct operation |

**Table 2: FUNCTION TABLE (Configuration Controls)**

| Control | Default | 0 | 1 |
|---|---|---|---|
| REF_SEL | 1 | Selects CCLKx as the PLL reference clock | Selects the LVPECL inputs as the PLL reference clock |
| CCLK_SEL | 1 | Selects CCLK0 | Selects CCLK1 |
| VCO_SEL | 1 | Selects VCO÷1. (high VCO frequency range) | Selects VCO÷2. The VCO frequency is scaled by a factor of 2 (low VCO frequency range). |
| PLL_EN | 1 | Test mode with the PLL bypassed. The reference clock is substituted for the internal VCO output. MPC9773 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable. | Normal operation mode with PLL enabled. |
| INV_CLK | 1 | QC2 and QC3 are in phase with QC0 and QC1 | QC2 and QC3 are inverted (180° phase shift) with respect to QC0 and QC1 |
| $\overline{\text{MR}}$/OE | 1 | Outputs disabled (high-impedance state) and reset of the device. During reset/output disable the PLL feedback loop is open and the internal VCO is tied to its lowest frequency. The MPC9773 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLKx). | Outputs enabled (active) |
| VCO_SEL, FSEL_A[0:1], FSEL_B[0:1], FSEL_C[0:1], FSEL_FB[0:2] control the operating PLL frequency range and input/output frequency ratios. See Table 3 to Table 6 and the applications section for supported frequency ranges and output to input frequency ratios. | | | |

**Table 3: Output Divider Bank A ($N_A$)**

| VCO_SEL | FSEL_A1 | FSEL_A0 | QA[0:3] |
|---|---|---|---|
| 0 | 0 | 0 | VCO÷8 |
| 0 | 0 | 1 | VCO÷12 |
| 0 | 1 | 0 | VCO÷16 |
| 0 | 1 | 1 | VCO÷24 |
| 1 | 0 | 0 | VCO÷4 |
| 1 | 0 | 1 | VCO÷6 |
| 1 | 1 | 0 | VCO÷8 |
| 1 | 1 | 1 | VCO÷12 |

**Table 4: Output Divider Bank B ($N_B$)**

| VCO_SEL | FSEL_B1 | FSEL_B0 | QB[0:3] |
|---|---|---|---|
| 0 | 0 | 0 | VCO÷8 |
| 0 | 0 | 1 | VCO÷12 |
| 0 | 1 | 0 | VCO÷16 |
| 0 | 1 | 1 | VCO÷20 |
| 1 | 0 | 0 | VCO÷4 |
| 1 | 0 | 1 | VCO÷6 |
| 1 | 1 | 0 | VCO÷8 |
| 1 | 1 | 1 | VCO÷10 |

**Table 5: Output Divider Bank C ($N_C$)**

| VCO_SEL | FSEL_C1 | FSEL_C0 | QC[0:3] |
|---|---|---|---|
| 0 | 0 | 0 | VCO÷4 |
| 0 | 0 | 1 | VCO÷8 |
| 0 | 1 | 0 | VCO÷12 |
| 0 | 1 | 1 | VCO÷16 |
| 1 | 0 | 0 | VCO÷2 |
| 1 | 0 | 1 | VCO÷4 |
| 1 | 1 | 0 | VCO÷6 |
| 1 | 1 | 1 | VCO÷8 |

**Table 6: Output Divider PLL Feedback (M)**

| VCO_SEL | FSEL_FB2 | FSEL_FB1 | FSEL_FB0 | QFB |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | VCO÷8 |
| 0 | 0 | 0 | 1 | VCO÷12 |
| 0 | 0 | 1 | 0 | VCO÷16 |
| 0 | 0 | 1 | 1 | VCO÷20 |
| 0 | 1 | 0 | 0 | VCO÷16 |
| 0 | 1 | 0 | 1 | VCO÷24 |
| 0 | 1 | 1 | 0 | VCO÷32 |
| 0 | 1 | 1 | 1 | n/a |
| 1 | 0 | 0 | 0 | VCO÷4 |
| 1 | 0 | 0 | 1 | VCO÷6 |
| 1 | 0 | 1 | 0 | VCO÷8 |
| 1 | 0 | 1 | 1 | VCO÷10 |
| 1 | 1 | 0 | 0 | VCO÷8 |
| 1 | 1 | 0 | 1 | VCO÷12 |
| 1 | 1 | 1 | 0 | VCO÷16 |
| 1 | 1 | 1 | 1 | VCO÷20 |

**Table 7: GENERAL SPECIFICATIONS**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output Termination Voltage | | $V_{CC} \div 2$ | | V | |
| MM | ESD Protection (Machine Model) | 200 | | | V | |
| HBM | ESD Protection (Human Body Model) | 2000 | | | V | |
| LU | Latch–Up Immunity | 200 | | | mA | |
| $C_{PD}$ | Power Dissipation Capacitance | | 12 | | pF | Per output |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | Inputs |

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**Table 8: ABSOLUTE MAXIMUM RATINGS[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage Temperature | -65 | 125 | °C | |

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 9: DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = 0°C to 85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{CC\_PLL}$ | PLL Supply Voltage | 2.325 | | $V_{CC}$ | V | LVCMOS |
| $V_{IH}$ | Input High Voltage | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | | | 0.8 | V | LVCMOS |
| $V_{PP}$ | Peak–to–peak Input Voltage PCLK, $\overline{PCLK}$ | 250 | | | mV | LVPECL |
| $V_{CMR}$[a] | Common Mode Range PCLK, $\overline{PCLK}$ | 1.0 | | $V_{CC}$ – 0.6 | V | LVPECL |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$=-24 mA[b] |
| $V_{OL}$ | Output Low Voltage | | | 0.55<br>0.30 | V<br>V | $I_{OL}$= 24 mA<br>$I_{OL}$= 12 mA |
| $Z_{OUT}$ | Output Impedance | | 14 - 17 | | Ω | |
| $I_{IN}$ | Input Current[c] | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CC\_PLL}$ | Maximum PLL Supply Current | | 3.0 | 5.0 | mA | $V_{CC\_PLL}$ Pin |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (DC) specification.

b. The MPC9773 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

c. Inputs have pull–down resistors affecting the input current.

**Table 10: AC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = 0°C to 85°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input reference frequency | ÷4 feedback | 50.0 | | 120.0 | MHz | PLL locked |
| | | ÷6 feedback | 33.3 | | 80.0 | MHz | |
| | | ÷8 feedback | 25.0 | | 60.0 | MHz | |
| | | ÷10 feedback | 20.0 | | 48.0 | MHz | |
| | | ÷12 feedback | 16.6 | | 40.0 | MHz | |
| | | ÷16 feedback | 12.5 | | 30.0 | MHz | |
| | | ÷24 feedback | 8.33 | | 20.0 | MHz | |
| | | ÷32 feedback | 6.25 | | 15 | MHz | |
| | Input reference frequency in PLL bypass mode[c] | | | | TBD | MHz | PLL bypass |
| $f_{VCO}$ | VCO frequency range[d] | | 200 | | 480 | MHz | |
| $f_{MAX}$ | Output Frequency | ÷2 output | 100.0 | | 240.0 | MHz | PLL locked |
| | | ÷4 output | 50.0 | | 120.0 | MHz | |
| | | ÷6 output | 33.3 | | 80.0 | MHz | |
| | | ÷8 output | 25.0 | | 60.0 | MHz | |
| | | ÷10 output | 20.0 | | 48.0 | MHz | |
| | | ÷12 output | 16.6 | | 40.0 | MHz | |
| | | ÷16 output | 12.5 | | 30.0 | MHz | |
| | | ÷20 output | 10.0 | | 24.0 | MHz | |
| | | ÷24 output | 8.33 | | 20.0 | | |
| $f_{STOP\_CLK}$ | Serial interface clock frequency | | | | 20 | MHz | |
| $V_{PP}$ | Peak–to–peak Input Voltage | PCLK, $\overline{PCLK}$ | 500 | | 1000 | mV | LVPECL |
| $V_{CMR}$[e] | Common Mode Range | PCLK, $\overline{PCLK}$ | 1.2 | | $V_{CC}$–0.9 | V | LVPECL |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | | 60 | % | |
| tr, tf | CCLKx Input Rise/Fall Time | | | | 1.0 | ns | 0.8 to 2.0V |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) | | | | | | PLL locked |
| | | CCLKx to FB_IN | | ±150 | | ps | |
| | | PCLK to FB_IN | | ±150 | | ps | |
| $t_{sk(O)}$ | Output-to-output Skew[f] | | | | 300 | ps | |
| DC | Output duty cycle | | 45 | 50 | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.55 to 2.4V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 8 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 8 | ns | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ)[g] | | TBD | | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | TBD | | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1 σ) | | TBD | | ps | |
| BW | PLL closed loop bandwidth[h] | | | | | kHz | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 10 | | ms | |

a All AC characteristics are design targets and subject to change upon device characterization.
b AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
c In bypass mode, the MPC9773 divides the input reference clock.
d The input reference frequency must match the VCO lock range divided by the total feedback divider ratio: $f_{ref} = f_{VCO} \div (M \cdot VCO\_SEL)$
e $V_{CMR}$ (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ or $V_{PP}$ impacts static phase offset $t_{(\varnothing)}$.
f See application section for part-to-part skew calculation.
g See application section for a jitter calculation for other confidence factors than 1 σ.
h -3 dB point of PLL transfer characteristics.

**Table 11: DC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = 0°C to 85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{CC\_PLL}$ | PLL Supply Voltage | 2.325 | | $V_{CC}$ | V | LVCMOS |
| $V_{IH}$ | Input High Voltage | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | –0.3 | | 0.7 | V | LVCMOS |
| $V_{PP}$ | Peak–to–peak Input Voltage PCLK, $\overline{PCLK}$ | 250 | | | mV | LVPECL |
| $V_{CMR}$[a] | Common Mode Range PCLK, $\overline{PCLK}$ | 1.0 | | $V_{CC}$ – 0.6 | V | LVPECL |
| $V_{OH}$ | Output High Voltage | 1.8 | | | V | $I_{OH}$=-15 mA[b] |
| $V_{OL}$ | Output Low Voltage | | | 0.6 | V | $I_{OL}$= 15 mA |
| $Z_{OUT}$ | Output Impedance | | 17 - 20 | | Ω | |
| $I_{IN}$ | Input Current | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CC\_PLL}$ | Maximum PLL Supply Current | | 2.0 | 5.0 | mA | $V_{CC\_PLL}$ Pin |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (DC) specification.

b. The MPC9773 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.

**Table 12: AC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = 0°C to 85°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input reference frequency | ÷4 feedback | 50.0 | | 100.0 | MHz | PLL locked |
| | | ÷6 feedback | 33.3 | | 66.6 | MHz | |
| | | ÷8 feedback | 25.0 | | 50.0 | MHz | |
| | | ÷10 feedback | 20.0 | | 40.0 | MHz | |
| | | ÷12 feedback | 16.6 | | 33.3 | MHz | |
| | | ÷16 feedback | 12.5 | | 25.0 | MHz | |
| | | ÷24 feedback | 8.33 | | 16.6 | MHz | |
| | | ÷32 feedback | 6.25 | | 12.5 | MHz | |
| | Input reference frequency in PLL bypass mode[c] | | | | TBD | MHz | PLL bypass |
| $f_{VCO}$ | VCO frequency range[d] | | 200 | | 400 | MHz | |
| $f_{MAX}$ | Output Frequency | ÷2 output | 100.0 | | 200.0 | MHz | PLL locked |
| | | ÷4 output | 50.0 | | 100.0 | MHz | |
| | | ÷6 output | 33.3 | | 66.6 | MHz | |
| | | ÷8 output | 25.0 | | 50.0 | MHz | |
| | | ÷10 output | 20.0 | | 40.0 | MHz | |
| | | ÷12 output | 16.6 | | 33.3 | MHz | |
| | | ÷16 output | 12.5 | | 25.0 | MHz | |
| | | ÷20 output | 10.0 | | 20.0 | MHz | |
| | | ÷24 output | 8.33 | | 16.6 | | |
| $f_{STOP\_CLK}$ | Serial interface clock frequency | | | | 20 | MHz | |
| $V_{PP}$ | Peak–to–peak Input Voltage | PCLK, $\overline{PCLK}$ | 500 | | 1000 | mV | LVPECL |
| $V_{CMR}$[e] | Common Mode Range | PCLK, $\overline{PCLK}$ | 1.2 | | $V_{CC}$–0.6 | V | LVPECL |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | | 60 | % | |
| tr, tf | CCLKx Input Rise/Fall Time | | | | 1 | ns | 0.7 to 1.7V |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) | | | | | | PLL locked |
| | | CCLKx to FB_IN | | ±150 | | ps | |
| | | PCLK to FB_IN | | ±150 | | ps | |
| $t_{sk(O)}$ | Output-to-output Skew[f] | | | | 300 | ps | |
| DC | Output duty cycle | | 45 | 50 | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.6 to 1.8V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 10 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 10 | ns | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ)[g] | | TBD | | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | TBD | | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1 σ) | | TBD | | ps | |
| BW | PLL closed loop bandwidth[h] | | | | TBD | kHz | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 10 | | ms | |

a All AC characteristics are design targets and subject to change upon device characterization.
b AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
c In bypass mode, the MPC9773 divides the input reference clock.
d The input reference frequency must match the VCO lock range divided by the total feedback divider ratio: $f_{ref} = f_{VCO} \div (M \cdot VCO\_SEL)$.
e $V_{CMR}$ (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ or $V_{PP}$ impacts static phase offset $t_{(\varnothing)}$.
f See application section for part-to-part skew calculation.
g See application section for a jitter calculation for other confidence factors than 1 σ.
h -3 dB point of PLL transfer characteristics.

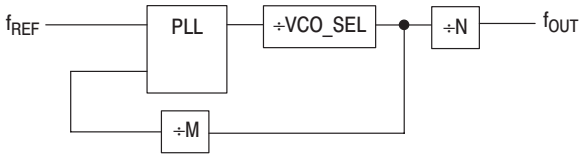
2

## APPLICATIONS INFORMATION

### MPC9773 Configurations

Configuring the MPC9773 amounts to properly configuring the internal dividers to produce the desired output frequencies. The output frequency can be represented by this formula:

$$f_{OUT} = f_{REF} \cdot M \div N$$




where $f_{REF}$ is the reference frequency of the selected input clock source (CCLKO, CCLK1 or PCLK), M is the PLL feedback divider and N is a output divider. The PLL feedback divider is configured by the FSEL_FB[2:0] and the output dividers are individually configured for each output bank by the FSEL_A[1:0], FSEL_B[1:0] and FSEL_C[1:0] inputs.

The reference frequency $f_{REF}$ and the selection of the feedback-divider M is limited by the specified VCO frequency range. $f_{REF}$ and M must be configured to match the VCO frequency range of 200 to 480[1] MHz ($V_{CC}$=3.3V) in order to achieve stable PLL operation:

$$f_{VCO,MIN} \leq (f_{REF} \cdot VCO\_SEL \cdot M) \leq f_{VCO,MAX}$$

The PLL post-divider VCO_SEL is either a divide-by-one or a divide-by-two and can be used to situate the VCO into the specified frequency range. This divider is controlled by the VCO_SEL pin. VCO_SEL effectively extends the usable input frequency range while it has no effect on the output to reference frequency ratio.

The output frequency for each bank can be derived from the VCO frequency and output divider:

$$f_{QA[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_A)$$
$$f_{QB[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_B)$$
$$f_{QC[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_C)$$

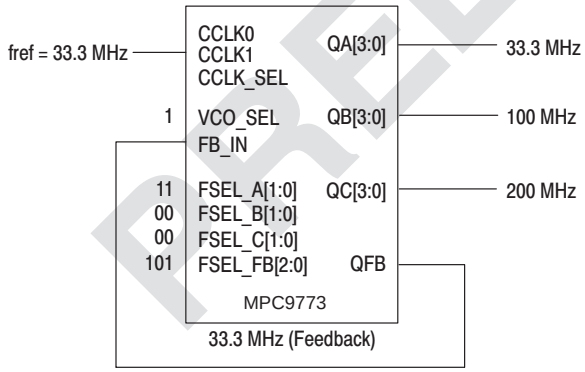
**Table 13: MPC9773 Divider**

| Divider | Function | VCO_SEL | Values |
|---|---|---|---|
| M | PLL feedback FSEL_FB[0:3] | ÷1 | 4, 6, 8, 10, 12, 16 |
| | | ÷2 | 8, 12, 16, 20, 24, 32 |
| $N_A$ | Bank A Output Divider FSEL_A[0:1] | ÷1 | 4, 6, 8, 12 |
| | | ÷2 | 8, 12, 16, 24 |
| $N_B$ | Bank B Output Divider FSEL_B[0:1] | ÷1 | 4, 6, 8, 10 |
| | | ÷2 | 8, 12, 16, 20 |
| $N_C$ | Bank C Output Divider FSEL_C[0:1] | ÷1 | 2, 4, 6, 8 |
| | | ÷2 | 4, 8, 12, 16 |

1 The VCO frequency range for 2.5V operation is specified from 200 to 400 MHz.

Table 13 shows the various PLL feedback and output dividers and Figure 3 and Figure 4 display example configurations for the MPC9773:

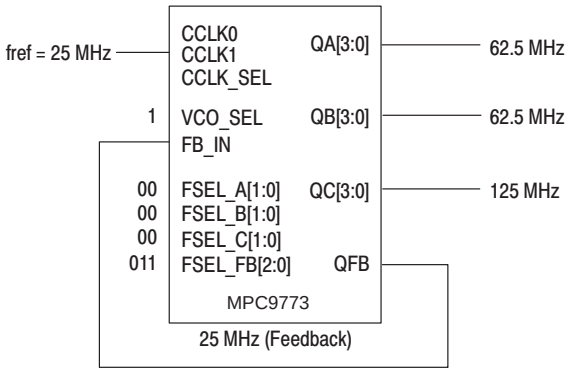
**Figure 3. Example Configuration**




MPC9773 example configuration (feedback of QFB = 33.3 MHz, $f_{VCO}$=400 MHz, VCO_SEL=÷1, M=12, $N_A$=12, $N_B$=4, $N_C$=2).

| Frequency range | Min | Max |
|---|---|---|
| Input | 16.6 MHz | 40 MHz |
| QA outputs | 16.6 MHz | 40 MHz |
| QB outputs | 50 MHz | 120 MHz |
| QC outputs | 100 MHz | 200 MHz |

**Figure 4. Example Configuration**




MPC9773 example configuration (feedback of QFB = 25 MHz, $f_{VCO}$=250 MHz, VCO_SEL=÷1, M=10, $N_A$=4, $N_B$=4, $N_C$=2).

| Frequency range | Min | Max |
|---|---|---|
| Input | 20 MHz | 48 MHz |
| QA outputs | 50 MHz | 120 MHz |
| QB outputs | 50 MHz | 120 MHz |
| QC outputs | 100 MHz | 200 MHz |

**MPC9773 Individual Output Disable (Clock Stop) Circuitry**

The individual clock stop (output enable) control of the MPC9773 allows designers, under software control, to implement power management into the clock distribution design. A simple serial interface and a clock stop control logic provides a mechanism through which the MPC9773 clock outputs can be individually stopped in the logic ‘0’ state: The clock stop mechanism allows serial loading of a 12–bit serial input register. This register contains one programmable clock stop bit for 12 of the 14 output clocks. The QC0 and QFB outputs cannot be stopped (disabled) with the serial port.

The user can program an output clock to stop (disable) by writing logic ‘0’ to the respective stop enable bit. Likewise, the user may programmably enable an output clock by writing logic ‘1’ to the respective enable bit. The clock stop logic enables or disables clock outputs during the time when the output would be in normally in logic low state, eliminating the possibility of short or ‘runt’ clock pulses.

The user can write to the serial input register through the STOP_DATA input by supplying a logic ‘0’ start bit followed serially by 12 NRZ disable/enable bits. The period of each STOP_DATA bit equals the period of the free–running STOP_CLK signal. The STOP_DATA serial transmission should be timed so the MPC9773 can sample each STOP_DATA bit with the rising edge of the free–running STOP_CLK signal. (see Figure 5)

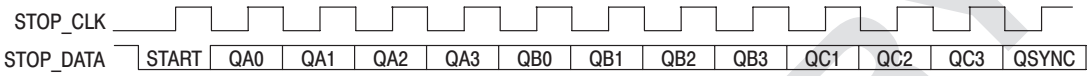



**Figure 5. Clock Stop Circuit Programming**

**SYNC Output Description**

The MPC9773 has a system synchronization pulse output QSYNC. In configurations with the output frequency relationships are not integer multiples of each other QSYNC provides a signal for system synchronization purposes. The MPC9773 monitors the relationship between the A bank and the B bank of outputs. The QSYNC output is asserted (logic low) one period in duration and one period prior to the coincident rising edges of the QA and QC outputs. The duration and the placement of the pulse is dependent QA and QC output frequencies: the QSYNC pulse width is equal to the period of the higher of the QA and QC output frequencies. Figure 6 shows various waveforms for the QSYNC output. The QSYNC output is defined for all possible combinations of the bank A and bank C outputs.

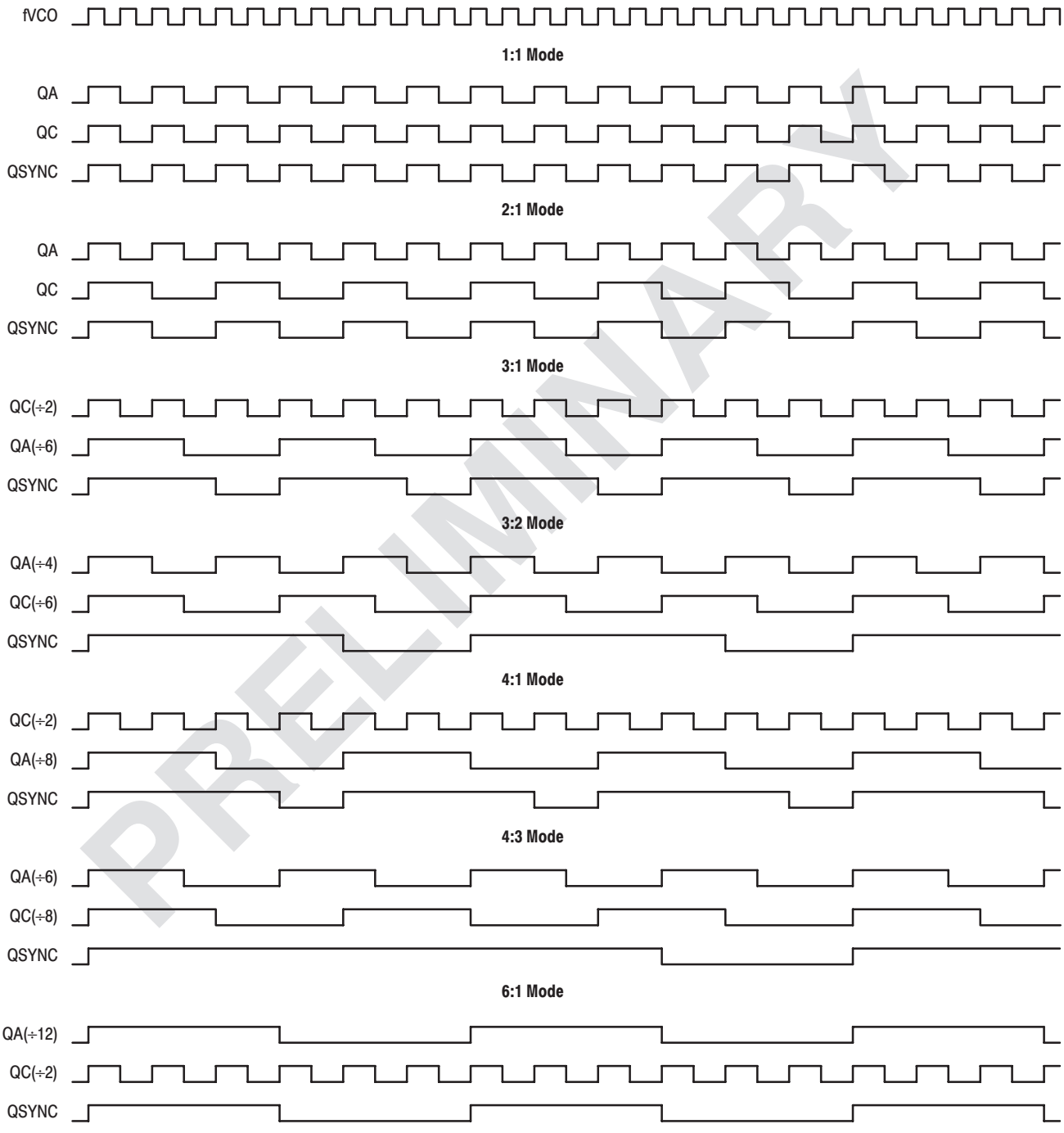





**Figure 6. QSYNC Timing Diagram**

### Power Supply Filtering

The MPC9773 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the $V_{CC\_PLL}$ power supply impacts the device characteristics, for instance I/O jitter. The MPC9773 provides separate power supplies for the output buffers ($V_{CC}$) and the phase-locked loop ($V_{CC\_PLL}$) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the $V_{CCA\_PLL}$ pin for the MPC9773. Figure 7 illustrates a typical power supply filter scheme. The MPC9773 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor $R_F$. From the data sheet the $I_{CC\_PLL}$ current (the current sourced through the $V_{CC\_PLL}$ pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V ($V_{CC}$=3.3V or $V_{CC}$=2.5V) must be maintained on the $V_{CC\_PLL}$ pin. The resistor $R_F$ shown in Figure 7 "$V_{CC\_PLL}$ Power Supply Filter" must have a resistance of 9-10Ω ($V_{CC}$=2.5V) to meet the voltage drop criteria.

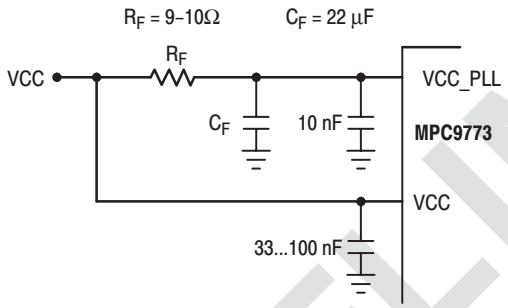



**Figure 7. $V_{CC\_PLL}$ Power Supply Filter**

The minimum values for $R_F$ and the filter capacitor $C_F$ are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 7 "$V_{CC\_PLL}$ Power Supply Filter", the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9773 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

### Using the MPC9773 in zero–delay applications

Nested clock trees are typical applications for the MPC9773. Designs using the MPC9773 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC9773 clock driver allows for its use as a zero delay buffer. One example configuration is to use a ÷4 output as a feedback to the PLL and configuring all other outputs to a divide-by-4 mode. The propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

### Calculation of part-to-part skew

The MPC9773 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9773 are connected together, the maximum overall timing uncertainty from the common CCLKx input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

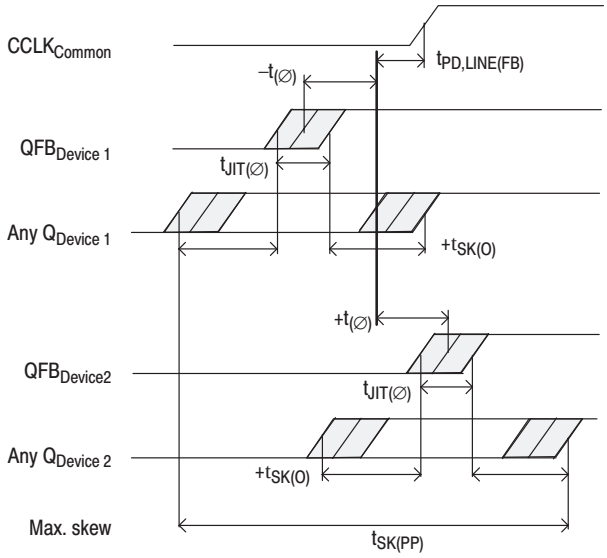



**Figure 8. MPC9773 max. device-to-device skew**

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 14.

**Table 14: Confidence Facter CF**

| CF | Probability of clock edge within the distribution |
|---|---|
| ± 1σ | 0.68268948 |
| ± 2σ | 0.95449988 |
| ± 3σ | 0.99730007 |
| ± 4σ | 0.99993663 |
| ± 5σ | 0.99999943 |
| ± 6σ | 0.99999999 |

2

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of -495 ps to 495 ps[1] relative to CCLK:

$t_{SK(PP)}$ = *[–300ps...300ps] + [–150ps...150ps] + [(15ps · –3)...(15ps · 3)] +* $t_{PD,\ LINE(FB)}$

$t_{SK(PP)}$ = *[–495ps...495ps] +* $t_{PD,\ LINE(FB)}$

Due to the frequency dependence of the I/O jitter, Figure 9 “Max. I/O Jitter versus frequency” can be used for a more precise timing performance analysis.

TBD
See MPC961C application section for
an example I/O jitter characteristics

**Figure 9. Max. I/O Jitter versus frequency**

**Driving Transmission Lines**

The MPC9773 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}$÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9773 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 10 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9773 clock driver is effectively doubled due to its capability to drive multiple lines.

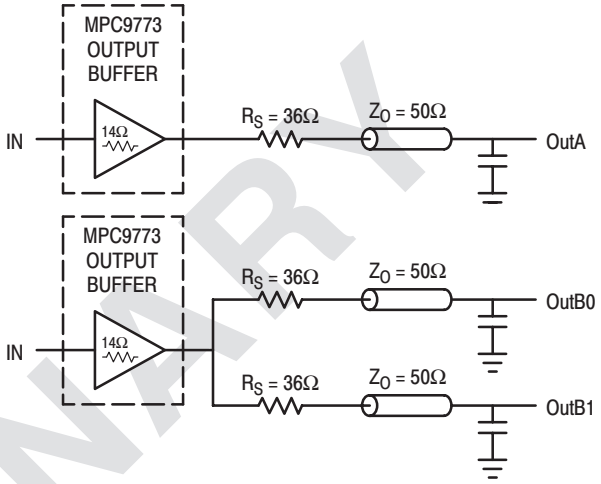



**Figure 10. Single versus Dual Transmission Lines**

The waveform plots in Figure 11 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9773 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9773. The output waveform in Figure 11 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$V_L = V_S ( Z_0 \div (R_S + R_0 + Z_0))$
$Z_0 = 50\Omega \parallel 50\Omega$
$R_S = 36\Omega \parallel 36\Omega$
$R_0 = 14\Omega$
$V_L = 3.0 ( 25 \div (18+17+25)$
$= 1.31V$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

1. Final skew data pending specification.

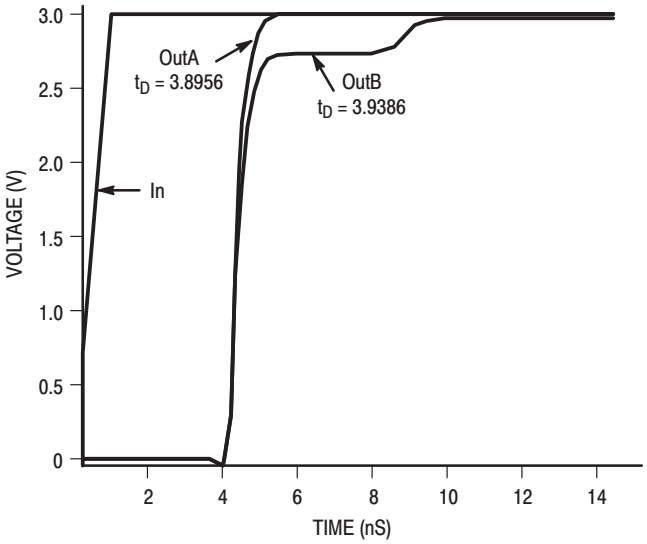
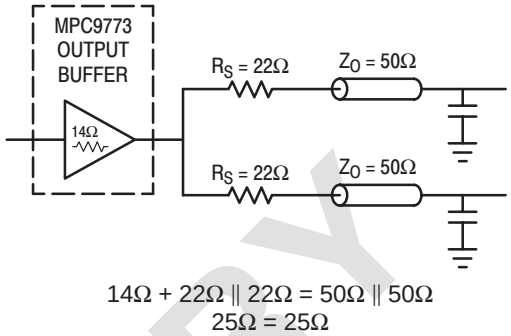



**Figure 11. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 12 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




14Ω + 22Ω || 22Ω = 50Ω || 50Ω
25Ω = 25Ω

**Figure 12. Optimized Dual Line Termination**



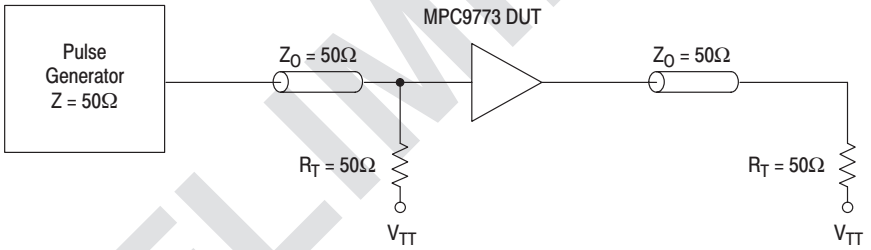



**Figure 13. CCLK MPC9773 AC test reference for $V_{cc}$ = 3.3V and $V_{cc}$ = 2.5V**

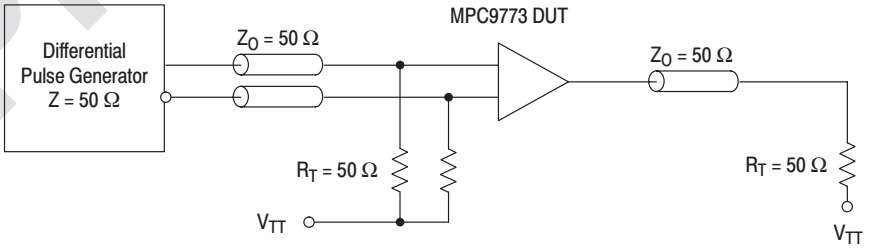
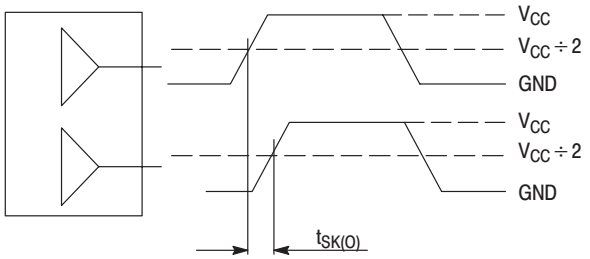



**Figure 14. PCLK MPC9773 AC test reference**




The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 15. Output–to–output Skew $t_{SK(O)}$**

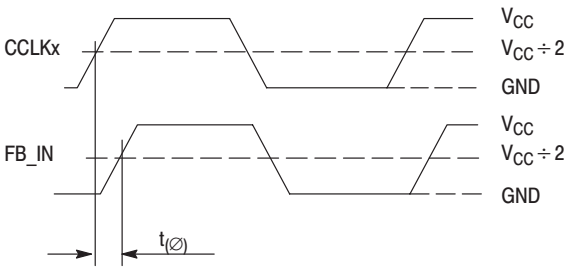
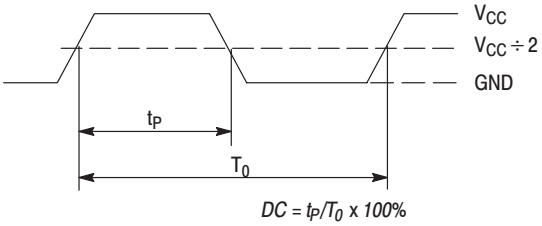
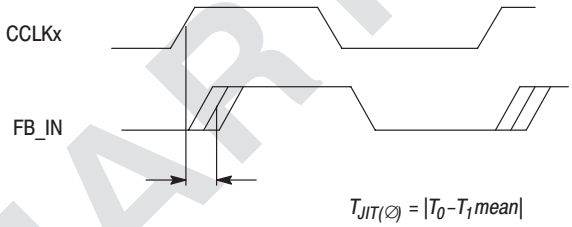



**Figure 16. Propagation delay ($t_{(\varnival)}$, static phase offset) test reference**



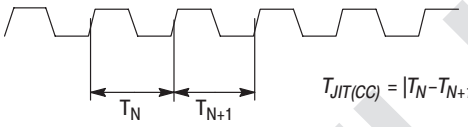

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 17. Output Duty Cycle (DC)**



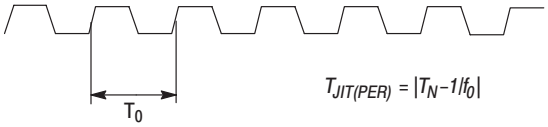

The deviation in $t_0$ for a controlled edge with respect to a $t_0$ mean in a random sample of cycles

**Figure 18. I/O Jitter**




The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

**Figure 19. Cycle–to–cycle Jitter**




The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

**Figure 20. Period Jitter**

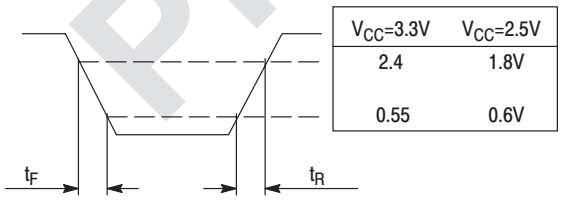



**Figure 21. Output Transition Time Test Reference**

**Order Number: MPC9774/D**
**Rev 0, 12/2001**

*Product Preview*

# 3.3V/2.5V 1:14 LVCMOS PLL Clock Generator

**MPC9774**

**3.3V/2.5V 1:14 LVCMOS PLL CLOCK GENERATOR**

2

The MPC9774 is a 3.3V or 2.5V compatible, 1:14 PLL based clock generator targeted for high performance low-skew clock distribution in mid-range to high-performance networking, computing and telecom applications. With output frequencies up to 125 MHz and output skews less than 300 ps[1] the device meets the needs of the most demanding clock applications.

**Features**

- 1:14 PLL based low-voltage clock generator
- 2.5V or 3.3V power supply
- Generates clock signals up to 125 MHz
- Maximum output skew of 300 ps[1]
- Two LVCMOS PLL reference clock inputs
- External PLL feedback supports zero-delay capability
- Various feedback and output dividers (see application section)
- Supports up to three individual generated output clock frequencies
- Drives up to 28 clock lines
- Ambient temperature range 0°C to +85°C
- Pin and function compatible to the MPC974

**FA SUFFIX**
52 LEAD LQFP PACKAGE
CASE 848D



**Functional Description**

The MPC9774 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9774 requires the connection of the PLL feedback output QFB to feedback input FB_IN to close the PLL feedback path. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range.

The MPC9774 features frequency programmability between the three output banks outputs as well as the output to input relationships. Output frequency ratios of 1:1, 2:1, 3:1, 3:2 and 3:2:1 can be realized. Additionally, the device supports a separate configurable feedback output which allows for a wide variety of of input/output frequency multiplication alternatives. The VCO_SEL pin provides an extended PLL input reference frequency range.

The REF_SEL pin selects the internal crystal oscillator or the LVCMOS compatible inputs as the reference clock signal. Two alternative LVCMOS compatible clock inputs are provided for clock redundancy support. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply.

The MPC9774 requires an external reset signal for start-up and and for PLL recovery in the case the external feedback is interrupted.

The MPC9774 is fully 2.5V and 3.3V compatible and requires no external loop filter components. All inputs (except XTAL) accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9774 outputs can drive one or two traces giving the devices an effective fanout of 1:12. The device is pin and function compatible to the MPC974 and is packaged in a 52-lead LQFP package.

1. Final specification of this parameter is pending characterization.



**Rev 0**

2

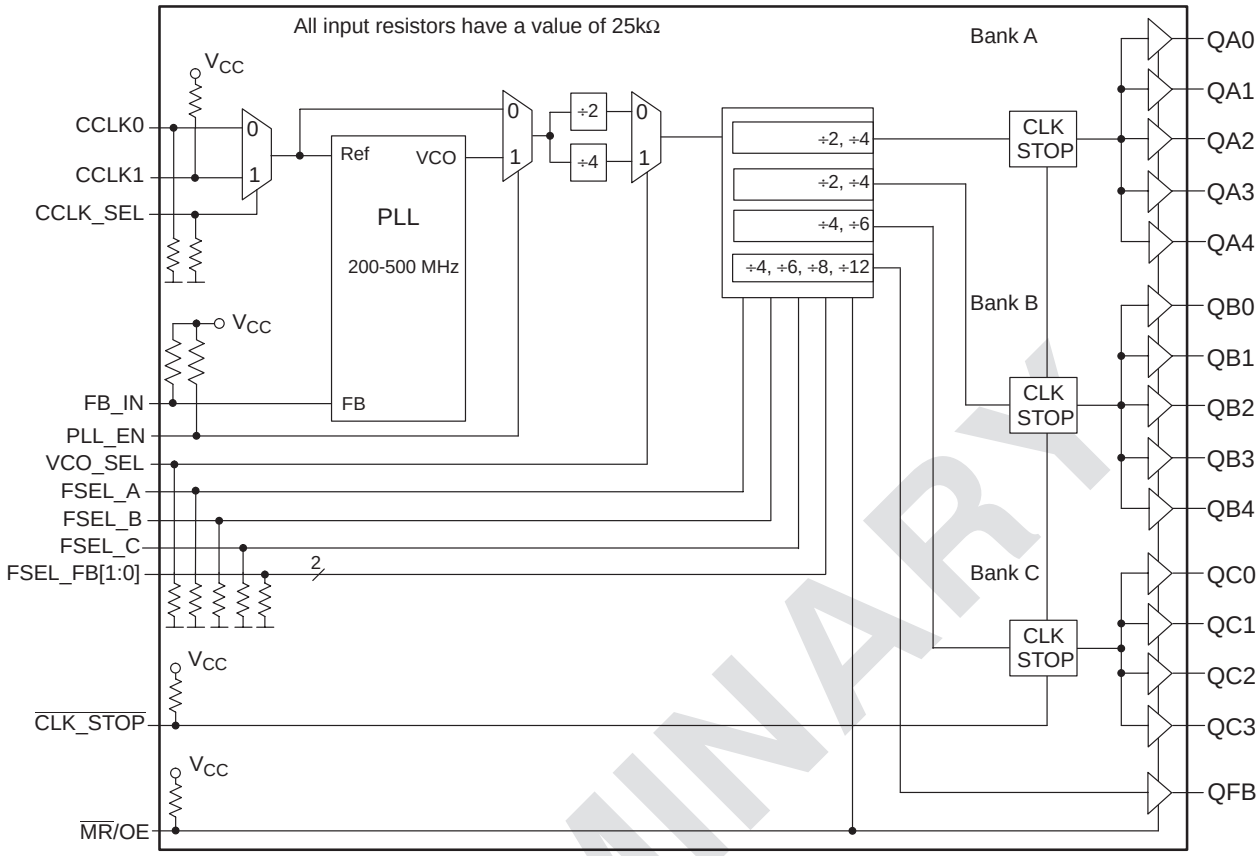



**Figure 1. MPC9774 Logic Diagram**

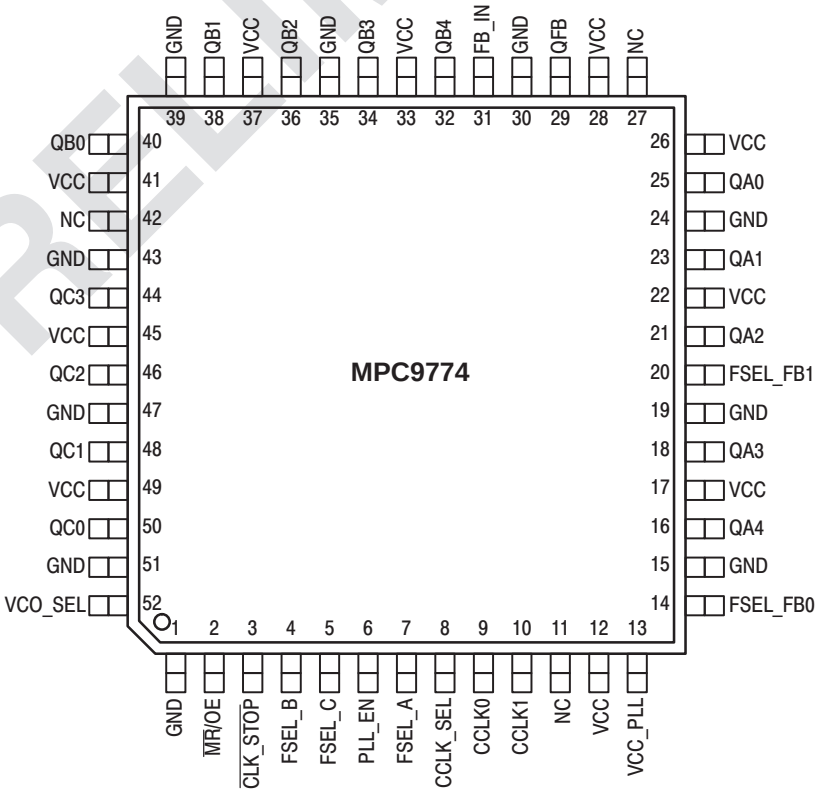



**Figure 2. MPC9774 52–Lead Package Pinout** (Top View)

**Table 1. PIN CONFIGURATION**

| Pin | I/O | Type | Function |
|---|---|---|---|
| CCLK0 | Input | LVCMOS | PLL reference clock |
| CCLK1 | Input | LVCMOS | Alternative PLL reference clock |
| FB_IN | Input | LVCMOS | PLL feedback signal input, connect to QFB |
| CCLK_SEL | Input | LVCMOS | LVCMOS clock reference select |
| VCO_SEL | Input | LVCMOS | VCO operating frequency select |
| PLL_EN | Input | LVCMOS | PLL enable/PLL bypass mode select |
| $\overline{MR}$/OE | Input | LVCMOS | Output enable/disable (high-impedance tristate) and device reset |
| $\overline{CLK\_STOP}$ | Input | LVCMOS | Output enable/clock stop (logic low state) |
| FSEL_A | Input | LVCMOS | Frequency divider select for bank A outputs |
| FSEL_B | Input | LVCMOS | Frequency divider select for bank B outputs |
| FSEL_C | Input | LVCMOS | Frequency divider select for bank C outputs |
| FSEL_FB[1:0] | Input | LVCMOS | Frequency divider select for the QFB output |
| QA[4:0] | Output | LVCMOS | Clock outputs (Bank A) |
| QB[4:0] | Output | LVCMOS | Clock outputs (Bank B) |
| QC[3:0] | Output | LVCMOS | Clock outputs (Bank C) |
| QFB | Output | LVCMOS | PLL feedback output. Connect to FB_IN. |
| GND | Supply | Ground | Negative power supply |
| VCC_PLL | Supply | $V_{CC}$ | PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin $V_{CC\_PLL.}$ Please see applications section for details. |
| $V_{CC}$ | Supply | $V_{CC}$ | Positive power supply for I/O and core. All $V_{CC}$ pins must be connected to the positive power supply for correct operation |

**Table 2. Function Table (MPC9774 configuration controls)**

| Control | Default | 0 | 1 |
|---|---|---|---|
| CCLK_SEL | 0 | Selects CCLK0 as PLL refererence signal input | Selects CCKL1 as PLL reference signal input |
| VCO_SEL | 0 | Selects VCO ÷ 2. The VCO frequency is scaled by a factor of 2 (high input frequency range) | Selects VCO ÷ 4. The VCO frequency is scaled by a factor of 4 (low input frequency range). |
| PLL_EN | 1 | Test mode with the PLL bypassed. The reference clock is substituted for the internal VCO output. MPC9774 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable. | Normal operation mode with PLL enabled. |
| $\overline{CLK\_STOP}$ | 1 | QA, QB an QC outputs disabled in logic low state. QFB is not affected by $\overline{CLK\_STOP}$. $\overline{CLK\_STOP}$ deassertion may cause the initial output clock pulse to be distorted. | Outputs enabled (active) |
| $\overline{MR}$/OE | 1 | Outputs disabled (high-impedance state) and reset of the device. During reset/output disable the PLL feedback loop is open and the internal VCO is tied to its lowest frequency. The MPC9774 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLKx). | Outputs enabled (active) |
| VCO_SEL, FSEL_A, FSEL_B, FSEL_C and FSEL_FB[1:0] control the operating PLL frequency range and input/output frequency ratios. See Table 3 and Table 4 for the device frequency configuration. | | | |

**Table 3. Function Table (Output Dividers Bank A, B, and C)**

| VCO_SEL | FSEL_A | QA[4:0] | VCO_SEL | FSEL_B | QB[4:0] | VCO_SEL | FSEL_C | QC[3:0] |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | VCO ÷ 4 | 0 | 0 | VCO ÷ 4 | 0 | 0 | VCO ÷ 8 |
| 0 | 1 | VCO ÷ 8 | 0 | 1 | VCO ÷ 8 | 0 | 1 | VCO ÷ 12 |
| 1 | 0 | VCO ÷ 8 | 1 | 0 | VCO ÷ 8 | 1 | 0 | VCO ÷ 16 |
| 1 | 1 | VCO ÷ 16 | 1 | 1 | VCO ÷ 16 | 1 | 1 | VCO ÷ 24 |



**Table 4. Function Table (QFB)**

| VCO_SEL | FSEL_B1 | FSEL_B0 | QFB |
|---|---|---|---|
| 0 | 0 | 0 | VCO ÷ 8 |
| 0 | 0 | 1 | VCO ÷ 16 |
| 0 | 1 | 0 | VCO ÷ 12 |
| 0 | 1 | 1 | VCO ÷ 24 |
| 1 | 0 | 0 | VCO ÷ 16 |
| 1 | 0 | 1 | VCO ÷ 32 |
| 1 | 1 | 0 | VCO ÷ 24 |
| 1 | 1 | 1 | VCO ÷ 48 |

**Table 5. General Specifications**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output termination voltage | | $V_{CC} \div 2$ | | V | |
| MM | ESD protection (Machine model) | 200 | | | V | |
| HBM | ESD protection (Human body model) | 2000 | | | V | |
| LU | Latch-up immunity | 200 | | | mA | |
| $C_{PD}$ | Power dissipation capacitance | | 12 | | pF | Per output |
| $C_{IN}$ | Input capacitance | | 4.0 | | pF | Inputs |

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**Table 6. Absolute Maximum Ratings[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition5 |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -65 | 125 | °C | |

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 7. DC Characteristics** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = 0°C to +85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{CC\_PLL}$ | PLL supply voltage | 2.325 | | $V_{CC}$ | V | LVCMOS |
| $V_{IH}$ | Input high voltage | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | | | 0.8 | V | LVCMOS |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$ = -24 mA[a] |
| $V_{OL}$ | Output Low Voltage | | | 0.55<br>0.30 | V<br>V | $I_{OL}$ = 24 mA<br>$I_{OL}$ = 12 mA |
| $Z_{OUT}$ | Output impedance | | 14 - 17 | | Ω | |
| $I_{IN}$ | Input Current[b] | | | ±200 | µA | $V_{IN} = V_{CC}$ or GND |
| $I_{CC\_PLL}$ | Maximum PLL Supply Current | | 3.0 | 5.0 | mA | $V_{CC\_PLL}$ Pin |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a. The MPC9774 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

b. Inputs have pull-down or pull-up resistors affecting the input current.

**Table 8. AC Characteristics** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = 0°C to + 85°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input reference frequency | ÷8 feedback | 25.0 | | 62.5 | MHz | PLL locked |
| | | ÷12 feedback | 16.6 | | 41.6 | MHz | |
| | | ÷16 feedback | 12.5 | | 31.25 | MHz | |
| | | ÷24 feedback | 8.33 | | 20.83 | MHz | |
| | | ÷32 feedback | 6.25 | | 15.625 | MHz | |
| | | ÷48 feedback | 4.16 | | 10.41 | MHz | |
| | Input reference frequency in PLL bypass mode[c] | | | | TBD | MHz | PLL bypass |
| $f_{VCO}$ | VCO frequency range[d] | | 200 | | 500 | MHz | |
| $f_{MAX}$ | Output Frequency | ÷4 output | 50.0 | | 125.0 | MHz | PLL locked |
| | | ÷8 output | 25.0 | | 62.5 | MHz | |
| | | ÷12 output | 16.6 | | 41.6 | MHz | |
| | | ÷16 output | 12.5 | | 31.25 | MHz | |
| | | ÷24 output | 8.33 | | 20.83 | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | | 60 | % | |
| tr, tf | CCLKx Input Rise/Fall Time | | | | 1.0 | ns | 0.8 to 2.0V |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) CCLKx or FB_IN | | | ±150 | | ps | PLL locked |
| $t_{sk(O)}$ | Output-to-output Skew[e] | | | | 300 | ps | |
| DC | Output duty cycle | | 45 | 50 | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.55 to 2.4V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 8 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 8 | ns | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ)[f] | | TBD | | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | TBD | | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1 σ) | | TBD | | ps | |
| BW | PLL closed loop bandwidth[g] | | | | | kHz | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 10 | | ms | |

a All AC characteristics are design targets and subject to change upon device characterization.
b AC characteristics apply for parallel output termination of 50Ω to $V_{TT.}$
c In bypass mode, the MPC9774 divides the input reference clock.
d The input reference frequency must match the VCO lock range divided by the total feedback divider ratio: $f_{ref} = f_{VCO} \div (M \cdot VCO\_SEL)$.
e See application section for part-to-part skew calculation.
f See application section for a jitter calculation for other confidence factors than 1 σ.
g -3 dB point of PLL transfer characteristics.

**Table 9. DC Characteristics** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = 0°C to + 85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{CC\_PLL}$ | PLL supply voltage | 2.325 | | $V_{CC}$ | V | LVCMOS |
| $V_{IH}$ | Input high voltage | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | -0.3 | | 0.7 | V | LVCMOS |
| $V_{OH}$ | Output High Voltage | 1.8 | | | V | $I_{OH}$ =-15 mA[a] |
| $V_{OL}$ | Output Low Voltage | | | 0.6 | V | $I_{OL}$ = 15 mA |
| $Z_{OUT}$ | Output impedance | | 17 - 20 | | Ω | |
| $I_{IN}$ | Input Current[b] | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CC\_PLL}$ | Maximum PLL Supply Current | | 2.0 | 5.0 | mA | $V_{CCA}$ Pin |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a. The MPC9774 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.
b. Inputs have pull-down or pull-up resistors affecting the input current.

**Table 10. AC Characteristics** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = 0°C to + 85°C)[a] [b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input reference frequency | ÷8 feedback | 25.0 | | 50.0 | MHz | PLL locked |
| | | ÷12 feedback | 16.6 | | 33.3 | MHz | |
| | | ÷16 feedback | 12.5 | | 25.0 | MHz | |
| | | ÷24 feedback | 8.33 | | 16.6 | MHz | |
| | | ÷32 feedback | 6.25 | | 12.5 | MHz | |
| | | ÷48 feedback | 4.16 | | 8.3 | MHz | |
| | Input reference frequency in PLL bypass mode[c] | | | | TBD | MHz | PLL bypass |
| $f_{VCO}$ | VCO frequency range[d] | | 200 | | 400 | MHz | |
| $f_{MAX}$ | Output Frequency | ÷4 output | 50.0 | | 100.0 | MHz | PLL locked |
| | | ÷8 output | 25.0 | | 50.0 | MHz | |
| | | ÷12 output | 16.6 | | 33.3 | MHz | |
| | | ÷16 output | 12.5 | | 25.0 | MHz | |
| | | ÷24 output | 8.33 | | 16.6 | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | | 60 | % | |
| tr, tf | CCLKx Input Rise/Fall Time | | | | 1 | ns | 0.7 to 1.7V |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) CCLKx or PCLK to FB_IN | | | ±150 | | ps | PLL locked |
| $t_{sk(O)}$ | Output-to-output Skew[e] | | | | 300 | ps | |
| DC | Output duty cycle | | 45 | 50 | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.6 to 1.8V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 10 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 10 | ns | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ)[f] | | TBD | | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | TBD | | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1 σ) | | TBD | | ps | |
| BW | PLL closed loop bandwidth[g] | | | | TBD | kHz | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 10 | | ms | |

a. All AC characteristics are design targets and subject to change upon device characterization.
b. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
c. In bypass mode, the MPC9774 divides the input reference clock.
d. The input reference frequency must match the VCO lock range divided by the total feedback divider ratio: $f_{ref} = f_{VCO} \div (M \cdot VCO\_SEL)$.
e. See application section for part-to-part skew calculation.
f. See application section for a jitter calculation for other confidence factors than 1 σ.
g. -3 dB point of PLL transfer characteristics.

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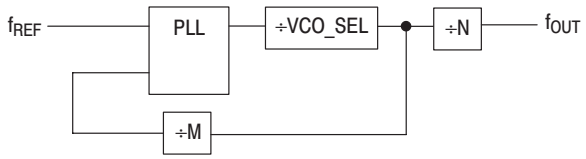
## APPLICATIONS INFORMATION

### MPC9774 Configurations

Configuring the MPC9774 amounts to properly configuring the internal dividers to produce the desired output frequencies. The output frequency can be represented by this formula:

$$f_{OUT} = f_{REF} \cdot M \div N$$




where $f_{REF}$ is the reference frequency of the selected input clock source (CCLKO or CCLK1), M is the PLL feedback divider and N is a output divider. M is configured by the FSEL_FB[0:1] and N is individually configured for each output bank by the FSEL_A, FSEL_B and FSEL_C inputs.

The reference frequency $f_{REF}$ and the selection of the feedback-divider M is limited by the specified VCO frequency range. $f_{REF}$ and M must be configured to match the VCO frequency range of 200 to 500[1] MHz ($V_{CC}$ = 3.3V) in order to achieve stable PLL operation:

$$f_{VCO,MIN} \leq (f_{REF} \cdot VCO\_SEL \cdot M) \leq f_{VCO,MAX}$$

The PLL post-divider VCO_SEL is either a divide-by-two or a divide-by-four and can be used to situate the VCO into the specified frequency range. This divider is controlled by the VCO_SEL pin. VCO_SEL effectively extends the usable input frequency range while it has no effect on the output to reference frequency ratio. The output frequency for each bank can be derived from the VCO frequency and the output divider:

$$f_{QA[4:0]} = f_{VCO} \div (VCO\_SEL \cdot N_A)$$
$$f_{QB[4:0]} = f_{VCO} \div (VCO\_SEL \cdot N_B)$$
$$f_{QC[3:0]} = f_{VCO} \div (VCO\_SEL \cdot N_C)$$

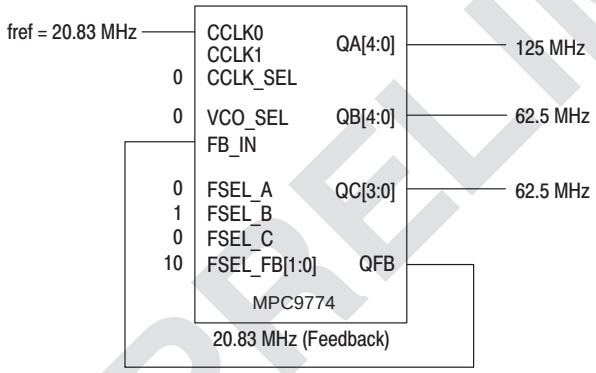
**Table 11. MPC9774 Divider**

| Divider | Function | VCO_SEL | Values |
|---|---|---|---|
| M | PLL feedback FSEL_FB[0:2] | ÷2 | 8, 12, 16, 24 |
| | | ÷4 | 16, 24, 32, 48 |
| $N_A$ | Bank A Output Divider FSEL_A | ÷2 | 4, 8 |
| | | ÷4 | 8, 16 |
| $N_B$ | Bank B Output Divider FSEL_B | ÷2 | 4, 8 |
| | | ÷4 | 8, 16 |
| $N_C$ | Bank C Output Divider FSEL_C | ÷2 | 8, 12 |
| | | ÷4 | 16, 24 |

1. The VCO frequency range for 2.5V operation is specified from 200 to 400 MHz.

Table 11 shows the various PLL feedback and output dividers. The output dividers for the three output banks allow the user to configure the outputs into 1:1, 2:1, 3:2 and 3:2:1 frequency ratios. Figure 3 and Figure 4 display example configurations for the MPC9774:

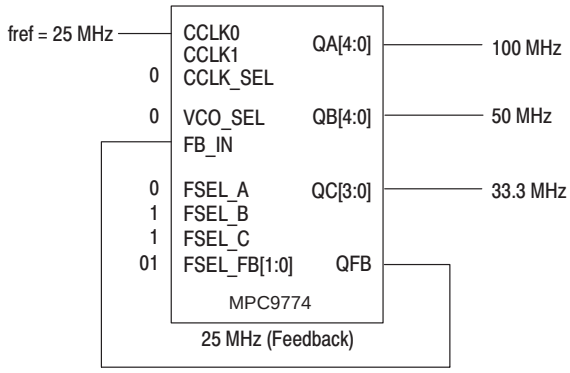
**Figure 3. Example Configuration**




MPC9774 example configuration (feedback of QFB = 20.83 MHz, VCO_SEL = ÷2, M = 12, $N_A$ = 2, $N_B$ = 4, $N_C$ = 4, $f_{VCO}$ = 500 MHz).

| Frequency range | Min | Max |
|---|---|---|
| Input | 8.33 MHz | 20.83 MHz |
| QA outputs | 50 MHz | 125 MHz |
| QB outputs | 25 MHz | 62.5 MHz |
| QC outputs | 25 MHz | 62.5 MHz |

**Figure 4. Example Configuration**




MPC9774 example configuration (feedback of QFB = 25 MHz, VCO_SEL = ÷2, M = 8, $N_A$ = 2, $N_B$ = 4, $N_C$ = 6, $f_{VCO}$ = 400 MHz).

| Frequency range | Min | Max |
|---|---|---|
| Input | 20 MHz | 48 MHz |
| QA outputs | 50 MHz | 120 MHz |
| QB outputs | 50 MHz | 120 MHz |
| QC outputs | 100 MHz | 200 MHz |

### Using the MPC9774 in zero-delay applications

Nested clock trees are typical applications for the MPC9774. Designs using the MPC9774 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback of the MPC9774 clock driver allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device (the propagation delay through the device is virtually eliminated). The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

### Calculation of part-to-part skew

The MPC9774 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9774 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

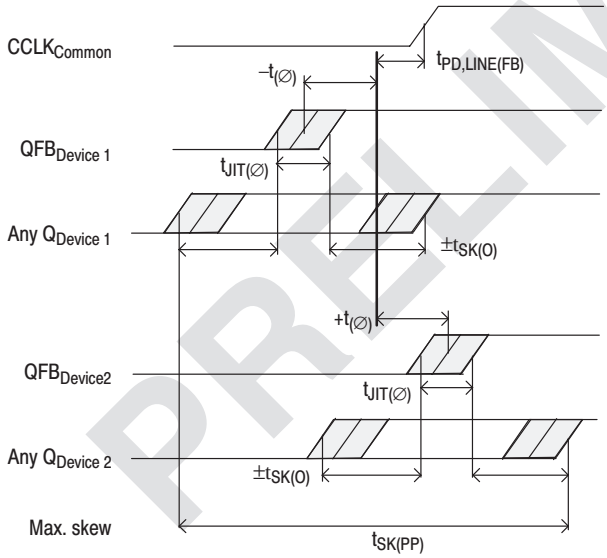



**Figure 5. MPC9774 max. device-to-device skew**

Due to the statistical nature of I/O jitter a rms value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 12.

**Table 12. MPC9774 Divider**

| CF | Probability of clock edge within the distribution |
|---|---|
| ± 1σ | 0.68268948 |
| ± 2σ | 0.95449988 |
| ± 3σ | 0.99730007 |
| ± 4σ | 0.99993663 |
| ± 5σ | 0.99999943 |
| ± 6σ | 0.99999999 |

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of -495 ps to 495 ps[2] relative to CCLK:

$$t_{SK(PP)} = [–300ps...300ps] + [–150ps...150ps] + [(15ps \cdot –3)...(15ps \cdot 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [–495ps...495ps] + t_{PD,\ LINE(FB)}$$

Due to the frequency dependence of the I/O jitter, Figure 6 can be used for a more precise timing performance analysis.

**TBD.**

See MPC961C application section for an example I/O jitter characteristic

**Figure 6.**

2. Final skew data pending specification

### Driving Transmission Lines

The MPC9774 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC} \div 2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9774 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 7 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9774

clock driver is effectively doubled due to its capability to drive multiple lines.

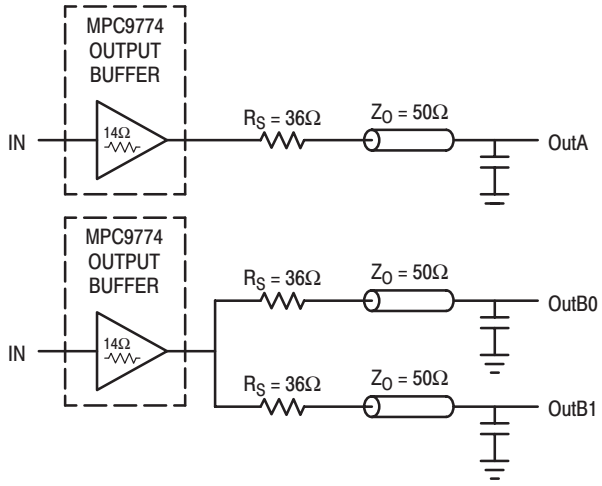



**Figure 7. Single versus Dual Transmission Lines**

The waveform plots in Figure 8 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9774 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9774. The output waveform in Figure 8 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S ( Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\Omega \parallel 50\Omega$$
$$R_S = 36\Omega \parallel 36\Omega$$
$$R_0 = 14\Omega$$
$$V_L = 3.0 ( 25 \div (18 + 17 + 25)$$
$$= 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

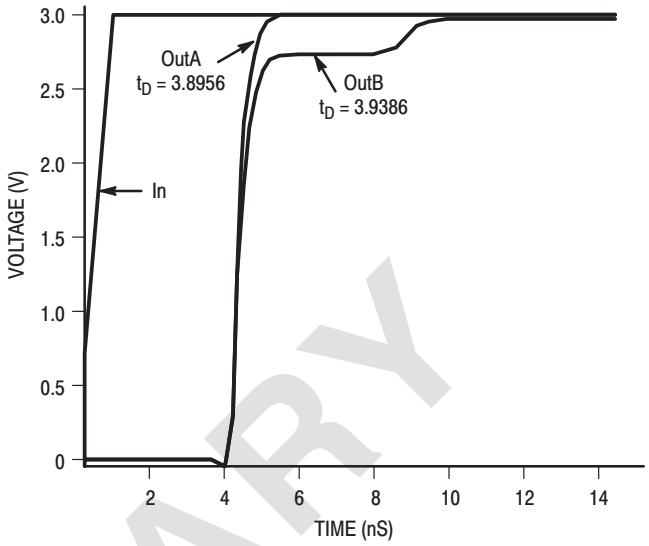
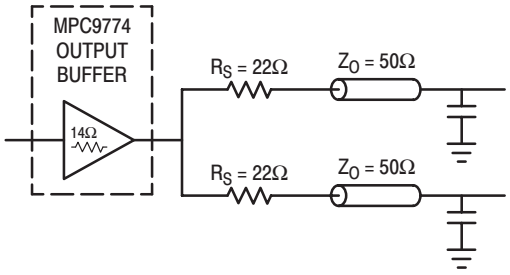



**Figure 8. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 9 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




$14\Omega + 22\Omega \parallel 22\Omega = 50\Omega \parallel 50\Omega$
$25\Omega = 25\Omega$

**Figure 9. Optimized Dual Line Termination**

**Power Supply Filtering**

The MPC9774 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the VCC_PLL power supply impacts the device characteristics, for instance I/O jitter. The MPC9774 provides separate power supplies for the output buffers ($V_{CC}$) and the phase-locked loop (VCC_PLL) of the device.The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the VCC_PLL pin for the MPC9774. Figure 10 illustrates a typical power supply filter scheme. The MPC9774 frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor $R_F$. From the data sheet the $I_{CC\_PLL}$ current (the current sourced through the VCC_PLL pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V ($V_{CC}$ = 3.3V or $V_{CC}$ = 2.5V) must be maintained on the $V_{CC\_PLL}$ pin. The resistor $R_F$ shown in MPC9774 must have a resistance of 9-10Ω ($V_{CC}$ = 2.5V) to meet the voltage drop criteria.

The minimum values for RF and the filter capacitor $C_F$ are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in MPC9774, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

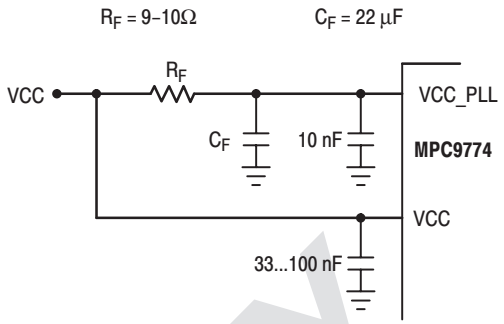



**Figure 10. $V_{CC}$ Power Supply Filter**

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9774 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

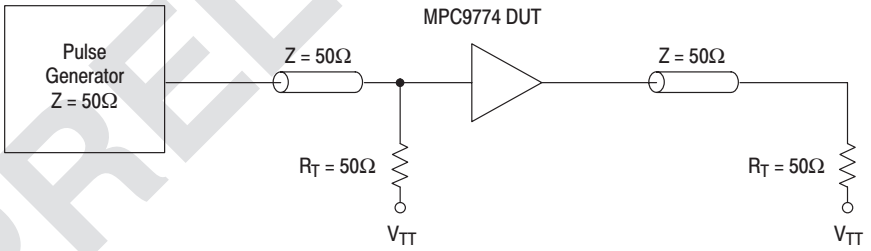
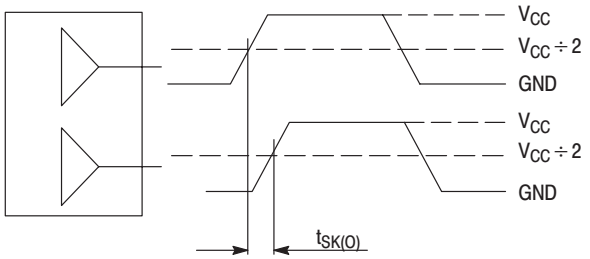



**Figure 11. CCLK MPC9774 AC test reference for $V_{cc}$ = 3.3V and $V_{cc}$ = 2.5V**




The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 12. Output–to–output Skew $t_{SK(O)}$**

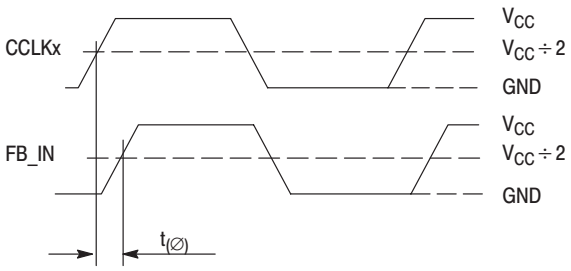
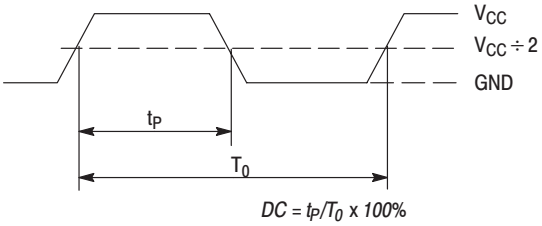
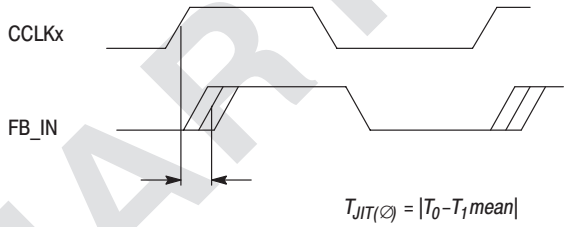



**Figure 13. Propagation delay ($t_{(\varnothing)}$, static phase offset) test reference**



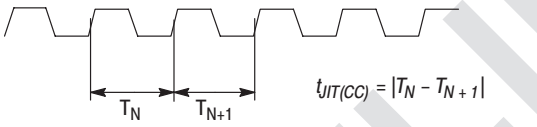

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 14. Output Duty Cycle (DC)**



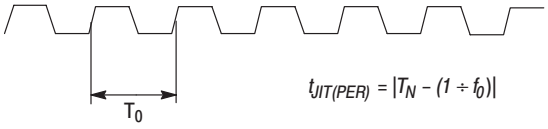

The deviation in $t_0$ for a controlled edge with respect to a $t_0$ mean in a random sample of cycles

**Figure 15. I/O Jitter**




The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

**Figure 16. Cycle–to–cycle Jitter**




The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

**Figure 17. Period Jitter**

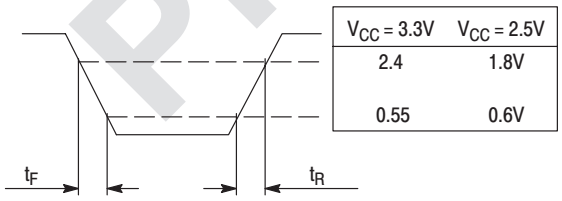



**Figure 18. Output Transition Time Test Reference**

*Product Preview*

# Low Voltage PLL Intelligent Dynamic Clock (IDCS) Switch

**MPC9893**

**LOW VOLTAGE 2.5V AND 3.3V IDCS AND PLL CLOCK GENERATOR**

**FA SUFFIX**
48–LEAD LQFP PACKAGE
CASE 932

2

The MPC9893 is a 2.5V and 3.3V compatible, PLL based intelligent dynamic clock switch and generator specifically designed for redundant clock distribution systems. The device receives two LVCMOS clock signals and generates 12 phase aligned output clocks. The MPC9893 is able to detect a failing reference clock signal and to dynamically switch to a redundant clock signal. The switch from the failing clock to the redundant clock occurs without interruption of the output clock signal (output clock slews to alignment). The phase bump typically caused by a clock failure is eliminated.

The device offers 12 low skew clock outputs organized into two output banks, each configurable to support the different clock frequencies.

The extended temperature range of the MPC9893 supports telecommunication and networking requirements. The device employs a fully differential PLL design to minimize jitter.

**Features**

- 12 output LVCMOS PLL clock generator
- 2.5V and 3.3V compatible
- IDCS - on-chip intelligent dynamic clock switch
- Automatically detects clock failure
- Smooth output phase transition during clock failover switch
- 6.25 - 200 MHz output frequency range
- LVCMOS compatible inputs and outputs
- External feedback enables zero-delay configurations
- Supports networking, telecommunications and computer applications
- Output enable/disable and static test mode (PLL bypass)
- Low skew characteristics: maximum 150 ps[1] output-to-output (within bank)
- 48 lead LQFP package
- Ambient operating temperature range of –40 to 85°C

**Functional Description**

The MPC9893 is a 3.3V or 2.5V compatible PLL clock driver and clock generator. The clock generator uses a fully integrated PLL to generate clock signals from redundant clock sources. The PLL multiplies the input reference clock signal by one, two, three, four or eight. The frequency-multiplied clock drives six bank A outputs. Six bank B outputs can run at either the same frequency than bank A or at half of the bank A frequency. Therefore, bank B outputs additionally support the frequency multiplication of the input reference clock by 3÷2 and 1÷2. Bank A and bank B outputs are phase-aligned[2]. Due to the external PLL feedback, the clock signals of both output banks are also phase-aligned[2] to the selected input reference clock, providing virtually zero-delay capability. The integrated IDCS continuously monitors both clock inputs and indicates a clock failure individually for each clock input. When a false clock signal is detected, the MPC9893 switches to the redundant clock input, forcing the PLL to slowly slew to alignment and not produce any phase bumps at the outputs. Both clock inputs are interchangeable, also supporting the switch to a failed clock that was restored. The MPC9893 also provides a manual mode that allows for user-controlled clock switches.

The PLL bypass of the MPC9893 disables the IDCS and PLL-related specifications do not apply. In PLL bypass mode, the MPC9893 is fully static in order to distribute low-frequency clocks for system test and diagnosis. Outputs of the MPC9893 can be disabled (high-impedance tristate) to isolate the device from the system. Applying output disable also resets the MPC9893. On power-up this reset function needs to be applied for correct operation of the circuitry. Please see the application section for power-on sequence recommendations.

The device is packaged in a 7x7 mm$^2$ 48-lead LQFP package.



**Rev 0**

1. Final specification subject to change
2. At coincident rising edges

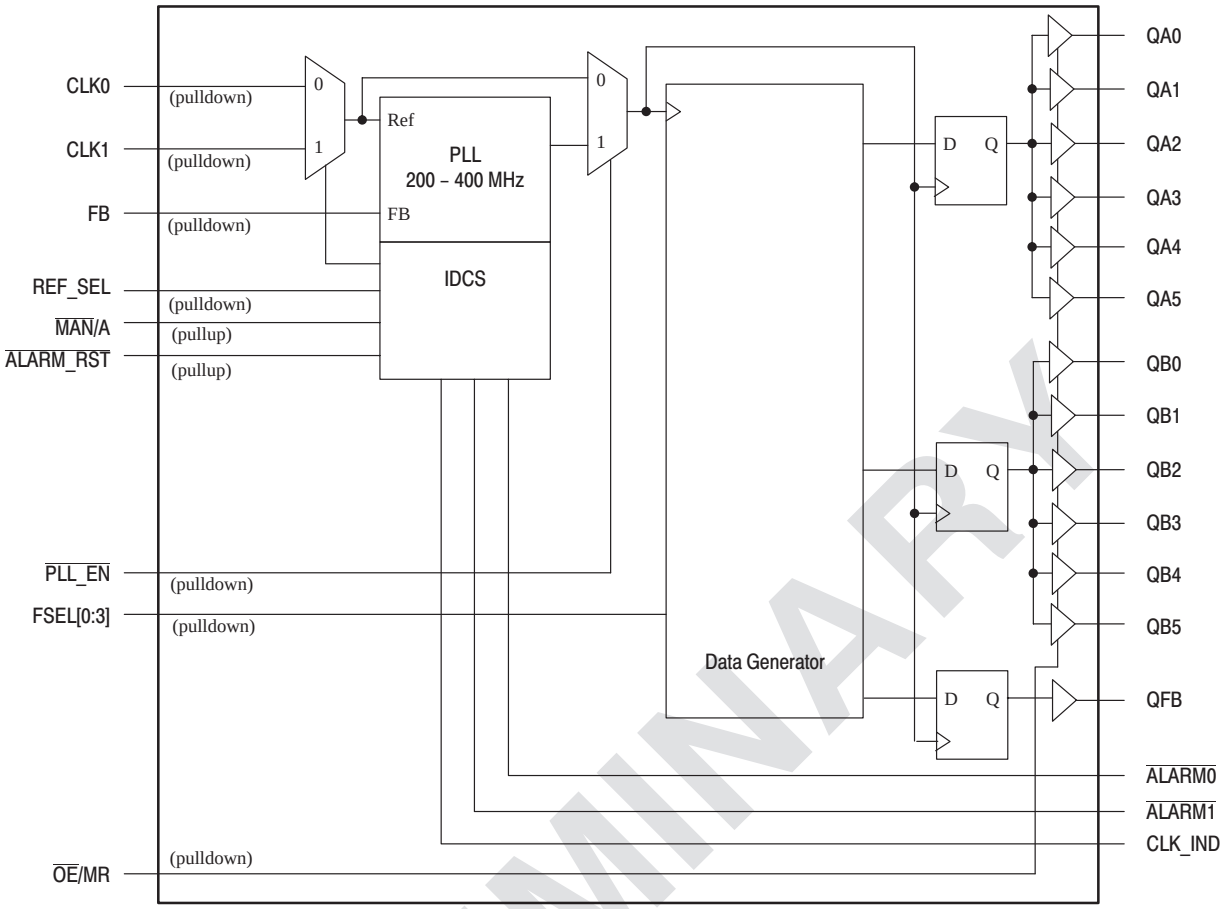
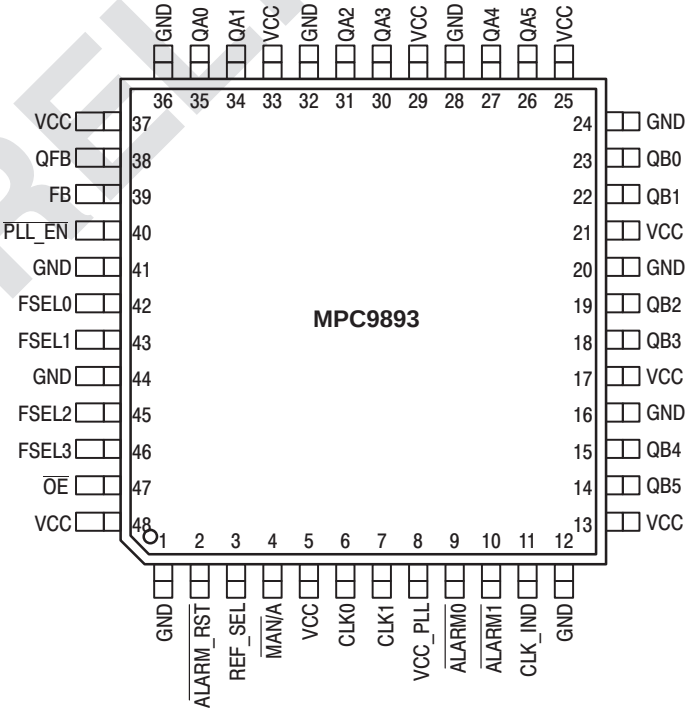



**Figure 1. MPC9893 Logic Diagram**




The MPC9893 requires an external RC filter for the analog power supply pin VCC_PLL. Please see application section for details.

**Figure 2. 48–Lead Package Pinout** (Top View)

**Table 1: PIN CONFIGURATION**

| Pin | I/O | Type | Function |
|---|---|---|---|
| CLK0, CLK1 | Input | LVCMOS | PLL reference clock inputs |
| FB | Input | LVCMOS | PLL feedback signal input, connect directly to QFB output |
| REF_SEL | Input | LVCMOS | Selects the primary reference clock |
| $\overline{\text{MAN}}$/A | Input | LVCMOS | Selects automatic switch mode or manual reference clock selection |
| $\overline{\text{ALARM\_RST}}$ | Input | LVCMOS | Reset of alarm flags and selected reference clock |
| $\overline{\text{PLL\_EN}}$ | Input | LVCMOS | Select PLL or static test mode |
| FSEL[0:3] | Input | LVCMOS | Clock frequency selection and configuration of clock divider modes |
| $\overline{\text{OE}}$/MR | Input | LVCMOS | Output enable/disable and device reset |
| QA[0:5] | Output | LVCMOS | Bank A clock outputs |
| QB[0:5] | Output | LVCMOS | Bank B clock outputs |
| QFB | Output | LVCMOS | Clock feedback output. QFB must be connected to FB for correct operation |
| $\overline{\text{ALARM0}}$ | Output | LVCMOS | Indicates clock failure on CLK0 |
| $\overline{\text{ALARM1}}$ | Output | LVCMOS | Indicates clock failure on CLK1 |
| CLK_IND | Output | LVCMOS | Indicates currently selected input reference clock |
| GND | Supply | Ground | Negative power supply |
| VCC_PLL | Supply | VCC | Positive power supply for the PLL (analog power supply). The MPC9893 requires an external RC filter for the analog power supply pin VCC_PLL. Please see the application section for details. |
| VCC | Supply | VCC | Positive power supply for I/O and core |

**Table 2: FUNCTION TABLE**

| Control | Default | 0 | 1 |
|---|---|---|---|
| Inputs | | | |
| $\overline{\text{PLL\_EN}}$ | 0 | PLL enabled. The input to output frequency relationship is that according to Table 3 if the PLL is frequency locked. | PLL bypassed and IDCS disabled. The VCO output is replaced by the reference clock signal fref. The MPC9893 is in manual mode. |
| $\overline{\text{MAN}}$/A | 1 | Manual clock switch mode. **IDCS disabled**. Clock failure detection and output flags ALARM0, ALARM1, CLK_IND are enabled. | Automatic clock switch mode. **IDCS enabled**. Clock failure detection and output flags ALARM0, ALARM1, CLK_IND are enabled. IDCS overrides REF_SEL on a clock failure. IDCS operation requires $\overline{\text{PLL\_EN}}$ = 0. |
| $\overline{\text{ALARM\_RST}}$ | 1 | $\overline{\text{ALARM0}}$, $\overline{\text{ALARM1}}$ and CLK_IND flags are reset: $\overline{\text{ALARM0}}$=H, $\overline{\text{ALARM1}}$=H and CLK_IND=REF_SEL. $\overline{\text{ALARM\_RST}}$ is an one-shot function. | $\overline{\text{ALARM0}}$, $\overline{\text{ALARM1}}$ and CLK_IND active |
| REF_SEL | 0 | Selects CLK0 as the primary clock source | Selects CLK1 as the secondary clock source |
| FSEL[0:3] | 0000 | See Following Table | |
| $\overline{\text{OE}}$/MR | 0 | Outputs enabled (active) | Outputs disabled (high impedance tristate), reset of data generators and output dividers. The MPC9893 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than two reference clock cycles (CLK0,1). MR/$\overline{\text{OE}}$ does not tristate the QFB output. |
| Outputs ($\overline{\text{ALARM0}}$, $\overline{\text{ALARM1}}$, CLK_IND are valid if PLL is locked) | | | |
| $\overline{\text{ALARM0}}$ | | CLK0 failure | |
| $\overline{\text{ALARM1}}$ | | CLK1 failure | |
| CLK_IND | | CLK0 is the reference clock | CLK1 is the reference clock |

**Table 3: CLOCK FREQUENCY CONFIGURATION**

| Name | FSEL 0 | FSEL 1 | FSEL 2 | FSEL 3 | $f_{REF}$ range [MHz] | QAx | | QBx | | QFB |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Ratio | $f_{QAX}$ [MHz] | Ratio | $f_{QBX}$[MHz] | |
| M8 | 0 | 0 | 0 | 0 | 12.5—25 | $f_{REF}$ *8 | 100—200 | $f_{REF}$ * 8 | 100—200 | $f_{REF}$ |
| M82 | 0 | 0 | 0 | 1 | | | | $f_{REF}$ * 4 | 50—100 | $f_{REF}$ |
| M4 | 0 | 0 | 1 | 0 | 25.0—50.0 | $f_{REF}$ * 4 | 100—200 | $f_{REF}$ * 4 | 100—200 | $f_{REF}$ |
| M42 | 0 | 0 | 1 | 1 | | | | $f_{REF}$ * 2 | 50—100 | $f_{REF}$ |
| M3 | 0 | 1 | 0 | 0 | 33.3—66.6 | $f_{REF}$ * 3 | 100—200 | $f_{REF}$ * 3 | 100—200 | $f_{REF}$ |
| M32 | 0 | 1 | 0 | 1 | | | | $f_{REF}$ * 3 ÷ 2 | 50—100 | $f_{REF}$ |
| M2M | 0 | 1 | 1 | 0 | 25.0—50.0 | $f_{REF}$ * 2 | 50—100 | $f_{REF}$ * 2 | 50—100 | $f_{REF}$ |
| M22M | 0 | 1 | 0 | 1 | | | | $f_{REF}$ * 1 | 25.0—50.0 | $f_{REF}$ |
| M2H | 1 | 0 | 0 | 0 | 50.0—100.0 | $f_{REF}$ * 2 | 100—200 | $f_{REF}$ * 2 | 100—200 | $f_{REF}$ |
| M22H | 1 | 0 | 0 | 1 | | | | $f_{REF}$ | 50—100 | $f_{REF}$ |
| M1L | 1 | 0 | 1 | 0 | 12.5—25 | $f_{REF}$ | 12.5—25 | $f_{REF}$ | 12.5—25 | $f_{REF}$ |
| M12L | 1 | 0 | 1 | 1 | | | | $f_{REF}$ ÷ 2 | 6.25—12.5 | $f_{REF}$ |
| M1M | 1 | 1 | 0 | 0 | 25.0—50.0 | $f_{REF}$ | 25.0—50.0 | $f_{REF}$ | 25.0—50.0 | $f_{REF}$ |
| M12M | 1 | 1 | 0 | 1 | | | | $f_{REF}$ ÷ 2 | 12.5—25 | $f_{REF}$ |
| M1H | 1 | 1 | 1 | 0 | 50.0—100.0 | $f_{REF}$ | 50.0—100.0 | $f_{REF}$ | 50.0—100.0 | $f_{REF}$ |
| M12H | 1 | 1 | 0 | 1 | | | | $f_{REF}$ ÷ 2 | 25.0—50.0 | $f_{REF}$ |

**Table 4: GENERAL SPECIFICATIONS**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output Termination Voltage | | $V_{CC}$ ÷ 2 | | V | |
| MM | ESD Protection (Machine Model) | 200 | | | V | |
| HBM | ESD Protection (Human Body Model) | 2000 | | | V | |
| LU | Latch–Up Immunity | 200 | | | mA | |
| $C_{PD}$ | Power Dissipation Capacitance | | 10 | | pF | Per output |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | Inputs |

**Table 5: ABSOLUTE MAXIMUM RATINGS[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage Temperature | -65 | 125 | °C | |

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 6: DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40° to 85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | | | 0.8 | V | LVCMOS |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$=-24 mA[a] |
| $V_{OL}$ | Output Low Voltage | | | 0.55<br>0.30 | V<br>V | $I_{OL}$= 24 mA<br>$I_{OL}$= 12 mA |
| $Z_{OUT}$ | Output Impedance | | 14 - 17 | | Ω | |
| $I_{IN}$ | Input Current | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CC\_PLL}$ | Maximum PLL Supply Current | | 2.0 | 5.0 | mA | $V_{CC\_PLL}$ Pin |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | | mA | All $V_{CC}$ Pins |
| $V_{TT}$ | Output Termination Voltage | | $V_{CC}$ ÷ 2 | | V | |

a. The MPC9893 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

**Table 7: AC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40° to 85°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency | FSEL= 000x | 12.5 | | 25.0 | MHz | PLL locked |
| | | FSEL= 001x | 25.0 | | 50.0 | MHz | |
| | | FSEL= 010x | 33.3 | | 66.6 | MHz | |
| | | FSEL= 011x | 25.0 | | 50.0 | MHz | |
| | | FSEL= 100x | 50.0 | | 100.0 | MHz | |
| | | FSEL= 101x | 12.5 | | 12.5 | MHz | |
| | | FSEL= 110x | 25.0 | | 50.0 | MHz | |
| | | FSEL= 111x | 50.0 | | 100.0 | MHz | |
| $f_{MAX}$ | Maximum Output Frequency | | | | | | PLL locked |
| | | FSEL= 000x | 50.0 | | 200.0 | MHz | |
| | | FSEL= 001x | 50.0 | | 200.0 | MHz | |
| | | FSEL= 010x | 50.0 | | 200.0 | MHz | |
| | | FSEL= 011x | 25.0 | | 100.0 | MHz | |
| | | FSEL= 100x | 50.0 | | 200.0 | MHz | |
| | | FSEL= 101x | 6.25 | | 25.0 | MHz | |
| | | FSEL= 110x | 12.5 | | 50.0 | MHz | |
| | | FSEL= 111x | 25.0 | | 100.0 | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 25 | | 75 | % | |
| tr, tf | CLK0, 1 Input Rise/Fall Time | | | | 1.0 | ns | 0.8 to 2.0V |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) | CLK to FB | | ±100 | | | PLL locked |
| Δ t | Rate of period change (phase slew rate) | | | | | ps/cycle | Failover switch |
| $t_{sk(O)}$ | Output-to-output Skew[c] | (within bank)<br>(within device) | | | 150<br>200 | ps<br>ps | |
| $DC_O$ | Output duty Cycle | | 45 | 50 | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.55 to 2.4V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 10 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 10 | ns | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ)[d] | | | TBD | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | | TBD | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1 σ) | | | TBD | ps | |
| BW | PLL closed loop bandwidth[e] | | | | TBD | kHz | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | | 10 | ms | |

a. All AC characteristics are design targets and subject to change upon device characterization
b. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$
c. See application section for part-to-part skew calculation
d. See application section for calculation for other confidence factors than 1 σ
e. -3dB point of PLL transfer characteristics

2

**Table 8: DC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40° to 85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | | | 0.7 | V | LVCMOS |
| $V_{OH}$ | Output High Voltage | 1.8 | | | V | $I_{OH}$=-15 mA[a] |
| $V_{OL}$ | Output Low Voltage | | | 0.6 | V | $I_{OL}$= 15 mA |
| $Z_{OUT}$ | Output Impedance | | 17 - 20 | | Ω | |
| $I_{IN}$ | Input Current | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CC\_PLL}$ | Maximum PLL Supply Current | | 2.0 | 5.0 | mA | $V_{CC\_PLL}$ Pin |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | | mA | All $V_{CC}$ Pins |
| $V_{TT}$ | Output Termination Voltage | | $V_{CC}$ ÷ 2 | | V | |

a. The MPC9893 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.

**Table 9: AC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40° to 85°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency | FSEL= 000x | 12.5 | | 25.0 | MHz | PLL locked |
| | | FSEL= 001x | 25.0 | | 50.0 | MHz | |
| | | FSEL= 010x | 33.3 | | 66.6 | MHz | |
| | | FSEL= 011x | 25.0 | | 50.0 | MHz | |
| | | FSEL= 100x | 50.0 | | 100.0 | MHz | |
| | | FSEL= 101x | 12.5 | | 12.5 | MHz | |
| | | FSEL= 110x | 25.0 | | 50.0 | MHz | |
| | | FSEL= 111x | 50.0 | | 100.0 | MHz | |
| $f_{MAX}$ | Maximum Output Frequency | | | | | | PLL locked |
| | | FSEL= 000x | 50.0 | | 200.0 | MHz | |
| | | FSEL= 001x | 50.0 | | 200.0 | MHz | |
| | | FSEL= 010x | 50.0 | | 200.0 | MHz | |
| | | FSEL= 011x | 25.0 | | 100.0 | MHz | |
| | | FSEL= 100x | 50.0 | | 200.0 | MHz | |
| | | FSEL= 101x | 6.25 | | 25.0 | MHz | |
| | | FSEL= 110x | 12.5 | | 50.0 | MHz | |
| | | FSEL= 111x | 25.0 | | 100.0 | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 25 | | 75 | % | |
| tr, tf | CLK0, 1 Input Rise/Fall Time | | | | 1.0 | ns | 0.7 to 1.7V |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) | CLK to FB | | ±100 | | | PLL locked |
| Δ t | Rate of period change (phase slew rate) | | | | | ps/cycle | Failover switch |
| $t_{sk(O)}$ | Output-to-output Skew[c] | (within bank) | | | 150 | ps | |
| | | (within device) | | | 200 | ps | |
| $DC_O$ | Output duty Cycle | | 45 | 50 | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.6 to 1.8V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 10 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 10 | ns | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ)[d] | | | TBD | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | | TBD | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1 σ) | | | TBD | ps | |
| BW | PLL closed loop bandwidth[e] | | | | TBD | kHz | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | | 10 | ms | |

a. All AC characteristics are design targets and subject to change upon device characterization
b. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$
c. See application section for part-to-part skew calculation
d. See application section for calculation for other confidence factors than 1 σ
e. -3dB point of PLL transfer characteristics

## APPLICATIONS INFORMATION

### Definitions

IDCS: Intelligent Dynamic Clock Switch. The IDCS monitors both primary and secondary clock signals. Upon a failure of the primary clock signal, the IDCS switches to a valid secondary clock signal and status flags are set.

Reference clock signal fref: The clock signal that is selected by the IDCS or REF_SEL as the input reference to the PLL.

Manual mode: The reference clock frequency is selected by REF_SEL.

Automatic mode: The reference clock frequency is determined by the internal IDCS logic.

Primary clock: The input clock signal selected by REF_SEL. The primary clock may or may not be the reference clock, depending on switch mode and IDCS status.

Secondary clock: The input clock signal not selected by REF_SEL

Selected clock: The CLK_IND flag indicates the reference clock signal: CLK_IND = 0 indicates CLK0 is the clock reference signal, CLK_IND =1 indicates CLK1 is the reference clock signal.

Clock failure: A valid clock signal that is stuck (high or low) for at least one input clock period. The primary clock and the secondary clock is monitored for failure. Valid clock signals must be within the AC and DC specification for the input reference clock. A loss of clock is detected if as well as the loss of both clocks. In the case of both clocks lost, the MPC9893 will set the alarm flags and the PLL will stall. The MPC9893 does not monitor and detect changes in the input frequency.

### Automatic mode and IDCS commanded clock switch

$\overline{MAN}$/A = 1, IDCS enabled: Both primary and secondary clocks are monitored. The first clock failure is reported by its $\overline{ALARMx}$ status flag (clock failure is indicated by a logic low). The $\overline{ALARMx}$ status is flag latched and remains latched until reset by assertion of $\overline{ALARM\_RST}$.

If the clock failure occurs on the primary clock, the IDCS attempts to switch to the secondary clock. The secondary clock signal needs to be valid for a successful switch. Upon a successful switch, CLK_IND indicates the reference clock, which may now be different as that originally selected by REF_SEL.

### Manual mode

$\overline{MAN}$/A = 0, IDCS disabled: PLL functions normally and both clocks are monitored. The reference clock signal will always be the clock signal selected by REF_SEL and will be indicated by CLK_IND.

### Clock output transition

A clock switch, either in automatic or manual mode, follows the next negative edge of the newly selected reference clock signal. The feedback and newly selected reference clock edge will start to slew to alignment at the next positive edge of both signals. Output runt pulses are eliminated.

### Reset

$\overline{ALARM\_RST}$ is asserted by a negative edge. It generates a one-shot reset pulse that clears both $\overline{ALARMx}$ latches and the CLK_IND latch. If both CLK0 and CLK1 are invalid or fail when $\overline{ALARM\_RST}$ is asserted, both $\overline{ALARMx}$ flags will be latched after one FB signal period and CLK_IND will be latched (L) indicating CLK0 is the reference signal. While neither $\overline{ALARMx}$ flag is latched ($\overline{ALARMx}$ = H), the CLK_IND can be freely changed with REF_SEL.

$\overline{OE}$/MR: Reset the data generator and output disable. Does not reset the IDCS flags.

### Acquiring frequency lock at startup

1. On startup, $\overline{OE}$/MR must be asserted to reset the output dividers. The IDCS should be disabled ($\overline{MAN}$/A=0) during startup to select the manual mode and the primary clock. It is recommended to assert $\overline{OE}$/MR until the PLL achieves frequency lock.
2. The PLL will attempt to gain lock if the primary clock is present on startup. PLL lock requires the specified lock time.
3. Applying a high to low transition to $\overline{ALARM\_RST}$ will clear the alarm flags.
4. Enable the IDCS ($\overline{MAN}$/A=1) to enable to IDCS.

### Power Supply Filtering

The MPC9893 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the VCC_PLL (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC9893 provides separate power supplies for the output buffers ($V_{CC}$) and the phase-locked loop (VCC_PLL) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the VCC_PLL pin for the MPC9893. Figure 3 illustrates a typical power supply filter scheme. The MPC9893 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor $R_F$. From the data sheet the $I_{CC\_PLL}$ current (the current sourced through the VCC_PLL pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V ($V_{CC}$=3.3V or $V_{CC}$=2.5V) must be maintained on the VCC_PLL pin. The resistor $R_F$ shown in Figure 3 “VCC_PLL Power Supply Filter” must have a resistance of 270Ω ($V_{CC}$=3.3V) or 9-10Ω ($V_{CC}$=2.5V) to meet the voltage drop criteria.

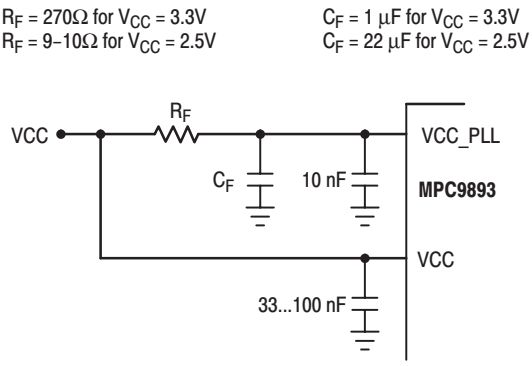



**Figure 3. VCC_PLL Power Supply Filter**

The minimum values for $R_F$ and the filter capacitor $C_F$ are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3 “VCC_PLL Power Supply Filter”, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9893 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

### Using the MPC9893 in zero–delay applications

Nested clock trees are typical applications for the MPC9893. Designs using the MPC9893 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC9893 clock driver allows for its use as a zero delay buffer. One example configuration is to use a ÷4 output as a feedback to the PLL and configuring all other outputs to a divide-by-4 mode. The propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

### Calculation of part-to-part skew

The MPC9893 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9893 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

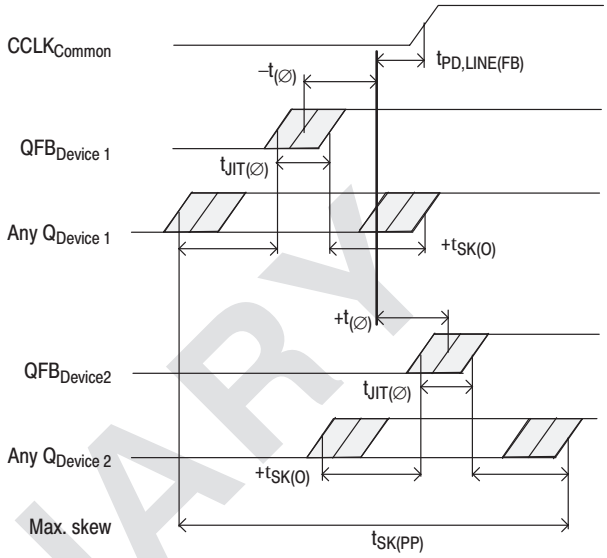



**Figure 4. MPC9893 max. device-to-device skew**

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 10.

**Table 10: Confidence Facter CF**

| CF | Probability of clock edge within the distribution |
|---|---|
| ± 1σ | 0.68268948 |
| ± 2σ | 0.95449988 |
| ± 3σ | 0.99730007 |
| ± 4σ | 0.99993663 |
| ± 5σ | 0.99999943 |
| ± 6σ | 0.99999999 |

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of -TBD ps to TBD ps[1] relative to CCLK:

$$t_{SK(PP)} = [-TBDps...TBDps] + [-200ps...200ps] + [(15ps \cdot -3)...(15ps \cdot 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [-TBDps...TBDps] + t_{PD,\ LINE(FB)}$$

Due to the frequency dependence of the I/O jitter, Figure 5 “Max. I/O Jitter versus frequency” can be used for a more precise timing performance analysis.

TBD
See MPC961C application section for
an example I/O jitter characteristics

**Figure 5. Max. I/O Jitter versus frequency**

1. Final skew data pending specification.

**Driving Transmission Lines**

The MPC9893 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}$÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9893 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 6 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9893 clock driver is effectively doubled due to its capability to drive multiple lines.

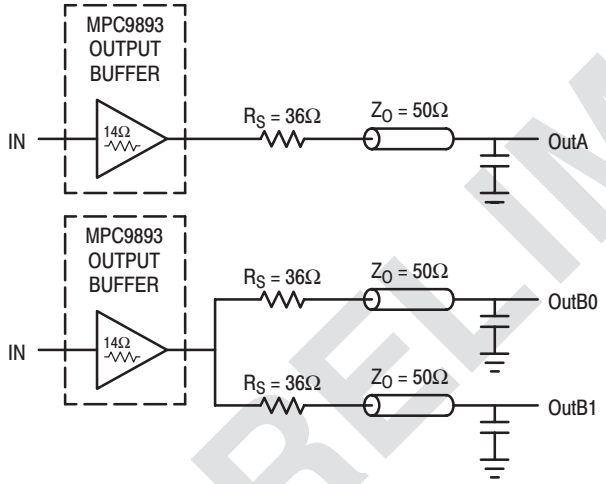



**Figure 6. Single versus Dual Transmission Lines**

The waveform plots in Figure 7 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9893 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9893. The output waveform in Figure 7 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S ( Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\Omega \parallel 50\Omega$$
$$R_S = 36\Omega \parallel 36\Omega$$
$$R_0 = 14\Omega$$
$$V_L = 3.0 ( 25 \div (18+17+25)$$
$$= 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

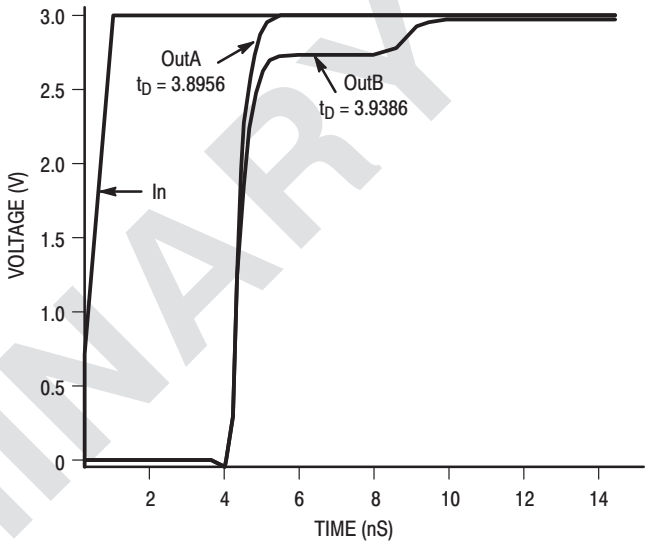
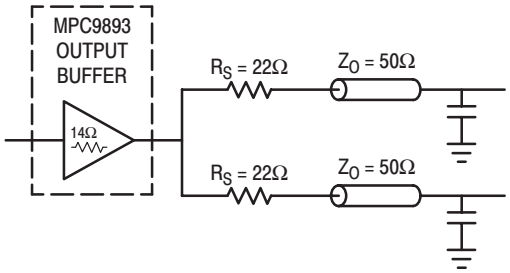



**Figure 7. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 8 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




$14\Omega + 22\Omega \parallel 22\Omega = 50\Omega \parallel 50\Omega$
$25\Omega = 25\Omega$

**Figure 8. Optimized Dual Line Termination**

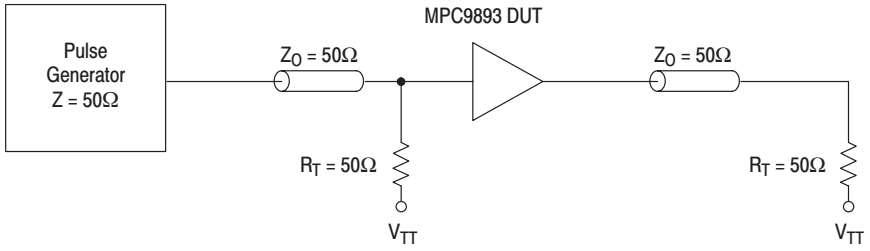
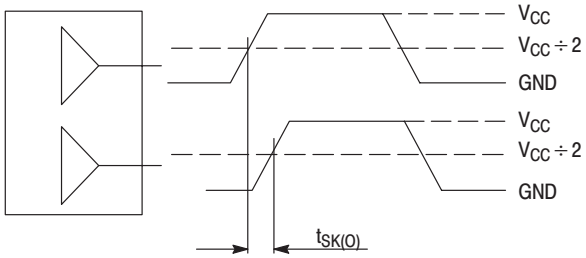



**Figure 9. CLK0, CLK1 MPC9893 AC test reference for $V_{cc}$ = 3.3V and $V_{cc}$ = 2.5V**




The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 10. Output–to–output Skew $t_{SK(O)}$**

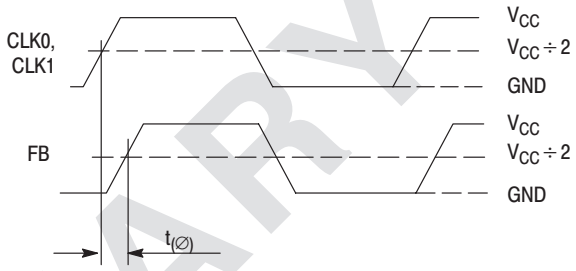
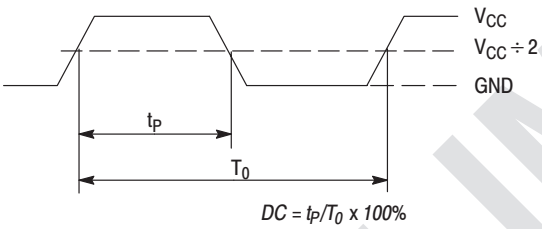
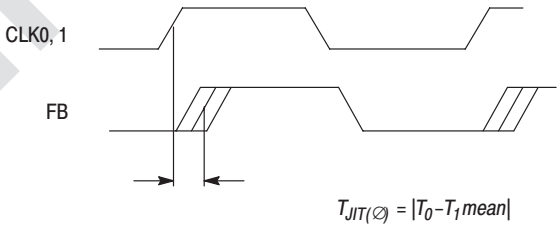



**Figure 11. Propagation delay ($t_{(\varnothing)}$, static phase offset) test reference**



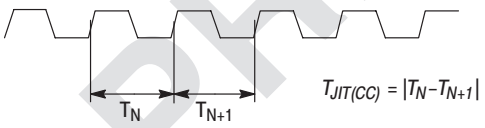

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 12. Output Duty Cycle (DC)**



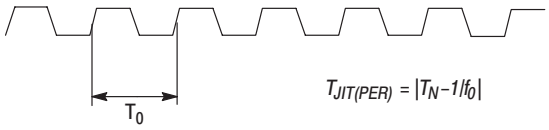

The deviation in $t_0$ for a controlled edge with respect to a $t_0$ mean in a random sample of cycles

**Figure 13. I/O Jitter**




The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

**Figure 14. Cycle–to–cycle Jitter**




The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

**Figure 15. Period Jitter**

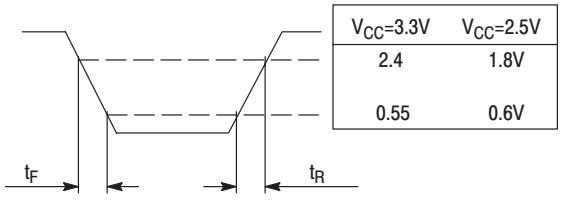



**Figure 16. Output Transition Time Test Reference**

**Order Number: MPC990/D**
**Rev 4, 09/2001**

# Low Voltage PLL Clock Driver

**MPC990**

**LOW VOLTAGE PLL CLOCK DRIVER**



**FA SUFFIX**
52–LEAD TQFP PACKAGE
CASE 848D–03

The MPC990 is a 3.3 V compatible, PLL based clock driver. The fully differential design ensures optimum skew and PLL jitter performance. The performance of the MPC990 makes the device ideal for Workstation, Mainframe Computer and Telecommunication applications. The MPC990 offers an on–board crystal oscillator as the PLL reference and offers a secondary single–ended ECL clock for system test capabilities.

- Fully Integrated PLL
- Output Frequency Up to 400 MHz
- Operates from a 3.3 V Supply
- Output Frequency Configurable
- TQFP Packaging
- ±50 ps Cycle–to–Cycle Jitter

The MPC990 offers three banks of outputs which can each be programmed via the the four fsel pins of the device. There are 16 different output frequency configurations available in the device. The configurations include output ratios of 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 4:3:1 and 4:3:2. The programming table in this data sheet illustrates the various programming options. The SYNC output monitors the relationship between the Qa and Qc output banks. The output pulses per the timing diagrams in this data sheet signal the coincident edges of the two output banks. This feature is useful for non binary relationships between output frequencies (i.e., 3:2 or 4:3 relationships). The Sync_Sel input toggles the Qd outputs between sync signals and extensions to the Qc bank of outputs.



The MPC990 provides a separate output for the feedback to the PLL. This allows for the feedback frequency to be programmed independently of the other outputs allowing for unique input vs output frequency relationships. The fselFB inputs provide 6 different feedback frequencies from the QFB differential output pair. The MPC990 features an external feedback to the PLL.

The PLL_En, Ref_Sel and the Test_Clk input pins provide a means of bypassing the PLL and driving the output buffers directly. This allows the user to single step a design during system debug. Note that the Test_Clk input is routed through the dividers so that, depending on the programming, several edges on the Test_Clk input will be needed to get corresponding edge transitions on the outputs. The VCO_Sel input provides a means of recentering the VCO to provide a broader range of VCO frequencies for stable PLL operation.

If the frequency select or the VCO_Sel pins are changed during operation, a master reset signal must be applied to ensure output synchronization and phase–lock. If the VCO is driven beyond its maximum frequency, the VCO can outrun the internal dividers when the VCO_Sel pin is low. This will also prevent the PLL from achieving lock. Again, a master reset signal will need to be applied to allow for phase–lock. The device employs a power–on reset circuit which will ensure output synchronization and PLL lock on initial power–up.

**Rev 4**

2

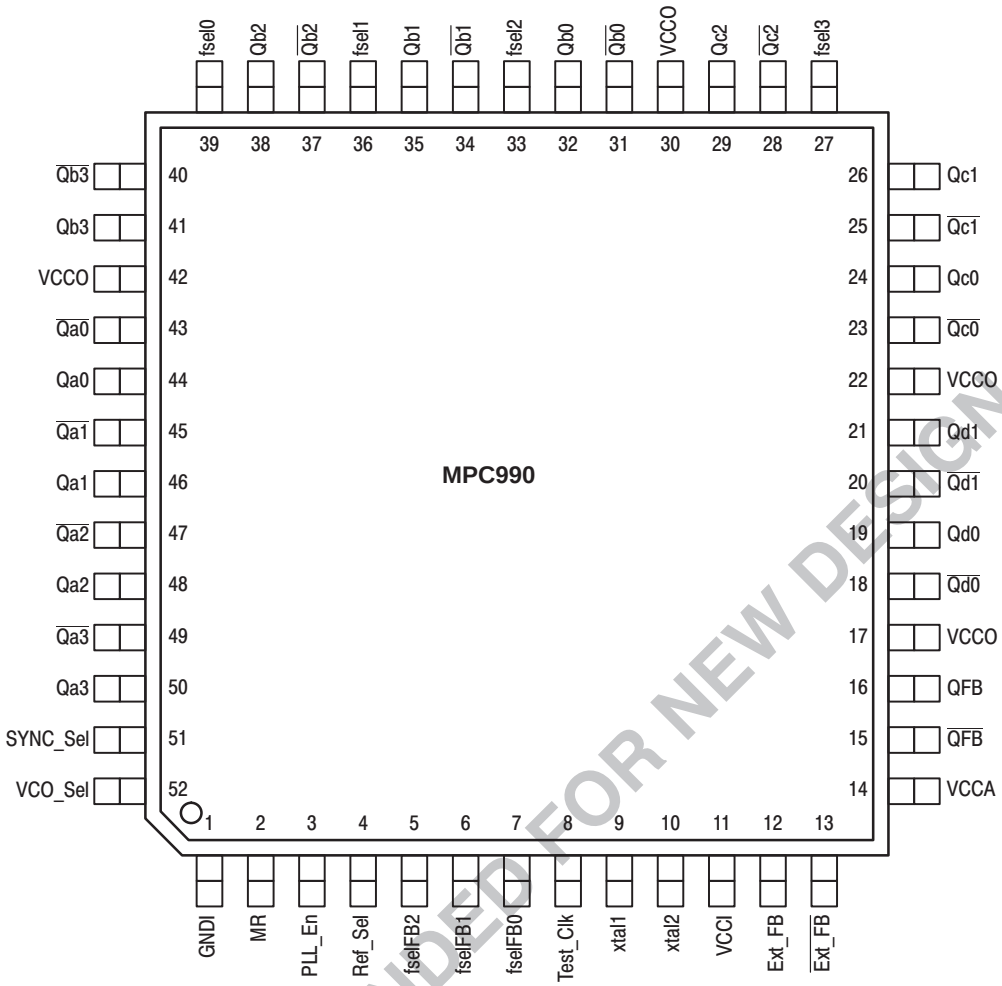



**Figure 1. 52–Lead Pinout** (Top View)



**FUNCTION TABLE 1**

| INPUTS | | | | OUTPUTS | | |
|---|---|---|---|---|---|---|
| **fsel3** | **fsel2** | **fsel1** | **fsel0** | **Qa** | **Qb** | **Qc** |
| 0 | 0 | 0 | 0 | ÷2 | ÷2 | ÷2 |
| 0 | 0 | 0 | 1 | ÷2 | ÷2 | ÷4 |
| 0 | 0 | 1 | 0 | ÷2 | ÷4 | ÷4 |
| 0 | 0 | 1 | 1 | ÷2 | ÷2 | ÷6 |
| 0 | 1 | 0 | 0 | ÷2 | ÷6 | ÷6 |
| 0 | 1 | 0 | 1 | ÷2 | ÷4 | ÷6 |
| 0 | 1 | 1 | 0 | ÷2 | ÷4 | ÷8 |
| 0 | 1 | 1 | 1 | ÷2 | ÷6 | ÷8 |
| 1 | 0 | 0 | 0 | ÷2 | ÷2 | ÷8 |
| 1 | 0 | 0 | 1 | ÷2 | ÷8 | ÷8 |
| 1 | 0 | 1 | 0 | ÷4 | ÷4 | ÷6 |
| 1 | 0 | 1 | 1 | ÷4 | ÷6 | ÷6 |
| 1 | 1 | 0 | 0 | ÷4 | ÷6 | ÷8 |
| 1 | 1 | 0 | 1 | ÷6 | ÷6 | ÷8 |
| 1 | 1 | 1 | 0 | ÷6 | ÷8 | ÷8 |
| 1 | 1 | 1 | 1 | ÷8 | ÷8 | ÷8 |

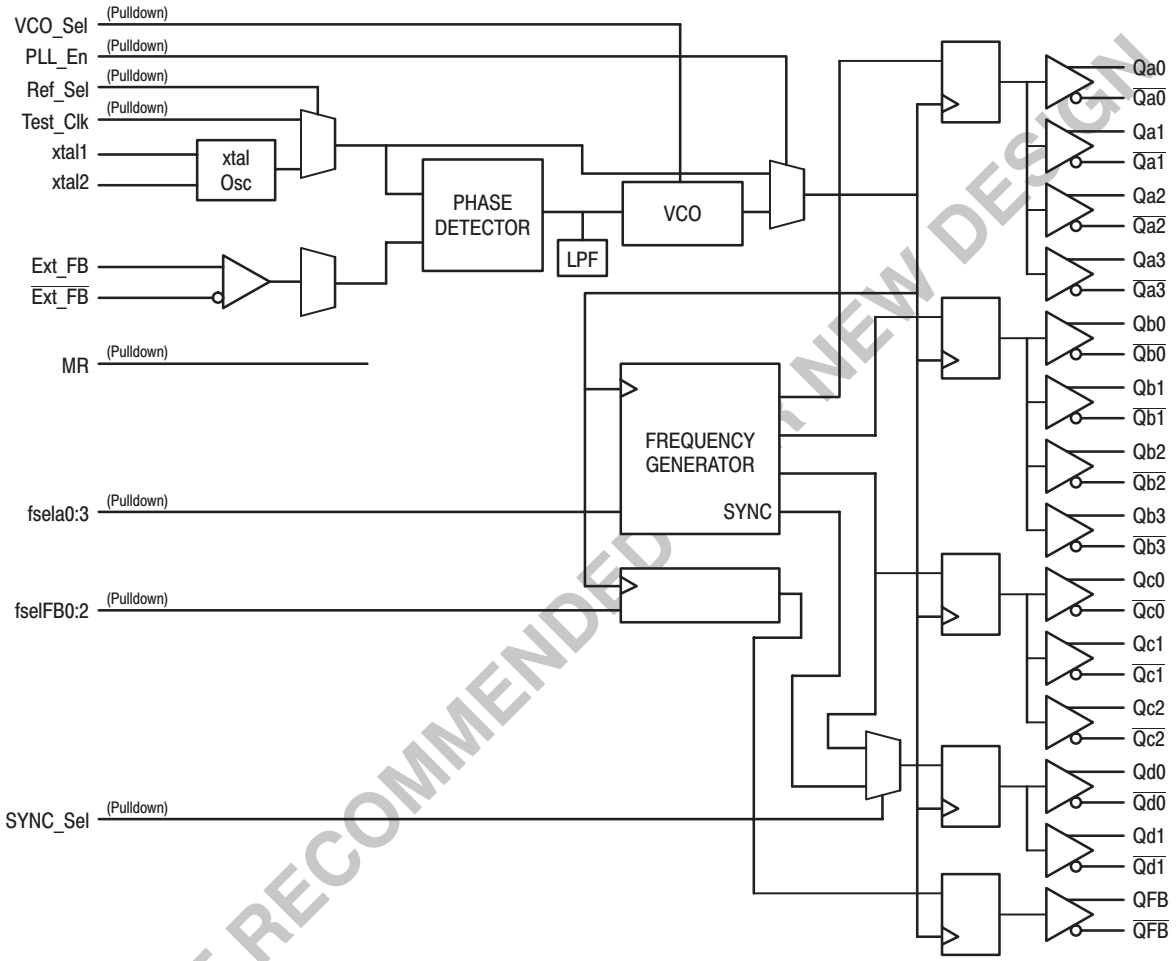
**FUNCTION TABLE 2**

| fselFB2 | fselFB1 | fselFB0 | QFB |
|---|---|---|---|
| 0 | 0 | 0 | ÷2 |
| 0 | 0 | 1 | ÷4 |
| 0 | 1 | 0 | ÷6 |
| 0 | 1 | 1 | ÷8 |
| 1 | 0 | 0 | ÷8 |
| 1 | 0 | 1 | ÷16 |
| 1 | 1 | 0 | ÷24 |
| 1 | 1 | 1 | ÷32 |

**FUNCTION TABLE 3**

| Control Pin | Logic ‘0’ | Logic ‘1’ |
|---|---|---|
| PLL_En | Enable PLL | Bypass PLL |
| VCO_Sel | fVCO | fVCO/2 |
| Ref_Sel | xtal | Test_Clk |
| MR | — | Reset Outputs |
| SYNC_Sel | SYNC Outputs | Match Qc Outputs |






NOTE: Ext_FB has internal pulldowns, while $\overline{\text{Ext\_FB}}$ has external pullups to ensure stability under open input conditions.

**Figure 2. MPC990 Logic Diagram**

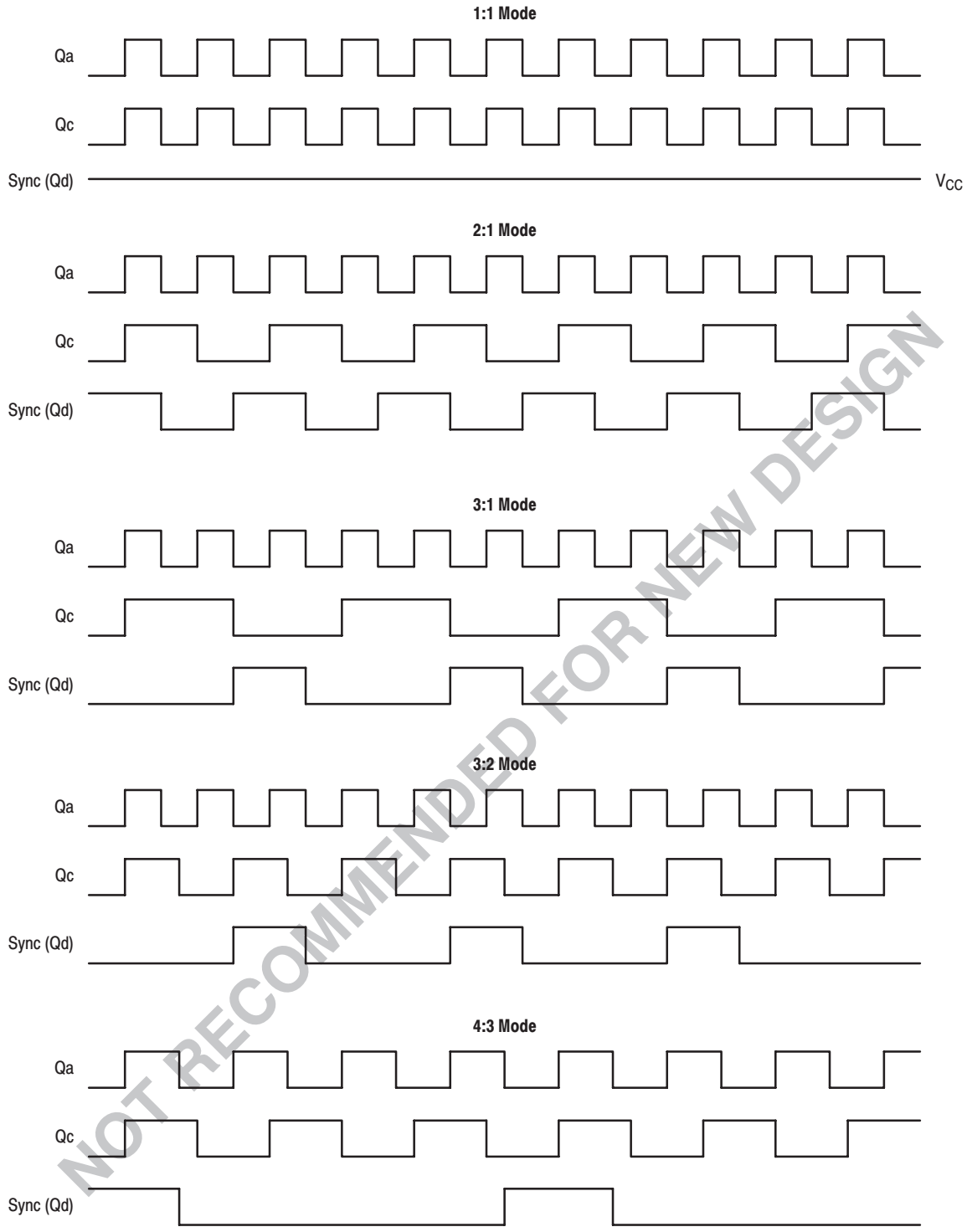





**Figure 3. Timing Diagrams**

**ECL DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CCA}$ = $V_{CCI}$ = $V_{CCO}$ = 0 V, GNDI = –3.3 V ±5%, Note 1.)

| | | 0°C | | | 25°C | | | 70°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $V_{OH}$ | Output HIGH Voltage | –1.3 | | –0.7 | –1.3 | –1.0 | –0.7 | –1.3 | | –0.7 | V |
| $V_{OL}$ | Output LOW Voltage | –2.0 | | –1.4 | –2.0 | –1.7 | –1.4 | –2.0 | | –1.4 | V |
| $V_{IH}$ | Input HIGH Voltage | –1.1 | | –0.9 | –1.1 | | –0.9 | –1.1 | | –0.9 | V |
| $V_{IL}$ | Input LOW Voltage | –1.8 | | –1.5 | –1.8 | | –1.5 | –1.8 | | –1.5 | V |
| $V_{PP}$ | Minimum Input Swing | 500 | | | 500 | | | 500 | | | mV |
| $V_{CMR}$ | Common Mode Range | $V_{CC}$ –1.3 V | | $V_{CC}$ –0.5 V | $V_{CC}$ –1.3 V | | $V_{CC}$ –0.5 V | $V_{CC}$ –1.3 V | | $V_{CC}$ –0.5 V | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | µA |
| $I_{GNDI}$ | Power Supply Current | | 200 | 240 | | 200 | 240 | | 200 | 240 | mA |

1. Refer to Motorola Application Note AN1545/D "*Thermal Data for MPC Clock Drivers*" for thermal management guidelines.

**PECL DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CCA}$ = $V_{CCI}$ = $V_{CCO}$ = 3.3 V ±5%, GNDI = 0 V, Note 2.)

| | | 0°C | | | 25°C | | | 70°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $V_{OH}$ | Output HIGH Voltage (Note 3.) | 2.0 | | 2.6 | 2.0 | 2.3 | 2.6 | 2.3 | | 2.6 | V |
| $V_{OL}$ | Output LOW Voltage (Note 3.) | 1.3 | | 1.9 | 1.3 | 1.6 | 1.9 | 1.3 | | 1.9 | V |
| $V_{IH}$ | Input HIGH Voltage (Note 3.) | 2.2 | | 2.4 | 2.2 | | 2.4 | 2.2 | | 2.4 | V |
| $V_{IL}$ | Input LOW Voltage (Note 3.) | 1.5 | | 1.8 | 1.5 | | 1.8 | 1.5 | | 1.8 | V |
| $V_{PP}$ | Minimum Input Swing | 500 | | | 500 | | | 500 | | | mV |
| $V_{CMR}$ | Common Mode Range | $V_{CC}$ –1.3 V | | $V_{CC}$ –0.5 V | $V_{CC}$ –1.3 V | | $V_{CC}$ –0.5 V | $V_{CC}$ –1.3 V | | $V_{CC}$ –0.5 V | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | µA |
| $I_{GNDI}$ | Power Supply Current | | 200 | 240 | | 200 | 240 | | 200 | 240 | mA |

2. Refer to Motorola Application Note AN1545/D "*Thermal Data for MPC Clock Drivers*" for thermal management guidelines.
3. These values are for $V_{CC}$ = 3.3 V. Level Specifications will vary 1:1 with $V_{CC}$.

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CCA}$ = $V_{CCI}$ = $V_{CCO}$ = 3.3 V ±5%, Termination of 50 Ω to $V_{CC}$ – 2.0 V)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $f_{xtal}$ | Crystal Oscillator Frequency | 10 | | 25 | MHz | |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.2 | | 1.0 | ns | 20% to 80% |
| $t_{pw}$ | Output Duty Cycle | 47.5 | 50 | 52.5 | % | |
| $t_{os}$ | Output-to-Output Skew Same Frequency<br>Different Frequencies | | 150<br>250 | 250<br>350 | ps | |
| $f_{VCO}$ | PLL VCO Lock Range VCO_Sel = '0'<br>VCO_Sel = '1' | 400<br>200 | | 800<br>400 | MHz | FB ÷8 to ÷32 (Note 4.)<br>FB ÷4 to ÷32 |
| $t_{pd}$ | Ref to Feedback Offset | 75 | 250 | 425 | ps | $f_{ref}$ = 50 MHz (Note 5.) |
| $f_{max}$ | Maximum Output Frequency Qa,Qb,Qc (÷2)<br>Qa,Qb,Qc (÷4)<br>Qa,Qb,Qc (÷6)<br>Qa,Qb,Qc (÷8) | | | 400<br>200<br>133<br>100 | MHz | |
| $t_{jitter}$ | Cycle–to–Cycle Jitter (Peak–to–Peak) | | ±50 | | ps | |
| $t_{lock}$ | Maximum PLL Lock Time | | | 10 | ms | |

4. With VCO_Sel = '0', the PLL will be unstable with a ÷2, ÷4 and some ÷6 feedback configurations. With VCO_Sel = '1', the PLL will be unstable with a ÷2 feedback ratio.
5. $t_{pd}$ is specified for 50MHz input reference FB ÷8. The window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The $t_{pd}$ does not include jitter.

**PLL INPUT REFERENCE CHARACTERISTICS** ($T_A$=0 to 70°C)

| Symbol | Characteristic | | Min | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $t_r$, $t_f$ | TCLK Input Rise/Falls | | | 3.0 | ns | |
| $f_{ref}$ | Reference Input Frequency VCO_SEL='0' | Feedback divide 6<br>Feedback divide 8<br>Feedback divide 16<br>Feedback divide 24<br>Feedback divide 32 | 100<br>50<br>25<br>16.67<br>12.5 | 125<br>100<br>50<br>33.33<br>25 | MHz | |
| | VCO_SEL='1' | Feedback divide 4<br>Feedback divide 6<br>Feedback divide 8<br>Feedback divide 16<br>Feedback divide 24<br>Feedback divide 32 | 50<br>33.3<br>25<br>12.5<br>8.33<br>6.25 | 100<br>66.67<br>50<br>25<br>16.67<br>12.5 | | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 25 | 75 | % | |

## APPLICATIONS INFORMATION

### Using the On–Board Crystal Oscillator

The MPC990 features an on–board crystal oscillator to allow for seed clock generation as well as final distribution. The on–board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC990 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required.

The oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on–board capacitors. Because the design is a series resonant design for the optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most of the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC990 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implementations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

The MPC990 is a clock driver which was designed to generate outputs with programmable frequency relationships and not a synthesizer with a fixed input frequency. As a result the crystal input frequency is a function of the desired output frequency. For a design which utilizes the external feedback to the PLL the selection of the crystal frequency is straight forward; simply chose a crystal which is equal in frequency to the fed back signal.

**Table 3. Crystal Specifications**

| Parameter | Value |
|---|---|
| Crystal Cut | Fundamental at Cut |
| Resonance | Series Resonance* |
| Frequency Tolerance | ±75 ppm at 25°C |
| Frequency/Temperature Stability | ±150 pm 0 to 70°C |
| Operating Range | 0 to 70°C |
| Shunt Capacitance | 5–7 pF |
| Equivalent Series Resistance (ESR) | 50 to 80 Ω Max |
| Correlation Drive Level | 100 μW |
| Aging | 5 ppm/Yr (First 3 Years) |

* See accompanying text for series versus parallel resonant discussion.

### Power Supply Filtering

The MPC990 provides a separate power supply for the internal PLL of the device. The purpose of this design technique is to allow the user to filter externally generated system noise from the internal, relatively sensitive analog PLL.

Figure 4 illustrates a suggested power supply filter using an LC filter network. The inductor value should be chosen to maximize the AC filter impedance while maintaining a low DC resistance. An inductor with a maximum DC series resistance of 5 Ω should be used. The parallel capacitor combination on the $V_{CCA}$ pin ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

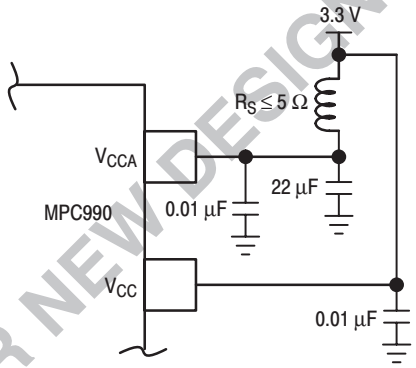



**Figure 4. Power Supply Filter**

**Order Number: MPC991/D**
**Rev 0, 08/2001**

# Low Voltage PLL Clock Driver

**MPC991**

**See Upgrade Product – MPC9991**

**LOW VOLTAGE PLL CLOCK DRIVER**

**FA SUFFIX**
52–LEAD TQFP PACKAGE
CASE 848D–03

2

The MPC991 is a 3.3 V compatible, PLL based ECL/PECL clock driver. The fully differential design ensures optimum skew and PLL jitter performance. The performance of the MPC991 makes the device ideal for Workstation, Mainframe Computer and Telecommunication applications. The MPC991 offers a differential ECL/PECL input for applications which need to lock to an existing clock signal. It also offers a secondary single–ended ECL clock for system test capabilities.

- Fully Integrated PLL
- Output Frequency up to 400 MHz
- ECL/PECL Inputs and Outputs
- Operates from a 3.3 V Supply
- Output Frequency Configurable
- TQFP Packaging
- ±50 ps Cycle–to–Cycle Jitter

The MPC991 offers three banks of outputs which can each be programmed via the the four fsel pins of the device. There are 16 different output frequency configurations available in the device. The configurations include output ratios of 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 4:3:1 and 4:3:2. The programming table in this data sheet illustrates the various programming options. The SYNC output monitors the relationship between the Qa and Qc output banks. The output pulses per the timing diagrams in this data sheet signal the coincident edges of the two output banks. This feature is useful for non binary relationships between output frequencies (i.e., 3:2 or 4:3 relationships). The Sync_Sel input toggles the Qd outputs between sync signals and extensions to the Qc bank of outputs.

The MPC991 provides a separate output for the feedback to the PLL. This allows for the feedback frequency to be programmed independently of the other outputs allowing for unique input vs output frequency relationships. The fselFB inputs provide 6 different feedback frequencies from the QFB differential output pair.

The MPC991 features an external differential ECL/PECL feedback to the PLL. This external feedback feature allows the MPC991 to be used as a “zero” delay buffer. The propagation delay between the input reference and the output is dependent on the input reference frequency. The selection of higher reference frequencies will provide near zero delay through the device.

The PLL_En, Ref_Sel and the Test_Clk input pins provide a means of bypassing the PLL and driving the output buffers directly. This allows the user to single step a design during system debug. Note that the Test_Clk input is routed through the dividers so that depending on the programming several edges on the Test_Clk input will be needed to get corresponding edge transitions on the outputs. The VCO_Sel input provides a means of recentering the VCO to provide a broader range of VCO frequencies for stable PLL operation.

If the frequency select or the VCO_Sel pins are changed during operation, a master reset signal must be applied to ensure output synchronization and phase–lock. If the VCO is driven beyond its maximum frequency, the VCO can outrun the internal dividers when the VCO_Sel pin is low. This will also prevent the PLL from achieving lock. Again, a master reset signal will need to be applied to allow for phase–lock. The device employs a power–on reset circuit which will ensure output synchronization and PLL lock on initial power–up.

**Rev 0**

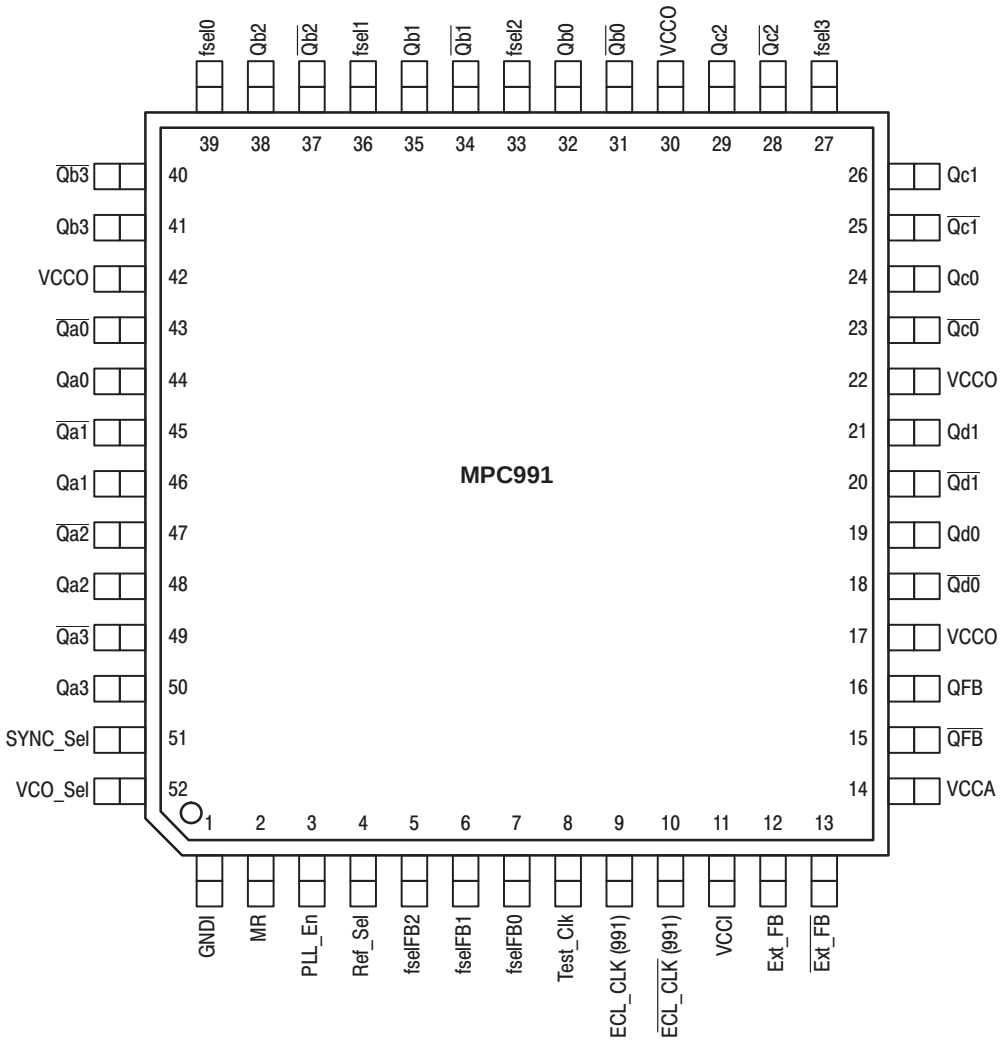



**Figure 1. 52–Lead Pinout** (Top View)

**FUNCTION TABLE 1**

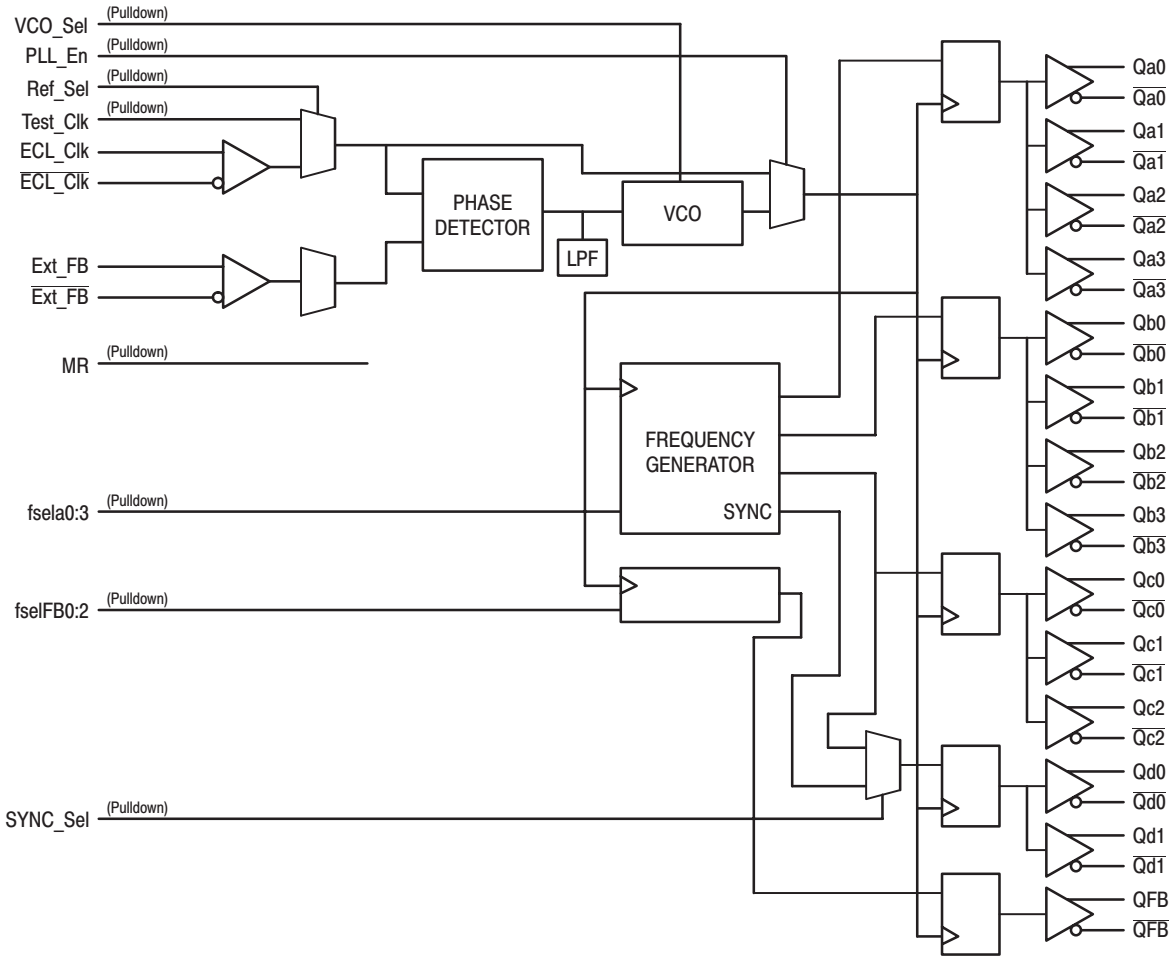
| INPUTS | | | | OUTPUTS | | |
|---|---|---|---|---|---|---|
| **fsel3** | **fsel2** | **fsel1** | **fsel0** | **Qa** | **Qb** | **Qc** |
| 0 | 0 | 0 | 0 | ÷2 | ÷2 | ÷2 |
| 0 | 0 | 0 | 1 | ÷2 | ÷2 | ÷4 |
| 0 | 0 | 1 | 0 | ÷2 | ÷4 | ÷4 |
| 0 | 0 | 1 | 1 | ÷2 | ÷2 | ÷6 |
| 0 | 1 | 0 | 0 | ÷2 | ÷6 | ÷6 |
| 0 | 1 | 0 | 1 | ÷2 | ÷4 | ÷6 |
| 0 | 1 | 1 | 0 | ÷2 | ÷4 | ÷8 |
| 0 | 1 | 1 | 1 | ÷2 | ÷6 | ÷8 |
| 1 | 0 | 0 | 0 | ÷2 | ÷2 | ÷8 |
| 1 | 0 | 0 | 1 | ÷2 | ÷8 | ÷8 |
| 1 | 0 | 1 | 0 | ÷4 | ÷4 | ÷6 |
| 1 | 0 | 1 | 1 | ÷4 | ÷6 | ÷6 |
| 1 | 1 | 0 | 0 | ÷4 | ÷6 | ÷8 |
| 1 | 1 | 0 | 1 | ÷6 | ÷6 | ÷8 |
| 1 | 1 | 1 | 0 | ÷6 | ÷8 | ÷8 |
| 1 | 1 | 1 | 1 | ÷8 | ÷8 | ÷8 |

**FUNCTION TABLE 2**

| fselFB2 | fselFB1 | fselFB0 | QFB |
|---|---|---|---|
| 0 | 0 | 0 | ÷2 |
| 0 | 0 | 1 | ÷4 |
| 0 | 1 | 0 | ÷6 |
| 0 | 1 | 1 | ÷8 |
| 1 | 0 | 0 | ÷8 |
| 1 | 0 | 1 | ÷16 |
| 1 | 1 | 0 | ÷24 |
| 1 | 1 | 1 | ÷32 |

**FUNCTION TABLE 3**

| Control Pin | Logic ‘0’ | Logic ‘1’ |
|---|---|---|
| PLL_En | Enable PLL | Bypass PLL |
| VCO_Sel | fVCO | fVCO/2 |
| Ref_Sel | ECL/PECL | Test_Clk |
| MR | — | Reset Outputs |
| SYNC_Sel | SYNC Outputs | Match Qc Outputs |




NOTE: ECL_Clk, Ext_FB have internal pulldowns, while $\overline{\text{ECL\_Clk}}$, $\overline{\text{Ext\_FB}}$ have external pullups to ensure stability under open input conditions.

**Figure 2. MPC991 Logic Diagram**

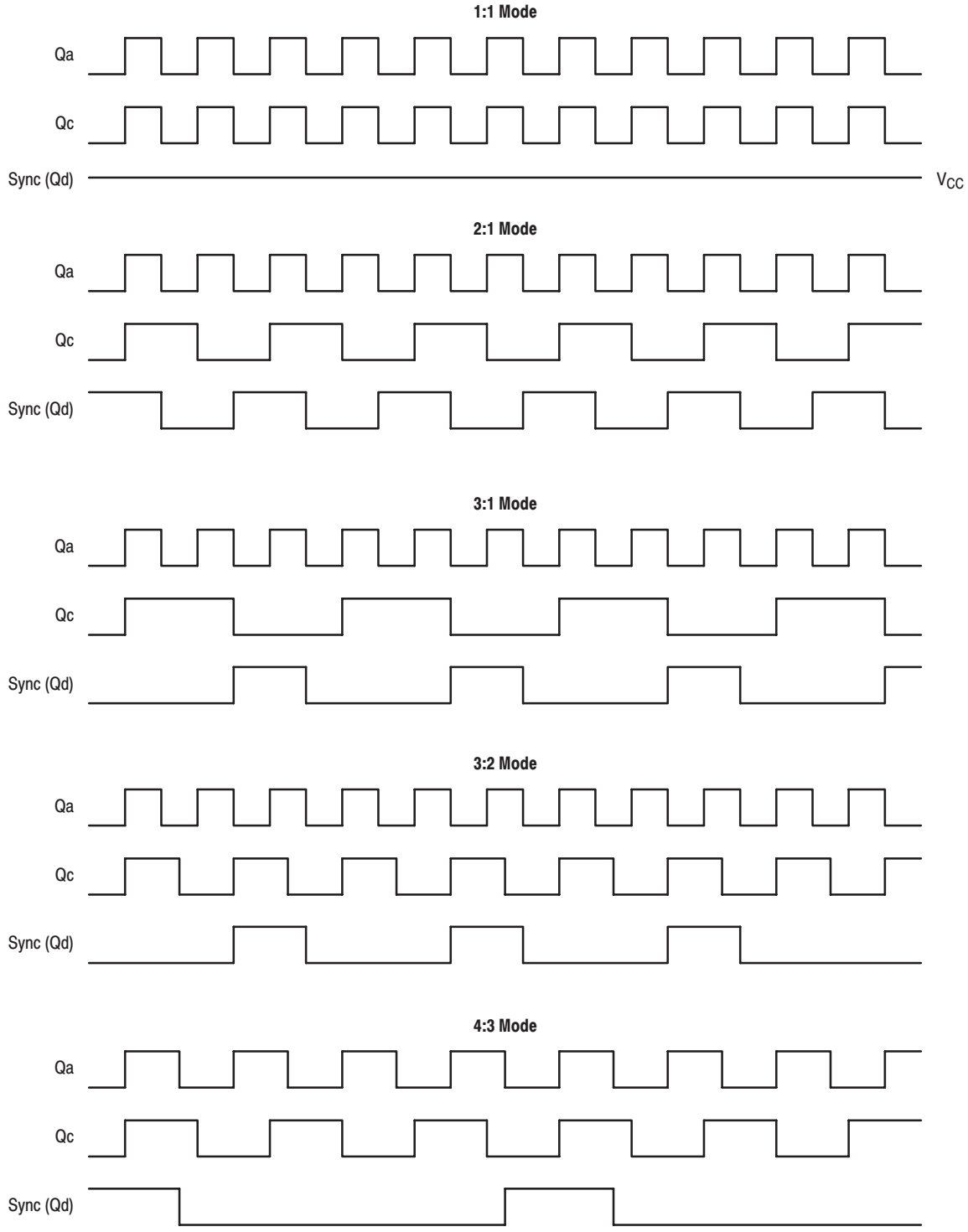



**Figure 3. Timing Diagrams**

**ECL DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CCA}$ = $V_{CCI}$ = $V_{CCO}$ = 0 V, GNDI = –3.3 V ±5%, Note 1.)

| | | 0°C | | | 25°C | | | 70°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $V_{OH}$ | Output HIGH Voltage | –1.3 | | –0.7 | –1.3 | –1.0 | –0.7 | –1.3 | | –0.7 | V |
| $V_{OL}$ | Output LOW Voltage | –2.0 | | –1.4 | –2.0 | –1.7 | –1.4 | –2.0 | | –1.4 | V |
| $V_{IH}$ | Input HIGH Voltage | –1.1 | | –0.9 | –1.1 | | –0.9 | –1.1 | | –0.9 | V |
| $V_{IL}$ | Input LOW Voltage | –1.8 | | –1.5 | –1.8 | | –1.5 | –1.8 | | –1.5 | V |
| $V_{PP}$ | Minimum Input Swing | 500 | | | 500 | | | 500 | | | mV |
| $V_{CMR}$ | Common Mode Range | $V_{CC}$ –1.3V | | $V_{CC}$ –0.5V | $V_{CC}$ –1.3V | | $V_{CC}$ –0.5V | $V_{CC}$ –1.3V | | $V_{CC}$ –0.5V | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | µA |
| $I_{GNDI}$ | Power Supply Current | | 200 | 240 | | 200 | 240 | | 200 | 240 | mA |

1. Refer to Motorola Application Note AN1545/D "*Thermal Data for MPC Clock Drivers*" for thermal management guidelines.

**PECL DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CCA}$ = $V_{CCI}$ = $V_{CCO}$ = 3.3 V ±5%, GNDI = 0 V, Note 2.)

| | | 0°C | | | 25°C | | | 70°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $V_{OH}$ | Output HIGH Voltage (Note 3.) | 2.0 | | 2.6 | 2.0 | 2.3 | 2.6 | 2.3 | | 2.6 | V |
| $V_{OL}$ | Output LOW Voltage (Note 3.) | 1.3 | | 1.9 | 1.3 | 1.6 | 1.9 | 1.3 | | 1.9 | V |
| $V_{IH}$ | Input HIGH Voltage (Note 3.) | 2.2 | | 2.4 | 2.2 | | 2.4 | 2.2 | | 2.4 | V |
| $V_{IL}$ | Input LOW Voltage (Note 3.) | 1.5 | | 1.8 | 1.5 | | 1.8 | 1.5 | | 1.8 | V |
| $V_{PP}$ | Minimum Input Swing | 500 | | | 500 | | | 500 | | | mV |
| $V_{CMR}$ | Common Mode Range | $V_{CC}$ –1.3V | | $V_{CC}$ –0.5V | $V_{CC}$ –1.3V | | $V_{CC}$ –0.5V | $V_{CC}$ –1.3V | | $V_{CC}$ –0.5V | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | µA |
| $I_{GNDI}$ | Power Supply Current | | 200 | 240 | | 200 | 240 | | 200 | 240 | mA |

2. Refer to Motorola Application Note AN1545/D "*Thermal Data for MPC Clock Drivers*" for thermal management guidelines.
3. These values are for $V_{CC}$ = 3.3V. Level Specifications will vary 1:1 with $V_{CC}$.

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CCA}$ = $V_{CCI}$ = $V_{CCO}$ = 3.3 V ±5%, Termination of 50 Ω to $V_{CC}$ – 2.0 V)

| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Unit** | **Condition** |
|---|---|---|---|---|---|---|
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.2 | | 1.0 | ns | 20% to 80% |
| $t_{pw}$ | Output Duty Cycle | 47.5 | 50 | 52.5 | % | |
| $t_{os}$ | Output-to-Output Skew Same Frequency<br>Different Frequencies | | 150<br>250 | 250<br>350 | ps | |
| $f_{VCO}$ | PLL VCO Lock Range VCO_Sel = '0'<br>VCO_Sel = '1' | 400<br>200 | | 800<br>400 | MHz | FB ÷8 to ÷32 (Note 4.)<br>FB ÷4 to ÷32 |
| $t_{pd}$ | Ref to Feedback Offset | 75 | 250 | 425 | ps | $f_{ref}$ = 50MHz (Note 5.) |
| $f_{max}$ | Maximum Output Frequency Qa,Qb,Qc (÷2)<br>Qa,Qb,Qc (÷4)<br>Qa,Qb,Qc (÷6)<br>Qa,Qb,Qc (÷8) | | | 400<br>200<br>133<br>100 | MHz | |
| $t_{jitter}$ | Cycle–to–Cycle Jitter (Peak–to–Peak) | | ±50 | | ps | |
| $t_{lock}$ | Maximum PLL Lock Time | | | 10 | ms | |

4. With VCO_Sel = '0', the PLL will be unstable with a ÷2, ÷4 and some ÷6 feedback configurations. With $V_{CO\_Sel}$ = '1', the PLL will be unstable with a ÷2 feedback ratio.
5. $t_{pd}$ is specified for 50MHz input reference FB ÷ 8. The window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The $t_{pd}$ does not include jitter.

**PLL INPUT REFERENCE CHARACTERISTICS** ($T_A$ = 0 to 70°C)

| Symbol | Characteristic | | Min | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $t_r$, $t_f$ | TCLK Input Rise/Falls | | | 3.0 | ns | |
| $f_{ref}$ | Reference Input Frequency VCO_SEL='0' | Feedback divide 6 | 100 | 125 | MHz | |
| | | Feedback divide 8 | 50 | 100 | | |
| | | Feedback divide 16 | 25 | 50 | | |
| | | Feedback divide 24 | 16.67 | 33.33 | | |
| | | Feedback divide 32 | 12.5 | 25 | | |
| | VCO_SEL='1' | Feedback divide 4 | 50 | 100 | | |
| | | Feedback divide 6 | 33.3 | 66.67 | | |
| | | Feedback divide 8 | 25 | 50 | | |
| | | Feedback divide 16 | 12.5 | 25 | | |
| | | Feedback divide 24 | 8.33 | 16.67 | | |
| | | Feedback divide 32 | 6.25 | 12.5 | | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 25 | 75 | % | |

2

## APPLICATIONS INFORMATION

### Power Supply Filtering

The MPC991 provides a separate power supply for the internal PLL of the device. The purpose of this design technique is to allow the user to filter externally generated system noise from the internal, relatively sensitive analog PLL.

Figure 4 illustrates a suggested power supply filter using an LC filter network. The inductor value should be choosen to maximize the AC filter impedance while maintaining a low DC resistance. An inductor with a maximum DC series resistance of 5 Ω should be used. The parallel capacitor combination on the $V_{CCA}$ pin ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

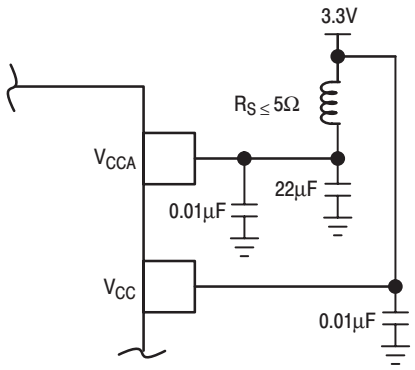



**Figure 4. Power Supply Filter**

**Order Number: MPC992/D**
**Rev. 2, 08/2001**

# Low Voltage PECL PLL Clock Driver

**MPC992**

**See Upgrade Product – MPC9992**

**LOW VOLTAGE PLL CLOCK DRIVER**

**FA SUFFIX**
PLASTIC TQFP PACKAGE
CASE 873A-02

2

The MPC992 is a 3.3V compatible, PLL based PECL clock generator and distributor. The fully differential design ensures optimum skew and PLL jitter performance. The performance of the device makes the MPC992 ideal for workstations, main frame computer, telecommunication and instrumentation applications. The device offers a crystal oscillator or a differential PECL reference clock input to provide flexibility in the reference clock interface. All of the control signals to the MPC992 are LVTTL compatible inputs.

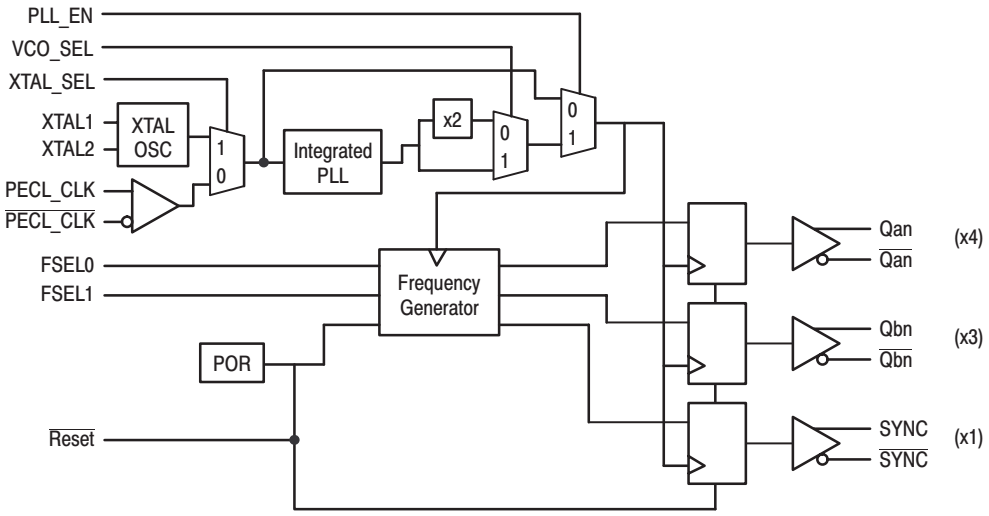
- Fully Integrated PLL
- Output Frequency of up to 400MHz
- PECL Clock Inputs and Outputs
- Operates from a 3.3V $V_{CC}$ Supply
- Output Frequency Configurable
- 32 TQFP Packaging
- ±25ps Cycle–Cycle Jitter

The MPC992 offers two banks of outputs which can be configured into four different relationships. The output banks can be configured into 2:1, 3:1, 3:2 and 5:2 ratios to provide a wide variety of potential frequency outputs. In addition to these two banks of outputs a synchronization output is also offered. The SYNC output will provide information as to the time when the two output banks will transition positively in phase. This information can be important when the odd ratios are used as it provides for a baseline point in the system timing. The SYNC output will pulse high for one Qa clock period, centered on the rising Qa clock edge four edges prior to the Qb synchronous edge. The relationship is illustrated in the timing diagrams in the data sheet.

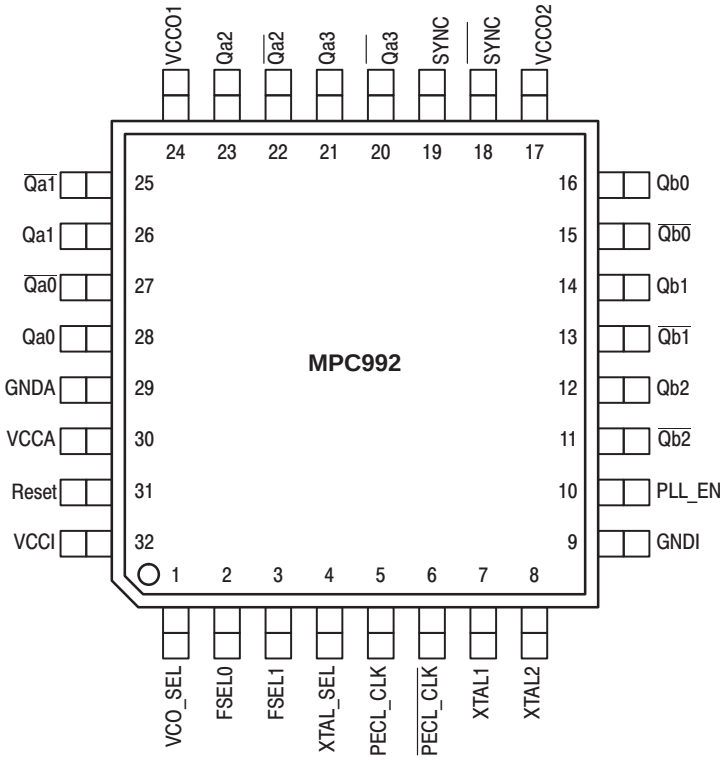
The MPC992 offers several features to aid in system debug and test. The PECL reference input pins can be interfaced to a test signal and the PLL can be bypassed to allow the designer to drive the MPC992 outputs directly. This allows for single stepping in a system functional debug mode. In addition an overriding reset is provided which will force all of the Q outputs LOW upon assertion.

The MPC992 is packaged in a 32–lead TQFP package to optimize both performance and board density.

**MPC992 LOGIC DIAGRAM**




**Rev 2**




**FUNCTION TABLE 1**

| FSEL0 | FSEL1 | Qa | Qb | Feedback | Ratio |
|---|---|---|---|---|---|
| 0 | 0 | VCO/4 | VCO/6 | VCO/24 | 3:2 |
| 0 | 1 | VCO/2 | VCO/4 | VCO/16 | 2:1 |
| 1 | 0 | VCO/4 | VCO/10 | VCO/40 | 5:2 |
| 1 | 1 | VCO/2 | VCO/6 | VCO/24 | 3:1 |

**INPUT vs OUTPUT FREQUENCY**

| FSEL0 | FSEL1 | Qa | Qb | Int Feedback |
|---|---|---|---|---|
| 0 | 0 | 6 ($f_{ref}$) | 4 ($f_{ref}$) | $f_{ref}$ |
| 0 | 1 | 8 ($f_{ref}$) | 4 ($f_{ref}$) | $f_{ref}$ |
| 1 | 0 | 10 ($f_{ref}$) | 4 ($f_{ref}$) | $f_{ref}$ |
| 1 | 1 | 12 ($f_{ref}$) | 4 ($f_{ref}$) | $f_{ref}$ |

**FUNCTION TABLE 2**

| Control Signal | Logic ‘0’ | Logic ‘1’ |
|---|---|---|
| Reset | Outputs Enabled | Outputs Disabled |
| XTAL_SEL | PECL REF | XTAL REF |
| PLL_EN | Disabled | Enabled |
| VCO_SEL | High Frequency | Low Frequency |

**PIN DESCRIPTION**

| Pin Name | Function |
|---|---|
| VCO_SEL | VCO range select pin (Int Pullup) |
| PLL_EN | PLL bypass select pin (Int Pullup) |
| XTAL_SEL | Input reference source select pin (Int Pullup) |
| XTAL1:2 | Crystal interface pins for the internal oscillator |
| PECL_CLK | True PECL reference clock input (Int Pulldown) |
| $\overline{\text{PECL\_CLK}}$ | Compliment PECL reference clock input (Int Pullup) |
| FSELn | Internal divider select pins (Int Pullup) |
| RESET | Internal flip–flop reset, true outputs go LOW (Int Pulldown) |

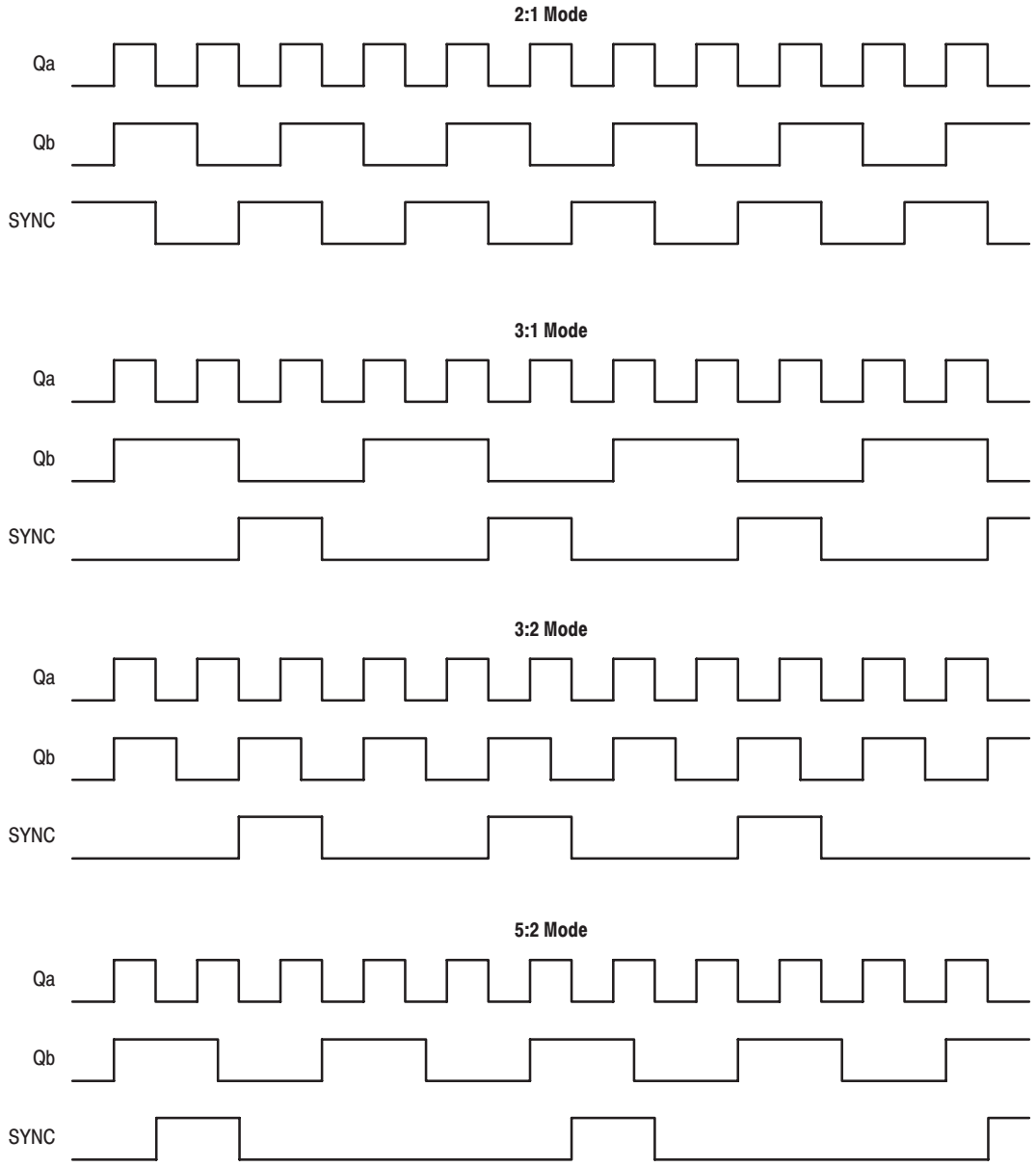



**Figure 1. Output Waveforms**

**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 4.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_{OUT}$ | Output Current Continuous<br>Surge | | 50<br>100 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | PECL_CLK[1]<br>Other | 2.15<br>2.0 | | 2.4<br>$V_{CC}$ | V | $V_{CC}$ = 3.3V |
| $V_{IL}$ | Input LOW Voltage | PECL_CLK[1]<br>Other | 1.5<br>0 | | 1.8<br>0.8 | V | $V_{CC}$ = 3.3V |
| $V_{OH}$ | Output HIGH Voltage[1] | | 1.8 | | 2.4 | V | $V_{CC}$ = 3.3V |
| $V_{OL}$ | Output LOW Voltage[1] | | 1.2 | | 1.7 | V | $V_{CC}$ = 3.3V |
| $I_{IN}$ | Input Current | | –120 | | 120 | µA | |
| $I_{CCI}$ | Maximum Quiescent Supply Current | | | 130 | 150 | mA | |
| $I_{CCA}$ | Maximum PLL Supply Current | | | 15 | 20 | mA | |

1. DC levels will vary 1:1 with $V_{CC}$.

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $t_r$, $t_f$ | Output Rise/Fall Time | | 200 | | 850 | ps | 20% to 80% |
| $t_{pw1}$ | Output Duty Cycle | | 49 | | 51 | % | |
| $t_{pw2}$ | SYNC Output Duty Cycle | | 0.95 | | 1.05 | % | PCLK Period |
| $f_{ref}$ | Input Reference Frequency | Xtal<br>FREF | 10<br>Note 2 | | 20<br>Note 2 | MHz | |
| $t_{os}$ | Output-to-Output Skew | Qa, Qb<br>Qa (–) to SYNC (+) | | | 100<br>300 | ps | |
| $f_{VCO}$ | PLL VCO Lock Range | | 200<br>400 | | 440<br>750 | MHz | VCO_SEL = 1<br>VCO_SEL = 0 |
| $f_{max}$ | Maximum Output Frequency | Qa (÷2)<br>Qa,Qb (÷4)<br>Qb (÷6)<br>Qb (÷10) | | | 375<br>187.5<br>125<br>75 | MHz | Note 1 |
| $t_{jitter}$ | Cycle–to–Cycle Jitter (Peak–to–Peak) | | | ±25 | ±50 | ps | Note 3 |
| $t_{lock}$ | Maximum PLL Lock Time | | | | 10 | ms | |

1. At 400MHz the output swing will be less than the nominal value.
2. ECLK and XTAL input reference limited by the feedback divide and the guaranteed VCO lock range.
3. Guaranteed by characterization.

## APPLICATIONS INFORMATION



### Using the On–Board Crystal Oscillator

The MPC992 features an on–board crystal oscillator to allow for seed clock generation as well as final distribution. The on–board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC992 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required.

The oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on–board capacitors. Because the design is a series resonant design, for optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most off the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC992 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implementations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

Figure 2 shows an optional series capacitor in the crystal oscillator interface. The on–board oscillator introduces a small phase shift in the overall loop which causes the oscillator to operate at a frequency slightly slower than the specified crystal. The series capacitor is used to compensate the loop and allow the oscillator to function at the specified crystal frequency. If a 100ppm type error is not important, the capacitor can be left off the PCB. For more detailed information, order Motorola Application Note AN1579/D.

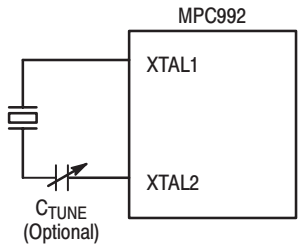



**Figure 2. Recommended Crystal Interface**

**Table 4. Crystal Specifications**

| Parameter | Value |
|---|---|
| Crystal Cut | Fundamental AT Cut |
| Resonance | Series Resonance* |
| Frequency Tolerance | ±75ppm at 25°C |
| Frequency/Temperature Stability | ±150ppm 0 to 70°C |
| Operating Range | 0 to 70°C |
| Shunt Capacitance | 5–7pF |
| Equivalent Series Resistance (ESR) | 50 to 80Ω max |
| Correlation Drive Level | 100μW |
| Aging | 5ppm/Yr (First 3 Years) |

### Power Supply Filtering

The MPC992 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC992 provides separate power supplies for the digital circuitry ($V_{CCI}$) and the internal PLL (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC992.

Figure 3 illustrates a typical power supply filter scheme. The MPC992 is most susceptible to noise with spectral content in the 10kHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the VCCA pin of the MPC992. From the data sheet the $I_{VCCA}$ current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V $V_{CC}$ supply is used. The resistor shown in Figure 3 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

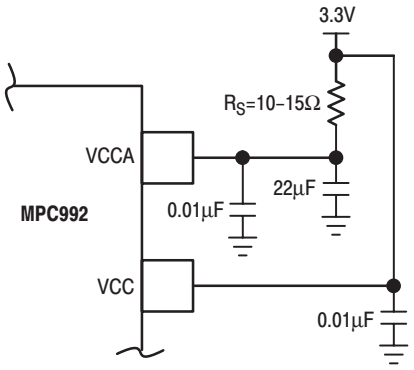



**Figure 3. Power Supply Filter**

A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000µH choke will show a significant impedance at 10KHz frequencies and above. Because of the current draw and the voltage that must be maintained on the VCCA pin a low DC resistance inductor is required (less than 15Ω). Generally the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering.

The MPC992 provides sub–nanosecond output edge rates and thus a good power supply bypassing scheme is a must. The important aspect of the layout for the MPC992 is low impedance connections between VCC and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the MPC992 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors.

No active signal lines should pass below the crystal interface to the MPC992. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on–board oscillator. In addition, the crystal interface circuitry will be adversely affected by activity on the PECL_CLK inputs. Therefore, it is recommended that the PECL input signals be static when the crystal oscillator circuitry is being used.

Although the MPC992 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

# Intelligent Dynamic Clock Switch (IDCS) PLL Clock Driver

**MPC993**

**See Upgrade Product – MPC9993**

2

The MPC993 is a PLL clock driver designed specifically for redundant clock tree designs. The device receives two differential LVPECL clock signals from which it generates 5 new differential LVPECL clock outputs. Two of the output pairs regenerate the input signals frequency and phase while the other three pairs generate 2x, phase aligned clock outputs. External PLL feedback is used to also provide zero delay buffer performance.

**FA SUFFIX**
32–LEAD PLASTIC LQFP PACKAGE
CASE 873A–02

- Fully Integrated PLL
- Intelligent Dynamic Clock Switch
- LVPECL Clock Outputs
- LVCMOS Control/Statis I/O
- 3.3V Operation
- 32–Lead LQFP Packaging
- ±50ps Cycle–Cycle Jitter

The MPC993 Intelligent Dynamic Clock Switch (IDCS) circuit continuously monitors both input CLK signals. Upon detection of a failure (CLK stuck HIGH or LOW for at least 1 period), the INP_BAD for that CLK will be latched (H). If that CLK is the primary clock, the IDCS will switch to the good secondary clock and phase/frequency alignment will occur with minimal output phase disturbance. The typical phase bump caused by a failed clock is eliminated. (See Application Information section).

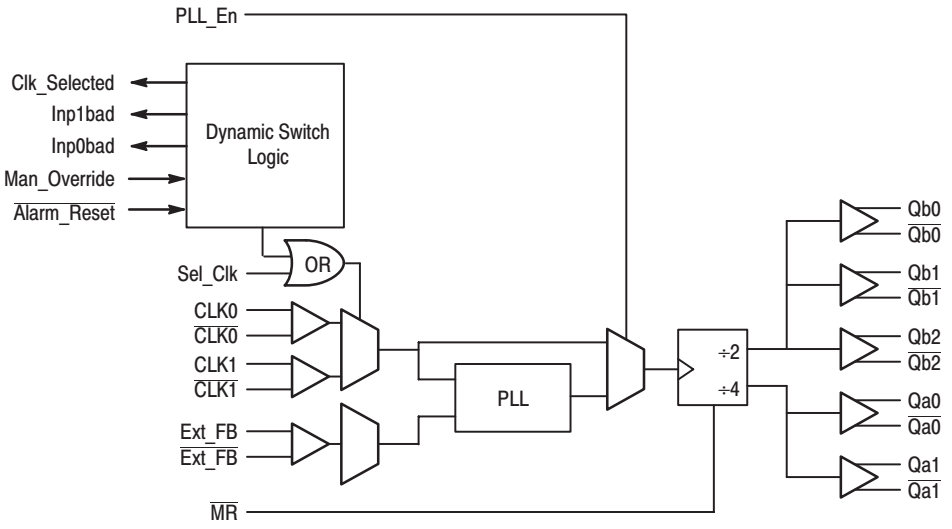



**Figure 1. Block Diagram**

**Rev 3**

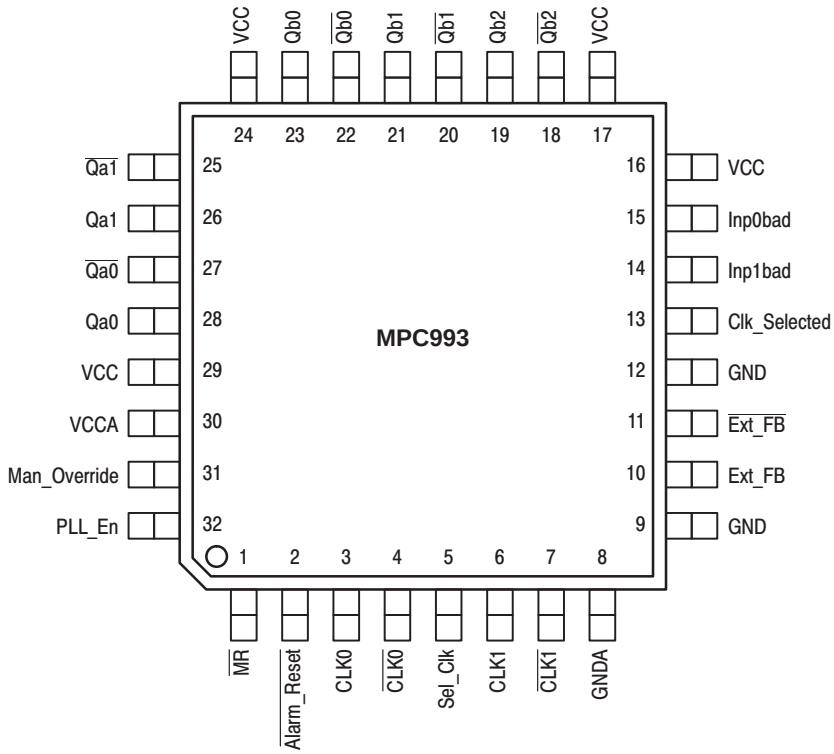



**Figure 2. 32–Lead Pinout** (Top View)

**3.3V PECL DC Characteristics** ($T_A$ = –40°C to 85°C, $V_{CC}$ = 3.3V ± 5%)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage (LVPECL Outputs) ($50\Omega$ to $V_{CC}$ – 2.0V) | $V_{CC}$ – 1.025 | | $V_{CC}$ – 0.80 | V |
| $V_{OL}$ | Output LOW Voltage (LVPECL Outputs) ($50\Omega$ to $V_{CC}$ – 2.0V) | $V_{CC}$ – 1.80 | | $V_{CC}$ – 1.60 | V |
| $V_{PP}$ | Input HIGH Voltage (LVPECL Inputs) | 0.3 | | 1.0 | V |
| $V_{CMR}$ | Input LOW Voltage (LVPECL Inputs) | 1.0 | | $V_{CC}$ – 0.6 | V |
| $V_{OH}$ | Output HIGH Voltage (LVCMOS Outputs) | 2.4 | | | V |
| $V_{OL}$ | Output LOW Voltage (LVCMOS Outputs) | | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage (LVCMOS Inputs) | 2.0 | | 3.3 | V |
| $V_{IL}$ | Input LOW Voltage (LVCMOS Inputs) | | | 0.8 | V |
| $I_{IL}$ | Input LOW Current | 0.5 | | | μA |
| $I_{EE}$ | Power Supply Current GNDA<br>GND | | 15<br>80 | 20<br>180 | mA |

**3.3V PECL AC Characteristics** ($T_A$ = –40°C to 85°C, $V_{CC}$ = 3.3V ± 5%) (Note 6.)

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{VCO}$ | PLL VCO Lock Range | (Note 5.) | 200 | | 360 | MHz |
| $t_{pwi}$ | | | 25 | | 75 | % |
| $t_{pd}$ | Propagation Delay (Note 1.) | CLKn to Q (Bypass)<br>CLKn to Ext_FB (Locked (Note 2.)) | 1.7<br>–150 | 2.3<br>0 | 2.8<br>170 | ns<br>ps |
| $t_r/t_f$ | Output Rise/Fall Time | | 200 | | 800 | ps |
| $t_{skew}$ | Output Skew | Within Bank<br>All Outputs | | | 70<br>100 | ps |
| $\Delta_{pe}$ | Maximum Phase Error Deviation | | | | TBD (Note 3.)<br>TBD (Note 4.) | ps |
| $\Delta_{per/cycle}$ | Rate of Change of Periods | 75MHz Output (Note 1., 3.)<br>150MHz Output (Note 1., 3.)<br>75MHz Output (Note 1., 4.)<br>150MHz Output (Note 1., 4.) | | 20<br>10<br>200<br>100 | 50<br>25<br>400<br>200 | ps/<br>cycle |
| $t_{pw}$ | Output Duty Cycle | | 45 | | 55 | % |
| $t_{jitter}$ | Cycle–to–Cycle Jitter, Standard Deviation (RMS) | (Note 1.) | | | 20 | ps |
| $t_{lock}$ | Maximum PLL Lock Time | | | | 10 | ms |

1. Guaranteed, not production tested.
2. Static phase offset between the selected reference clock and the feedback signal.
3. Specification holds for a clock switch between two signals no greater than 400ps out of phase. Delta period change per cycle is averaged over the clock switch excursion. (See Applications Information section on page 273 for more detail)
4. Specification holds for a clock switch between two signals no greater than ±π out of phase. Delta period change per cycle is averaged over the clock switch excursion.
5. The PLL will be unstable using a ÷2 output as the feedback. Either one of the ÷4 outputs (Qa0 or Qa1) should be used as the feedback signal.
6. PECL output termination is 50 ohms to $V_{CC}$ – 2.0V.

**PIN DESCRIPTIONS**

| Pin Name | I/O | Pin Definition |
|---|---|---|
| CLK0, $\overline{\text{CLK0}}$<br>CLK1, $\overline{\text{CLK1}}$ | LVPECL Input<br>LVPECL Input | Differential PLL clock reference (CLK0 pulldown, $\overline{\text{CLK0}}$ pullup)<br>Differential PLL clock reference (CLK1 pulldown, $\overline{\text{CLK1}}$ pullup) |
| Ext_FB, $\overline{\text{Ext\_FB}}$ | LVPECL Input | Differential PLL feedback clock (Ext_FB pulldown, $\overline{\text{Ext\_FB}}$ pullup) |
| Qa0:1, $\overline{\text{Qa0:1}}$ | LVPECL Output | Differential 1x output pairs |
| Qb0:2, $\overline{\text{Qb0:2}}$ | LVPECL Output | Differential 2x output pairs |
| Inp0bad | LVCMOS Output | Indicates detection of a bad input reference clock 0 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted |
| Inp1bad | LVCMOS Output | Indicates detection of a bad input reference clock 1 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted |
| Clk_Selected | LVCMOS Output | ‘0’ if clock 0 is selected, ‘1’ if clock 1 is selected |
| $\overline{\text{Alarm\_Reset}}$ | LVCMOS Input | ‘0’ will reset the input bad flags and align Clk_Selected with Sel_Clk. The input is “one–shotted” (50kΩ pullup) |
| Sel_Clk | LVCMOS Input | ‘0’ selects CLK0, ‘1’ selects CLK1 (50kΩ pulldown) |
| Manual_Override | LVCMOS Input | ‘1’ disables internal clock switch circuitry (50kΩ pulldown) |
| PLL_En | LVCMOS Input | ‘0’ bypasses selected input reference around the phase–locked loop (50kΩ pullup) |
| $\overline{\text{MR}}$ | LVCMOS Input | ‘0’ resets the internal dividers forcing Q outputs LOW. Asynchronous to the clock (50kΩ pullup) |
| VCCA | Power Supply | PLL power supply |
| VCC | Power Supply | Digital power supply |
| GNDA | Power Supply | PLL ground |
| GND | Power Supply | Digital ground |

# Applications Information

The MPC993 is a dual clock PLL with on–chip Intelligent Dynamic Clock Switch (IDCS) circuitry.

### Definitions

**primary clock:** The input CLK selected by Sel_Clk.
**secondary clock:** The input CLK NOT selected by Sel_Clk.
**PLL reference signal:** The CLK selected as the PLL reference signal by Sel_Clk or IDCS. (IDCS can override Sel_Clk).

### Status Functions

**Clk_Selected:** Clk_Selected (L) indicates CLK0 is selected as the PLL reference signal. Clk_Selected (H) indicates CLK1 is selected as the PLL reference signal.
**INP_BAD:** Latched (H) when it's CLK is stuck (H) or (L) for at least one Ext_FB period (Pos to Pos or Neg to Neg). Cleared (L) on assertion of $\overline{\text{Alarm\_Reset}}$.

### Control Functions

**Sel_Clk:** Sel_Clk (L) selects CLK0 as the primary clock. Sel_Clk (H) selects CLK1 as the primary clock.
**$\overline{\text{Alarm\_Reset}}$:** Asserted by a negative edge. Generates a one–shot reset pulse that clears INPUT_BAD latches and Clk_Selected latch.
**PLL_En:** While (L), the PLL reference signal is substituted for the VCO output.
**$\overline{\text{MR}}$:** While (L), internal dividers are held in reset which holds all Q outputs LOW.

### Man Override (H)

(IDCS is disabled, PLL functions normally). PLL reference signal (as indicated by Clk_Selected) will always be the CLK selected by Sel_Clk. The status function INP_BAD is active in Man Override (H) and (L).

### Man Override (L)

(IDCS is enabled, PLL functions enhanced). The first CLK to fail will latch it's INP_BAD (H) status flag and select the other input as the Clk_Selected for the PLL reference clock. Once latched, the Clk_Selected and INP_BAD remain latched until assertion of $\overline{\text{Alarm\_Reset}}$ which clears all latches (INP_BADs are cleared and Clk_Selected = Sel_Clk). NOTE: If both CLKs are bad when $\overline{\text{Alarm\_Reset}}$ is asserted, both INP_BADs will be latched (H) after one Ext_FB period and Clk_Selected will be latched (L) indicating CLK0 is the PLL reference signal. While neither INP_BAD is latched (H), the Clk_Selected can be freely changed with Sel_Clk. Whenever a CLK switch occurs, (manually or by IDCS), following the next negative edge of the newly selected PLL reference signal, the next positive edge pair of Ext_FB and the newly selected PLL reference signal will slew to alignment.

To calculate the overall uncertainty between the input CLKs and the outputs from multiple MPC993's, the following procedure should be used. Assuming that the input CLKs to all MPC993's are exactly in phase, the total uncertainty will be the sum of the static phase offset, max I/O jitter, and output to output skew.

During a dynamic switch, the output phase between two devices may be increased for a short period of time. If the two input CLKs are 400ps out of phase, a dynamic switch of an MPC993 will result in an instantaneous phase change of 400ps to the PLL reference signal without a corresponding change in the output phase (due to the limited response of the PLL). As a result, the I/O phase of a device, undergoing this switch, will initially be 400ps and diminish as the PLL slews to its new phase alignment. This transient timing issue should be considered when analyzing the overall skew budget of a system.

### Hot insertion and withdrawal

In PECL applications, a powered up driver will experience a low impedance path through an MPC993 input to its powered down VCC pins. In this case, a 100 ohm series resistance should be used in front of the input pins to limit the driver current. The resistor will have minimal impact on the rise and fall times of the input signals.

### Acquiring Frequency Lock

1. While the MPC993 is receiving a valid CLK signal, assert Man_Override HIGH.
2. The PLL will phase and frequency lock within the specified lock time.
3. Apply a HIGH to LOW transition to Alarm_Reset to reset Input Bad flags.
4. De–assert Man_Override LOW to enable Intelligent Dynamic Clock Switch mode.

# Low Voltage PLL Clock Driver

**MPC9952**

**See Upgrade Product – MPC9352**

**LOW VOLTAGE PLL CLOCK DRIVER**

**FA SUFFIX**
LQFP PACKAGE
CASE 873A-02

2

The MPC9952 is a 3.3V compatible, PLL based clock driver device targeted for high performance clock tree applications. The device features a fully integrated PLL with no external components required. With output frequencies of up to 180MHz and eleven low skew outputs the MPC9952 is well suited for high performance designs. The device employs a fully differential PLL design to optimize jitter and noise rejection performance. Jitter is an increasingly important parameter as more microprocessors and ASiC's are employing on chip PLL clock distribution.

- Fully Integrated PLL
- Output Frequency up to 180MHz
- High Impedance Disabled Outputs
- Compatible with **PowerPC**™, Intel and High Performance RISC Microprocessors
- Output Frequency Configurable
- LQFP Packaging
- ±100ps Cycle–to–Cycle Jitter

The MPC9952 features three banks of individually configurable outputs. The banks contain 5 outputs, 4 outputs and 2 outputs. The internal divide circuitry allows for output frequency ratios of 1:1, 2:1, 3:1 and 3:2:1. The output frequency relationship is controlled by the fsel frequency control pins. The fsel pins as well as the other inputs are LVCMOS/LVTTL compatible inputs.

The MPC9952 uses external feedback to the PLL. This features allows for the use of the device as a "zero delay" buffer. Any of the eleven outputs can be used as the feedback to the PLL. The VCO_Sel pin allows for the choice of two VCO ranges to optimize PLL stability and jitter performance. The MR/$\overline{OE}$ pin allows the user to force the outputs into high impedance for board level test.

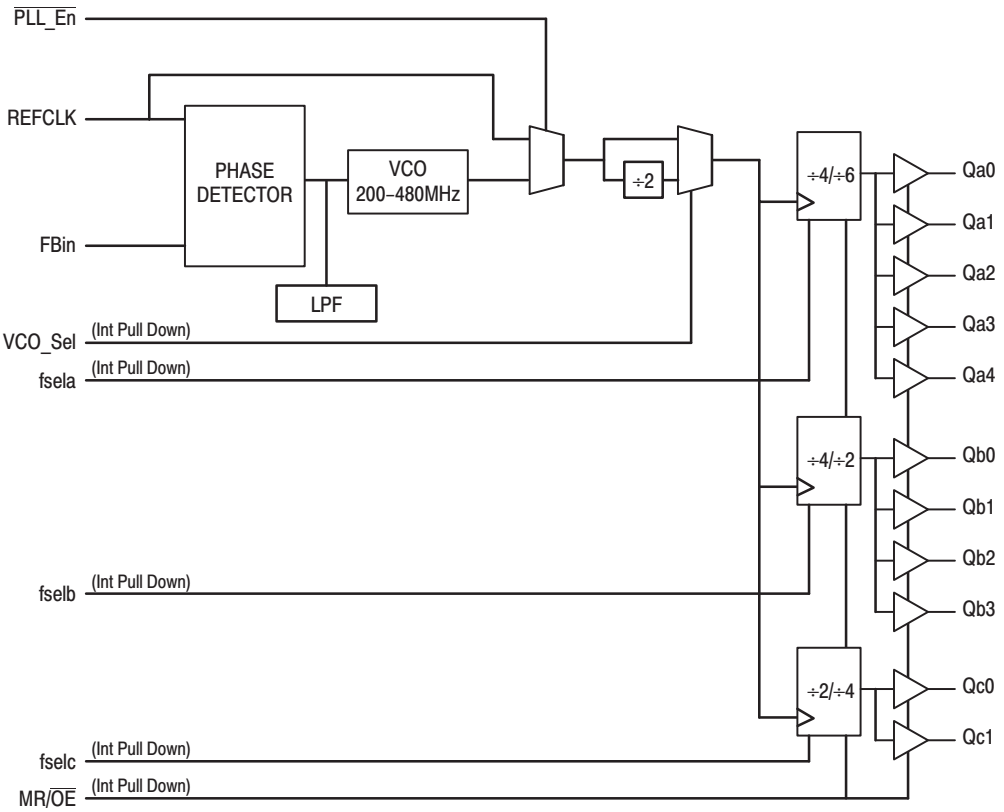
For system debug the PLL of the MPC9952 can be bypassed. When forced to a logic HIGH, the PLLEN input will route the signal on the RefClk input around the PLL directly to the internal dividers. Because the signal is routed through the dividers, it may take several transitions of the RefClk to affect a transition on the outputs. This features allows a designer to single step the design for debug purposes.

The outputs of the MPC9952 are LVCMOS outputs. The outputs are optimally designed to drive terminated transmission lines. For applications using series terminated transmission lines each MPC9952 output can drive two lines. This capability provides an effective fanout of 22, more than enough clocks for most clock tree designs. For more information on driving transmission lines consult the applications section of this data sheet.



**Rev 2**

**Figure 1. MPC9952 Logic Diagram**



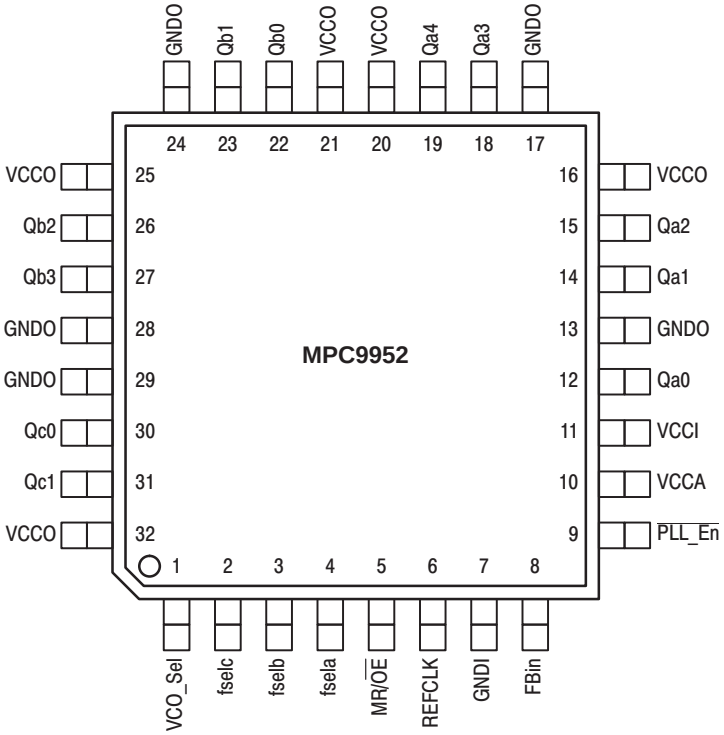




**Figure 2. 32–Lead Pinout** (Top View)

**FUNCTION TABLES**

| fsela | Qan | fselb | Qbn | fselc | Qcn |
|---|---|---|---|---|---|
| 0 | ÷4 | 0 | ÷4 | 0 | ÷2 |
| 1 | ÷6 | 1 | ÷2 | 1 | ÷4 |

| Control Pin | Logic ‘0’ | Logic ‘1’ |
|---|---|---|
| VCO_Sel | fVCO | fVCO/2 |
| MR/$\overline{OE}$ | Output Enable | High Z |
| $\overline{PLL\_En}$ | Enable PLL | Disable PLL |

| Pin Name | Description |
|---|---|
| VCCA | PLL Power Supply |
| VCCO | Output Buffer Power Supply |
| VCCI | Internal Core Logic Power Supply |
| GNDI | Internal Ground |
| GNDO | Output Buffer Ground |

**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 4.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | Input Current | | ±20 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

2

**THERMAL CHARACTERISTICS**

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CCO}$ = $V_{CCI}$ = $V_{CCA}$ = 3.3V ± 5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | 3.6 | V | |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | $I_{OH}$ = –20mA (Note 1.) |
| $V_{OL}$ | Output LOW Voltage | | | 0.5 | V | $I_{OL}$ = 20mA (Note 1.) |
| $I_{IN}$ | Input Current | | | ±120 | µA | Note 2. |
| $C_{IN}$ | Input Capacitance | | 2.7 | 4.0 | pF | |
| $C_{pd}$ | Power Dissipation Capacitance | | 25 | | pF | |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | 160 | mA | Total ICC Static Current |
| $I_{CCA}$ | PLL Supply Current | | 15 | 20 | mA | |

1. The MPC9952 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CCO}$/2) transmission lines on the incident edge (see Applications Info section).
2. Inputs have pull–up, pull–down resistors which affect input current.

**PLL INPUT REFERENCE CHARACTERISTICS** ($T_A$ = 0 to 70°C)

| Symbol | Characteristic | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $t_r$, $t_f$ | TCLK Input Rise/Falls | | 3.0 | ns | |
| $f_{ref}$ | Reference Input Frequency | | 100 | MHz | Note 3. |
| $f_{refDC}$ | Reference Input Duty Cycle | 25 | 75 | % | |

3. Maximum and minimum input reference is limited by the VCO lock range and the feedback divider.

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $t_r$, $t_f$ | Output Rise/Fall Time (Note 4.) | 0.10 | | 1.0 | ns | 0.8 to 2.0V |
| $t_{pw}$ | Output Pulse Width (Note 4.) | $t_{CYCLE}/2$ –750 | $t_{CYCLE}/2$ ±500 | $t_{CYCLE}/2$ +750 | ps | |
| $t_{os}$ | Output-to-Output Skew (Note 4.) Excluding Qa0<br>All Outputs<br>All Outputs | | | 350<br>450<br>550 | ps | Same Frequencies<br>Same Frequencies<br>Different Frequencies |
| $f_{VCO}$ | PLL VCO Lock Range | 200 | | 480 | MHz | Note 6. |
| $f_{max}$ | Maximum Output Frequency Qc,Qb (÷2)<br>Qa,Qb,Qc (÷4)<br>Qa (÷6) | 180<br>120<br>80 | | | MHz | Note 4. |
| $t_{pd}$ | REFCLK to FBIN Delay | –200 | 0 | 200 | ps | Notes 4., 5. |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time | 2 | | 8 | ns | Note 4. |
| $t_{PZL}$, $t_{PLH}$ | Output Enable Time | 2 | | 10 | ns | Note 4. |
| $t_{jit(cc)}$ | Cycle–to–Cycle Jitter | | ±100 | | ps | |
| $t_{lock}$ | Maximum PLL Lock Time | | | 10 | ms | |

4. Termination of 50Ω to $V_{CCO}$/2.
5. $t_{pd}$ is specified for 50MHz input ref, the window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The $t_{pd}$ does not include jitter.
6. The PLL may be unstable with a divide by 2 feedback ratio.

## APPLICATIONS INFORMATION

### Driving Transmission Lines

The MPC9952 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 7Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091.

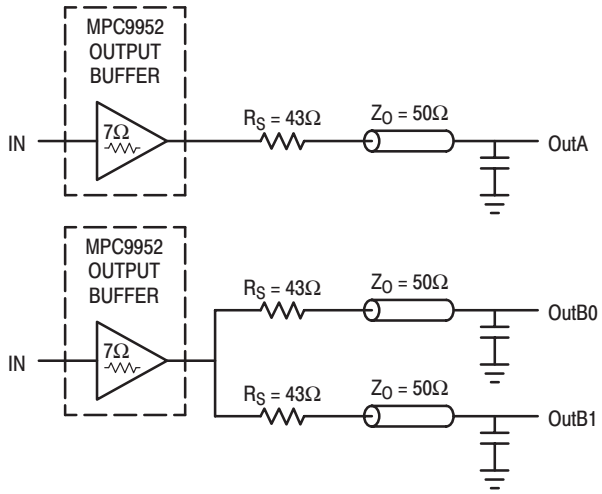



**Figure 3. Single versus Dual Transmission Lines**

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CCO}$/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9952 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9952 clock driver is effectively doubled due to its capability to drive multiple lines.

The waveform plots of Figure 4 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC9952 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC9952. The output waveform in Figure 4 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS (Zo / Rs + Ro + Zo) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

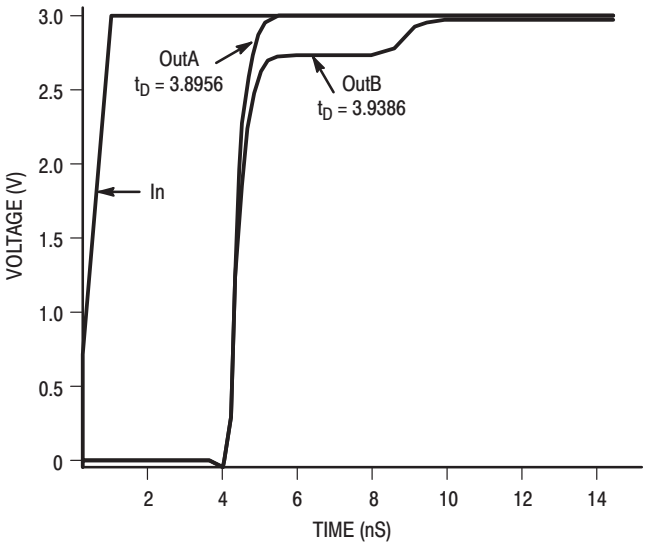
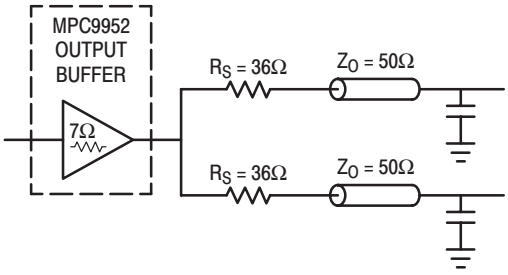



**Figure 4. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




$7\Omega + 36\Omega \parallel 36\Omega = 50\Omega \parallel 50\Omega$
$25\Omega = 25\Omega$

**Figure 5. Optimized Dual Line Termination**

**Power Supply Filtering**

The MPC9952 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC9952 provides separate power supplies for the output buffers ($V_{CCO}$) and the internal PLL (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC9952.

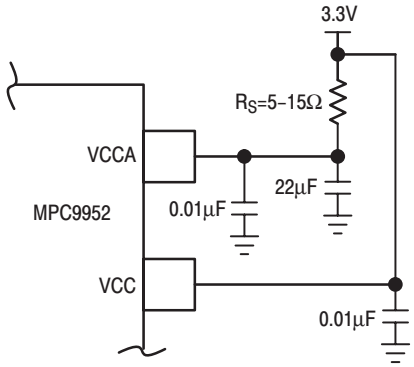



**Figure 6. Power Supply Filter**

Figure 6 illustrates a typical power supply filter scheme. The MPC9952 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the VCCA pin of the MPC9952. From the data sheet the $I_{VCCA}$ current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.3V – 5% must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V $V_{CC}$ supply is used. The resistor shown in Figure 6 must have a resistance of 5–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

Although the MPC9952 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

*Product Preview*

# Low Voltage PLL Clock Driver

**MPC9990**

**LOW VOLTAGE DIFFERENTIAL PECL–HSTL PLL CLOCK DRIVER**

**FA SUFFIX**
48–LEAD LQFP PACKAGE
CASE 932–03

2

The MPC9990 is a low voltage PLL clock driver designed for high speed clock generation and distribution in high performance computer, workstation and server applications. The clock driver accepts a LVPECL compatible clock signal and provides 10 low skew, differential HSTL[1] compatible outputs, one HSTL compatible output for system synchronization purposes and one HSTL compatible PLL feedback output. The device operates from a dual voltage supply: 3.3V for the core logic and 1.8V for the HSTL outputs. The fully integrated PLL supports an input frequency range of 75 to 300 MHz. The output frequencies are configurable.

- Supports high performance HSTL clock distribution systems
- Compatible to IA64 processor systems
- Fully Integrated PLL, differential design
- Core logic operates from 3.3V power supply
- HSTL outputs operate from a 1.8V supply
- Programmable frequency by output bank
- 10 HSTL compatible outputs (two banks)
- HSTL compatible PLL feedback output
- HSTL compatible sychronization output (QSYNC)
- Max. skew of 50 ps within outbank
- Zero–delay capability: max. SPO (tpd) window of ± 75 ps
- LVPECL compatible clock input, LVCMOS compatible control inputs
- Temperature range of 0 to +70°C

The MPC9990 provides output clock frequencies required for high–performance computer system optimization. The device drives up to 10 differential clock loads within the frequency range of 75 to 300 MHz. The 10 outputs are organized in 2 banks of 3 and 7 differential outputs. In the standard configuration the QFB output pair is connected to the FB input pair closing the PLL loop and enabling zero delay operation from the CLK input to the outputs. Bank B outputs are frequency and phase aligned to the CLK input, providing exact copies of the high–speed input signal. Bank A outputs are configured to operate at slower speeds driving the system bus devices. The output frequency ratio of bank A to bank B is adjustable (for available ratios, see “MPC9990 Application: CPU to System Bus Frequency Ratios” on page 280) for system optimization. In a computer application, bank B outputs generate the clock signals for the devices operating at the CPU frequency, while Bank A outputs are configured to drive the clock signals for the devices running at lower speeds (system clock). Four individual frequency ratios are available, providing a high degree of flexibility. The frequency ratios between CPU clock and system clock provided by the MPC9990 are listed in the table “Output configuration” on page 282.

The QSYNC output functionality is designed for system synchronization purpose. QSYNC is asserted at coincident rising edges of CPU (bank B and QFB signal) and slower system clock (bank A) outputs (see “QSYNC Phase Relation Diagram” on page 282), providing baseline timing in systems with fractional clocks. The QSYNC output is asserted for one QFB high pulse, centered on the rising QFB output.

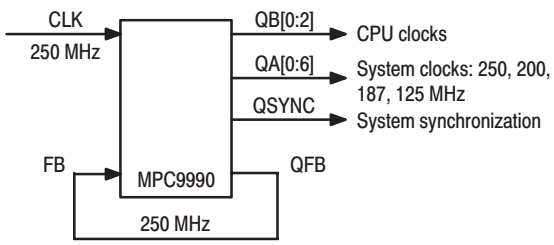



**Figure 1. MPC9990 Application Example**

1. In order to minimize output–to–output skew, HSTL outputs of the MPC9990 are generated with an open emitter architecture. For output termination, see ”HSTL Output Termination and AC Test Reference” on page 284.



**Rev 3**

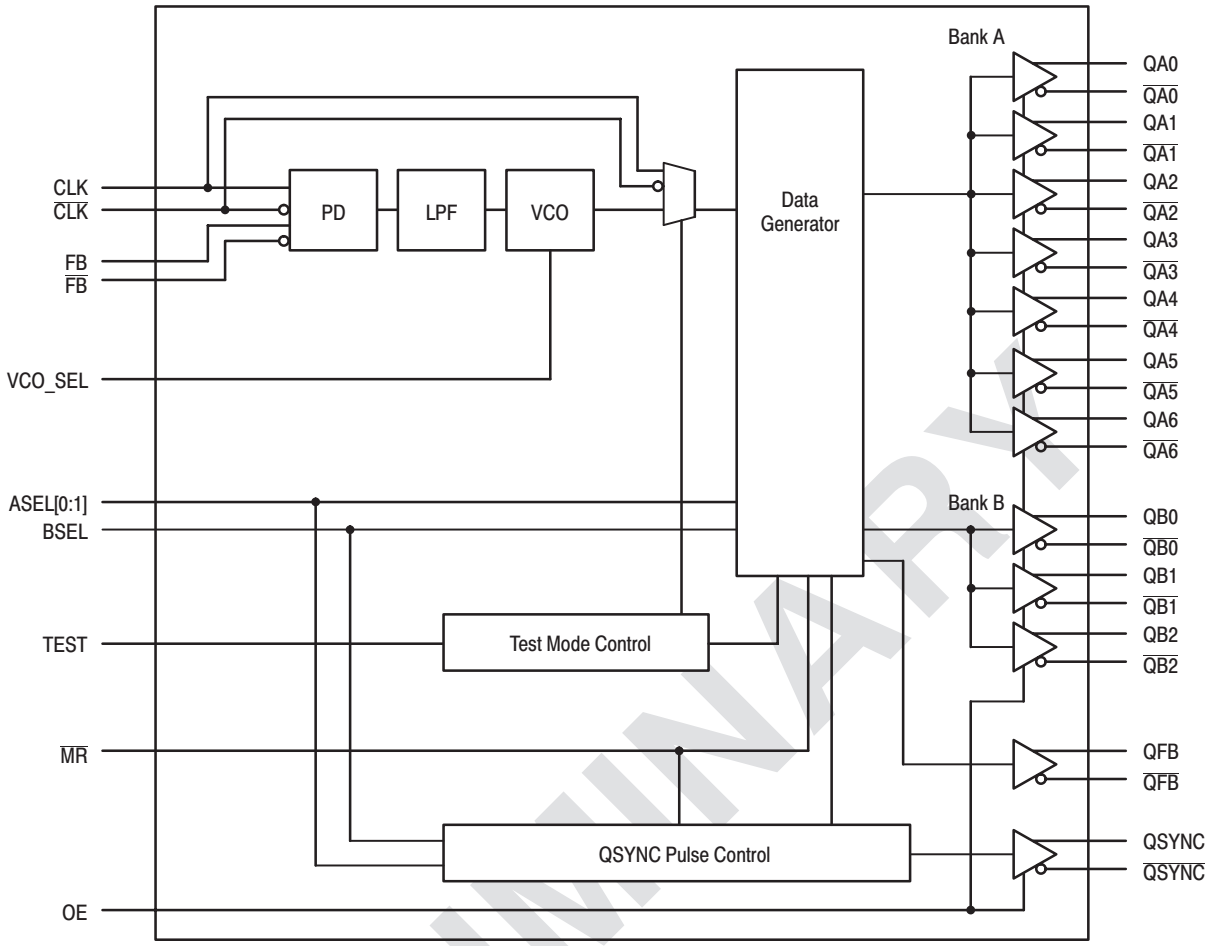



**Figure 2. MPC9990 Logic Diagram**

**Table 1: MPC9990 Application: CPU to System Bus Frequency Ratios**

| QA to QB frequency ratio | 1:1 | 1:2 | 3:4 | 4:5 | |
|---|---|---|---|---|---|
| Output frequencies for CLK = 75 MHz (BSEL=1, VCO_SEL=1) | | | | | |
| QA output frequency | 75 | 37.5 | 56.25 | 60 | MHz |
| QB output frequency | 75 | 75 | 75 | 75 | MHz |
| Output frequencies for CLK = 100 MHz (BSEL=1, VCO_SEL=1) | | | | | |
| QA output frequency | 100 | 50 | 75 | 80 | MHz |
| QB output frequency | 100 | 100 | 100 | 100 | MHz |
| Output frequencies for CLK = 125 MHz (BSEL=1, VCO_SEL=1) | | | | | |
| QA output frequency | 125 | 62.5 | 93.75 | 100 | MHz |
| QB output frequency | 125 | 125 | 125 | 125 | MHz |
| Output frequencies for CLK = 150 MHz (BSEL=1, VCO_SEL=1) | | | | | |
| QA output frequency | 150 | 75 | 112.5 | 120 | MHz |
| QB output frequency | 150 | 150 | 150 | 150 | MHz |
| Output frequencies for CLK = 200 MHz (BSEL=1, VCO_SEL=0) | | | | | |
| QA output frequency | 200 | 100 | 150 | 160 | MHz |
| QB output frequency | 200 | 200 | 200 | 200 | MHz |
| Output frequencies for CLK = 250 MHz (BSEL=1 VCO_SEL=0) | | | | | |
| QA output frequency | 250 | 125 | 187.5 | 200 | MHz |
| QB output frequency | 250 | 250 | 250 | 250 | MHz |
| Output frequencies for CLK = 300 MHz (BSEL=1 VCO_SEL=0) | | | | | |
| QA output frequency | 300 | 150 | 225 | 240 | MHz |
| QB output frequency | 300 | 300 | 300 | 300 | MHz |

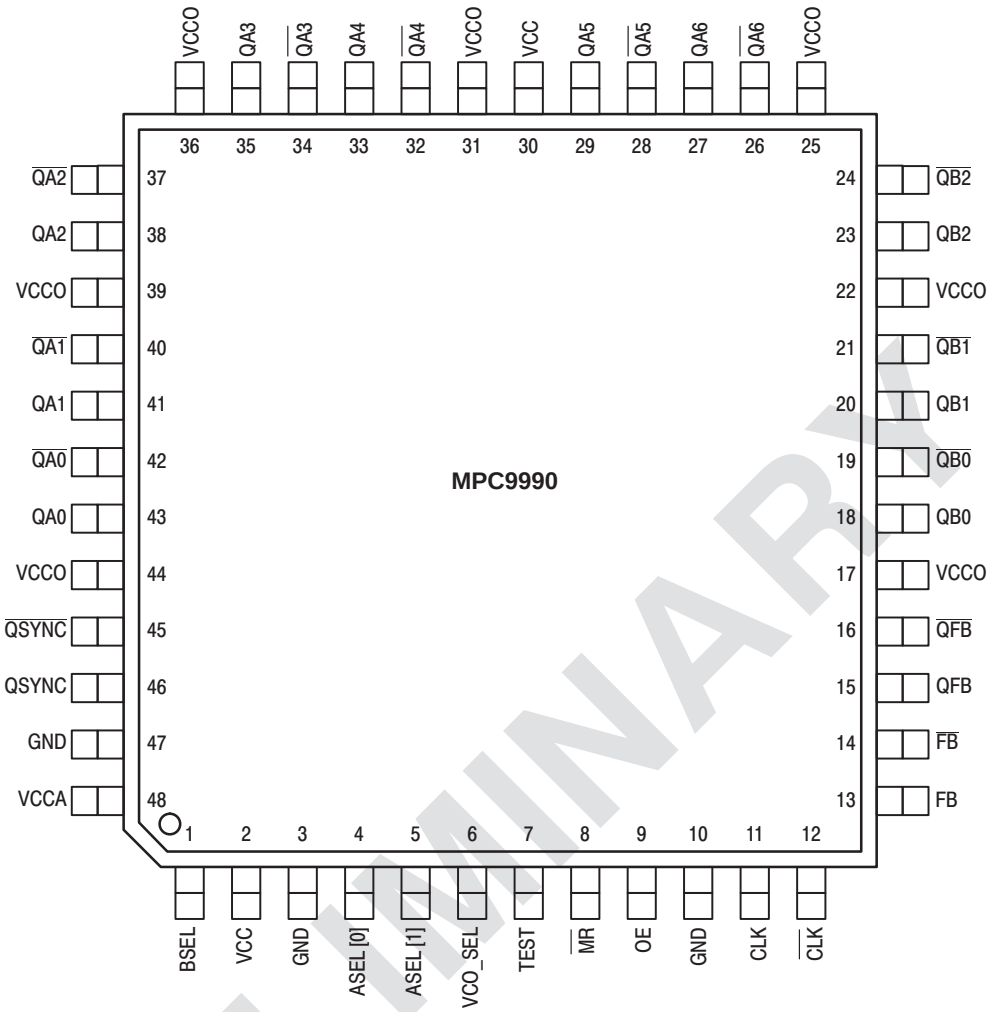



**Figure 3. 48–Lead Package Pinout** (Top View)

**Table 2: Pin configuration**

| Pin | I/O | Type | Internal resistor | Description |
|---|---|---|---|---|
| CLK, $\overline{CLK}$ | Input | LVPECL | CLK: pull-down, $\overline{CLK}$: pull-up | Differential clock frequency input |
| FB, $\overline{FB}$ | Input | HSTLL | FB: pull-down, $\overline{FB}$: pull-up | Differential feedback input |
| QAn, $\overline{QAn}$ | Output | HSTL | | Bank A outputs |
| QBn, $\overline{QBn}$ | Output | HSTL | | Bank B outputs |
| QSYNC, $\overline{QSYNC}$ | Output | HSTL | | Synchronization output |
| QFB, $\overline{QFB}$ | Output | HSTL | | Differential feedback output |
| VCO_SEL | Input | LVCMOS | pull-down | Selection of operating frequency range |
| ASEL[0:1] | Input | LVCMOS | pull-down | Selection of bank A output frequency |
| BSEL | Input | LVCMOS | pull-down | Selection of bank B output frequency |
| TEST | Input | LVCMOS | pull-down | Selection of PLL operation or TEST mode (PLL bypass) |
| $\overline{MR}$ | Input | LVCMOS | pull-up | Master reset. Assertion of master reset required on startup |
| OE | Input | LVCMOS | pull-up | Output enable |
| $V_{CCA}$ | | Power supply | | Analog power supply, typical 3.3V |
| $V_{CC}$ | | Power supply | | Core power supply, typical 3.3V |
| $V_{CCO}$ | | Power supply | | Output power supply, typical 1.8V |
| GND | | Ground | | Output, analog and core logic ground, 0V (VEE) |

**Table 3: Output Frequency Relationship for an Example Configuration**

| ASEL[0] | ASEL[1] | BSEL | f QAn | f QBn | f QFB | QSYNC |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | CLK | CLK | CLK | L |
| 0 | 1 | 0 | CLK ÷ 2 | CLK ÷ 2 | CLK | enabled |
| 1 | 0 | 0 | CLK x 3 ÷ 4 | CLK x 3 ÷ 4 | CLK | enabled |
| 1 | 1 | 0 | CLK x 4 ÷ 5 | CLK x 4 ÷ 5 | CLK | enabled |
| 0 | 0 | 1 | CLK | CLK | CLK | L |
| 0 | 1 | 1 | CLK ÷ 2 | CLK | CLK | enabled |
| 1 | 0 | 1 | CLK x 3 ÷ 4 | CLK | CLK | enabled |
| 1 | 1 | 1 | CLK x 4 ÷ 5 | CLK | CLK | enabled |



**Table 4: Function Table (Controls)**

| Control Pin | 0 | 1 |
|---|---|---|
| TEST | PLL enabled | PLL bypassed (Static test mode) |
| $\overline{MR}$ | Reset (Internal logic and PLL) | Normal operation mode |
| OE | Outputs disabled ($Q_X$ = L, $\overline{Q}_X$ = H), except QFB, $\overline{QFB}$ | Outputs enabled |
| VCO_SEL | High frequency operation (VCO frequency range from 600 to 1200 MHz) | Low frequency operation (VCO frequency range from 300 to 600 MHz) |

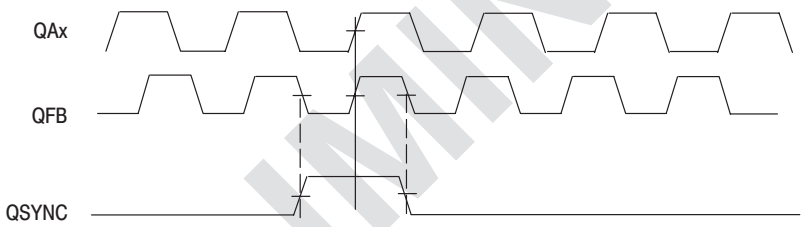



**Figure 4. QSYNC Phase Relation Diagram**

The MPC9990 has a system synchronization pulse output (QSYNC). The QSYNC pulse output is synchronous to the feedback clock signal (QFB) and activated when both QFB and bank A outputs are programmed to run at a frequency ratio other than 1:1. In the case of a 1:1 frequency ratio (ASEL[] = 00), QSYNC remains low. QSYNC output transitions occur prior coincident rising edges of QFB and bank A. The pulse width of the QSYNC pulse is equal to the period of the feedback clock frequency (QFB). The QSYNC pulse is asserted at the last falling edge of QFB prior to the coincident edge event, and deasserted at the next falling edge of QFB (see “QSYNC Phase Relation Diagram”). If BSEL = 1 and the PLL is frequency and phase-locked, QSYNC pulses occur on coincident edges between the QA-bank and QB-bank outputs (offset by feedback delay) due to the fixed phase relation between CLK, QFB and QB-bank outputs.

**Table 5: ABSOLUTE MAXIMUM RATINGS***

| Symbol | Characteristics | Min | Max | Units | Condition |
|---|---|---|---|---|---|
| $V_{CCA}$ | Analog power supply | –0.5 | 3.6 | V | |
| $V_{CC}$ | Core power supply | –0.5 | 3.6 | V | |
| $V_{CCO}$ | Output power supply | –0.5 | 3.6 | V | |
| $V_{IN}$ | Input voltage | –0.5 | $V_{CC}$ + 0.3 | V | |
| $I_{IN}$ | Input current | –1.0 | 1.0 | mA | DC |
| $I_{OUT}$ | Output current | –50 | 50 | mA | DC |
| $T_S$ | Storage temperature | –50 | 150 | °C | |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute–maximum–rated conditions is not implied.

**Table 6: DC CHARACTERISTICS** ($V_{CC}$ = $V_{CCA}$ = 3.3V ±5%, $V_{CCO}$ = 1.7 to 2.1V, $T_A$ = 0° to 70°C)

| Symbol | Characteristics | 0 °C | | | 25 °C | | | 70 °C | | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| HSTL I/O[a] | | | | | | | | | | | | |
| $V_{CCO}$ | Output power supply | 1.7 | 1.8 | 2.1 | 1.7 | 1.8 | 2.1 | 1.7 | 1.8 | 2.1 | | |
| $V_{IN}$ | Input voltage | -0.3 | | 1.45 | -0.3 | | 1.45 | -0.3 | | 1.45 | V | Differential |
| $V_{DIF}$ | Differential input voltage[b] | 0.2 | | 1.75 | 0.2 | | 1.75 | 0.2 | | 1.75 | V | Differential |
| $V_{CM}$ | Common mode input voltage[c] | 0.68 | | 0.9 | 0.68 | | 0.9 | 0.68 | | 0.9 | V | |
| $V_{OH}$ | Output high voltage | 1.0 | $V_X$+0.4 | 1.4 | 1.0 | $V_X$+0.4 | 1.4 | 1.0 | $V_X$+0.4 | 1.4 | V | |
| $V_{OL}$ | Output low voltage | 0 | $V_X$-0.4 | 0.4 | 0 | $V_X$-0.4 | 0.4 | 0 | $V_X$-0.4 | 0.4 | V | |
| LVPECL I/O | | | | | | | | | | | | |
| $V_{CC}$ | Power supply voltage (core) | 3.135 | 3.3 | 3.465 | 3.135 | 3.3 | 3.465 | 3.135 | 3.3 | 3.465 | V | |
| $V_{CCA}$ | Power supply voltage (PLL) | 3.135 | 3.3 | 3.465 | 3.135 | 3.3 | 3.465 | 3.135 | 3.3 | 3.465 | V | |
| $V_{PP}$ | Peak-to-peak input voltage[d] CLK, $\overline{PCLK}$ | 500 | | 1000 | 500 | | 1000 | 500 | | 1000 | mV | |
| $V_{CMR}$ | Common Mode Range[e f] CLK, $\overline{PCLK}$ | $V_{CC}$-1.4 | | $V_{CC}$-0.6 | $V_{CC}$-1.4 | | $V_{CC}$-0.6 | $V_{CC}$-1.4 | | $V_{CC}$-0.6 | V | |
| $V_{IH}$ | Input high voltage[g] | 2.135 | | 2.420 | 2.135 | | 2.420 | 2.135 | | 2.420 | V | $V_{CC}$=3.3V |
| $V_{IL}$ | Input low voltage[e] | 1.490 | | 1.825 | 1.490 | | 1.825 | 1.825 | | 1.825 | V | $V_{CC}$=3.3V |
| $I_{IH}$ | Input high current | | | ±150 | | | ±150 | | | ±150 | µA | |
| $I_{CC}$ | Power supply current (core) | | | TBD | | | TBD | | | TBD | mA | |
| $I_{CCA}$ | Power supply current (PLL) | | 15 | 20 | | 15 | 20 | | 15 | 20 | mA | |
| LVCMOS Inputs | | | | | | | | | | | | |
| $V_{IH}$ | Input high voltage | 2 | | $V_{CC}$ | 2 | | $V_{CC}$ | 2 | | $V_{CC}$ | V | |
| $V_{IL}$ | Input low voltage | 0 | | 0.8 | 0 | | 0.8 | 0 | | 0.8 | V | |
| $I_I$ | Input current | | | ±100 | | | ±100 | | | ±100 | µA | |

a. See “HSTL Differential Input Levels”
b. $V_{DIF}$ specifies the input differential voltage
c. $V_{CM}$ is the maximum allowable range of $V_{TR}$ - (($V_{TR}$ - $V_{CP}$)/2). $V_{TR}$ is true input signal, $V_{CP}$ is its complementary input signal
d. Pending characterization
e. $V_{CMR}$ is the difference from $V_{CC}$ and the crosspoint of the differential input signal. Normal operation is obtained when the “high” input is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ specification.
f. Pending characterization
g. LVPECL input level specifications will vary 1:1 with $V_{CC}$

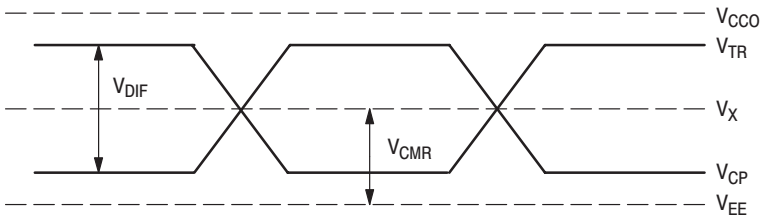



**Figure 5. HSTL Differential Input Levels**

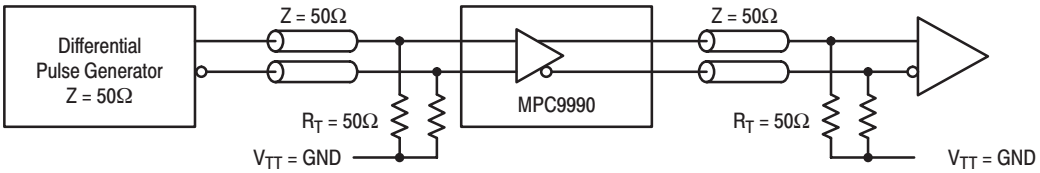



**Figure 6. HSTL Output Termination and AC Test Reference**

**Table 7: AC CHARACTERISTICS** ($V_{CC}$ = $V_{CCA}$ = 3.3V ±5%, $V_{CCO}$ = 1.7 to 2.1V, $T_A$ = 0° to 70°C)a

| Symbol | Characteristics | 0 °C | | | 25 °C | | | 70 °C | | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| $f_{IN}$ | Input frequency for VCO_SEL = 0 (high range) | | | | | | | | | | | |
| | 1:1 ratio, ASEL=00 | 150.0 | | 300.0 | 150.0 | | 300.0 | 150.0 | | 300.0 | MHz | 600 < $f_{VCO}$ |
| | 1:2 ratio, ASEL=01 | 150.0 | | 300.0 | 150.0 | | 300.0 | 150.0 | | 300.0 | MHz | < 1200 |
| | 3:4 ratio, ASEL=10 | 200.0 | | 300.0 | 200.0 | | 300.0 | 300.0 | | 300.0 | MHz | MHz |
| | 4:5 ratio, ASEL=11 | 150.0 | | 300.0 | 150.0 | | 300.0 | 150.0 | | 300.0 | MHz | |
| | Input frequency for VCO_SEL = 1 (low range) | | | | | | | | | | | |
| | 1:1 ratio, ASEL=00 | 75.0 | | 150.0 | 75.0 | | 150.0 | 75.0 | | 150.0 | MHz | |
| | 1:2 ratio, ASEL=01 | 75.0 | | 150.0 | 75.0 | | 150.0 | 75.0 | | 150.0 | MHz | 300 < $f_{VCO}$ |
| | 3:4 ratio, ASEL=10 | 100.0 | | 200.0 | 100.0 | | 200.0 | 100.0 | | 200.0 | MHz | < 600 MHz |
| | 4:5 ratio, ASEL=11 | 75.0 | | 150.0 | 75.0 | | 150.0 | 75.0 | | 150.0 | MHz | |
| $f_{VCO}$ | VCO frequency[b] | | | | | | | | | | | |
| | VCO_SEL = 1 (low range) | 300 | | 600 | 300 | | 600 | 300 | | 600 | MHz | |
| | VCO_SEL = 0 (high range) | 600 | | 1200 | 600 | | 1200 | 600 | | 1200 | MHz | |
| $f_{OUT}$ | Output frequency[c] | | | 300 | | | 300 | | | 300 | MHz | |
| SPO | Static phase offset, $t_{PD}$ between CLK and FB | X-75 | | X+75 | X-75 | | X+75 | X-75 | | X+75 | ps | "X" is TBD |
| DC | Output duty cycle[d] | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | % | |
| $t_{Skew}$ | Differential output skew | | | | | | | | | | | |
| | $t_{SK(OB)}$ within bank | | | 50 | | | 50 | | | | ps | Differential |
| | $t_{SK(O)}$ single frequency | | | 50 | | | 50 | | | | ps | HSTL |
| | $t_{SK(O)}$ multiple frequencies | | | TBD | | | TBD | | | | ps | outputs |
| | $t_{SK(O)}$ QFB to QSYNC | TBD | –100 | TBD | TBD | –100 | TBD | TBD | TBD | TBD | ps | |
| $V_{PP}$[e] | Minimum input swing | 0.5 | | 1 | 0.5 | | 1 | 0.5 | | 1 | V | LVPECL |
| $V_{CMR}$ | Common mode range | 1 | | $V_{CC}$-0.4 | 1 | | $V_{CC}$-0.4 | 1 | | $V_{CC}$-0.4 | V | LVPECL |
| $V_{DIF,OUT}$ | Minimum output swing | 0.6 | 0.8 | | 0.6 | 0.8 | | 0.6 | 0.8 | | V | HSTL |
| $V_X$ | Differential output crosspoint voltage | 0.68 | | 0.9 | 0.68 | | 0.9 | 0.68 | | 0.9 | V | HSTL |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter[f] | | | 75 | | | 75 | | | 75 | ps | |
| $t_{JIT(PER)}$ | Period Jitter | | | TBD | | | TBD | | | TBD | | |
| $t_{JIT(IO)}$ | I/O Phase Jitter RMS (1 σ) | | | 40 | | | 40 | | | 40 | ps | |
| BW | PLL bandwidth | | | | | | | | | | | |
| | 1:1 ratio, ASEL=00 | | | | | | | | | | kHz | |
| | 1:2 ratio, ASEL=01 | | | | | | | | | | kHz | |
| | 3:4 ratio, ASEL=10 | | | | | | | | | | kHz | |
| | 4:5 ratio, ASEL=11 | | | | | | | | | | kHz | |
| $t_r$, $t_f$ | Output transition rate | 0.8 | | 2.6 | 0.8 | | 2.6 | 0.8 | | 2.6 | V/ns | 20%–80% |
| $t_{Lock}$ | PLL lock time | | | 10 | | | 10 | | | 10 | ms | |

a. Refer to "HSTL Output Termination and AC Test Reference" for AC test conditions
b. $f_{VCO}$ specification is pending device characterization
c. $f_{OUT}$ at which output-to-output skew, $V_X$ and DC specification are still met. $f_{OUT}$ is primary a function of $f_{IN}$ and the input-to-output frequency ratio (M:N). Pending characterization.
d. Design target is 48%-52%. DC specification is pending characterization
e. $V_{PP}$ specifies the minimum input differential voltage required for switching
f. Jitter specification is pending device characterization. Maximum number represents design target. Cycle-to-cycle jitter is the period variation between adjacent clock cycles

## APPLICATIONS INFORMATION

### Using the MPC9990 in zero-delay applications

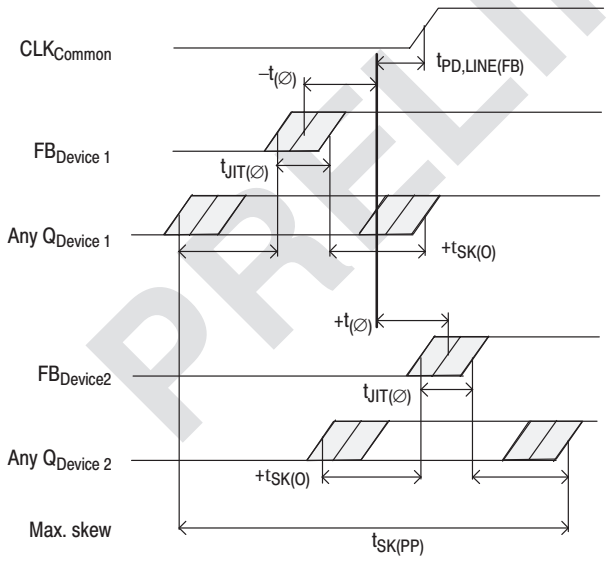
Nested clock trees are typical applications for the MPC9990. Designs using the MPC9990 as PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from static fanout buffers. The external feedback option of the MPC9990 clock driver allows for its use as a zero delay buffer. By using the differential QFB output pair as a feedback to the PLL the propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input (CLK) and any output. This effective delay consists of the static phase offset (SPO), I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

### Calculation of part-to-part skew

The MPC9990 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9990 are connected together, the maximum overall timing uncertainty from the common CLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset (SPO), output skew, feedback board trace delay and I/O (phase) jitter. The output skew ($t_{SK(O)}$) specification of the MPC9990 is different for single or for dual frequency bank configurations. :




Complementary signals are not shown. Signal references level is the differential voltage crosspoint $V_X$

**Figure 7. MPC9990 max. device-to-device skew**

Due to the statistical nature of I/O jitter a rms value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

**Table 8: Confidence Facter CF**

| CF | Probability of clock edge within the distribution |
|---|---|
| ± 1σ | 0.68268948 |
| ± 2σ | 0.95449988 |
| ± 3σ | 0.99730007 |
| ± 4σ | 0.99993663 |
| ± 5σ | 0.99999943 |
| ± 6σ | 0.99999999 |

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) and single frequency configuration is assumed, resulting in a worst case timing uncertainty from input to any output of -245 ps to 245 ps (result pending characterization) relative to CLK.

$$t_{SK(PP)} = [–75ps...75ps] + [–50ps...50ps] + [(40ps\cdot –3)...(40ps\cdot 3)] + t_{PD,\ LINE(FB)} + X$$

$$t_{SK(PP)} = [–245ps...245ps] + t_{PD,\ LINE(FB)} + X$$

On device characterization, final numbers for X (part of static phase offset, $t_{sk(O)}$ and SPO will be determined. Due to the frequency dependence of the I/O jitter, Figure 8 “Max. I/O Jitter versus frequency” can be used for a more precise timing performance analysis. The number for the I/O jitter at a specific frequency can be substituted for the more general datasheet specification number:

**TBD**

**Figure 8. Max. I/O Jitter versus frequency**

**Power Supply Filtering**

The MPC9990 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply. Random noise on the $V_{CCA}$ power supply impacts the device AC characteristics, for instance I/O jitter. The MPC9990 provides separate power supplies for the output buffers ($V_{CCO}$) and the phase-locked loop ($V_{CCA}$) of the device.

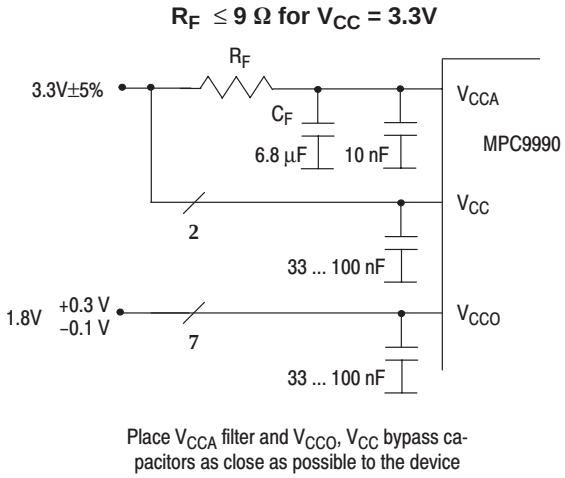



**Figure 9. Recommended Power Supply Filter**

The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is difficult to minimize noise on the power supplies a second level of isolation may be required. A simple but effective form of isolation is a power supply filter on the $V_{CCA}$ pin for the MPC9990. Figure 9 illustrates a recommended power supply low-pass frequency filter scheme. The MPC9990 VCO frequency and phase stability is most susceptible to noise with spectral content in the 300 kHz to 3 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor $R_F$. The maximum voltage drop on $V_{CCA}$ that can be tolerated is 135 mV with respect to $V_{CC}$ = 3.3V ± 5%, resulting in a lowest allowable supply voltage for $V_{CCA}$ equal to 2.835 V.

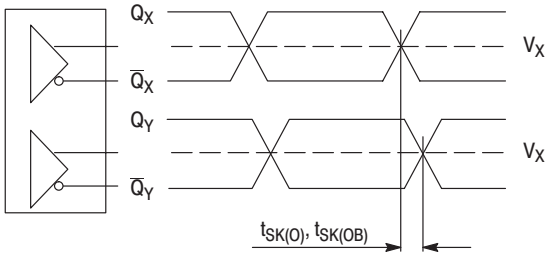
From the data sheet the $I_{CCA}$ current (the current sourced through the $V_{CCA}$ pin) is typically 11 mA (15 mA maximum), assuming that the minimum of 3.0V ($V_{CC}$=3.3V-5%-0.135V) must be maintained on the $V_{CCA}$ pin. The resistor $R_F$ shown in Figure 9 “Recommended Power Supply Filter” should have a maximum resistance of 9 Ω to meet the voltage drop criteria. The minimum resistance for $R_F$ and the filter capacitor $C_F$ are defined by the required filter characteristics: the RC filter should provide an attenuation greater 40 dB for noise whose spectral content is above 300 kHz. In the example RC filter shown in Figure 9 “Recommended Power Supply Filter”, the filter cut-off frequency is 16.3 kHz and the noise attenuation at 300 kHz is approximately 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown (6.8 µF || 10 nF) ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9990 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds, internal voltage regulation and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Recommended Power-up Sequence**

The MPC9990 does not require any special supply ramp sequence in case the system provides all supply voltages (3.3V and 1.8V) at the same time. The reference clock signal (CLK, $\overline{CLK}$) can be applied any time during or after the power up sequence if $V_{IN}$ is smaller or equal $V_{CC}$ during the voltage transition. Following are guidelines for the MPC9990 power-up sequence in case the 3.3V and 1.8V voltage supply cannot be applied at the same time:

- HSTL output supply voltage $V_{CCO}$ must be powered up to the specified voltage range before or at the same time than $V_{CC}$. $V_{CCA}$ can be powered up before, at the same time or after $V_{CC}$ and $V_{CCO}$.
- At the time the power supplies are powered up, the device should be reset ($\overline{MR}$=0).
- Apply the clock input signals to the PLL (CLK, $\overline{CLK}$) after all power supplies are stable. Then, $\overline{MR}$ can be deasserted ($\overline{MR}$=1). This will release the internal PLL which will attempt to lock
- The time from $\overline{MR}$ deassertion to PLL lock will be specified by the PLL lock time $t_{Lock.}$ After the PLL achieved lock, the AC characteristics are valid.
- Outputs can be enabled by OE any time. QFB is not affected by OE and the PLL can achieve lock even if OE is tied high (OE = 1, disable).




The pin–to–pin skew is defined as the worst case difference in propagation delay between any two similar delay path within a single device ($t_{SK(O)}$) or within a single output bank ($t_{SK(OB)}$)

**Figure 10. Output–to–output Skew $t_{SK(O)}$, $t_{SK(OB)}$**

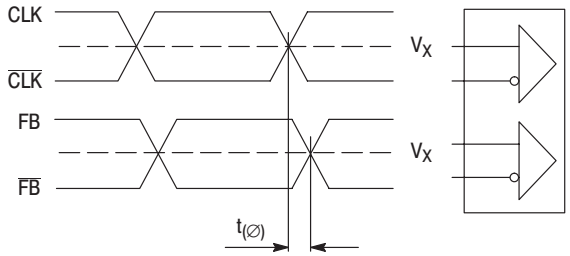
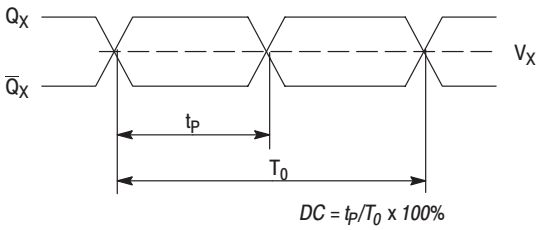
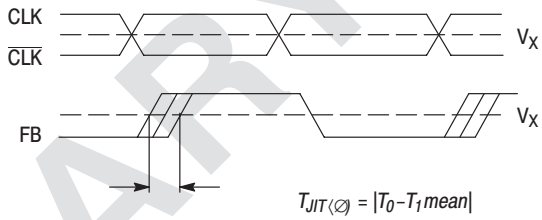



**Figure 11. Propagation delay ($t_{\varnothing}$, static phase offset, SPO) test reference**



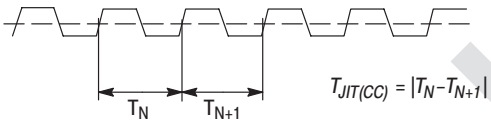

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 12. Output Duty Cycle (DC)**



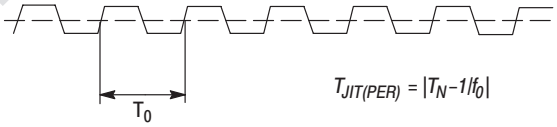

The deviation in $t_0$ for a controlled edge with respect to a $t_0$ mean in a random sample of cycles, measured at the FB signal (only true signal shown)

**Figure 13. I/O Jitter**




The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs, measured at an output (only true signal shown)

**Figure 14. Cycle–to–cycle Jitter**




The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles (only true signal shown)

**Figure 15. Period Jitter**

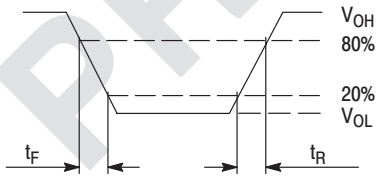



**Figure 16. Output Transition Time Test Reference**

**Order Number: MPC9991/D**
**Rev 0, 12/2001**

*Product Preview*

# 3.3V Differential ECL/PECL PLL Clock Generator

**MPC9991**

**3.3V DIFFERENTIAL ECL/PECL PLL CLOCK GENERATOR**

**FA SUFFIX**
52 LEAD LQFP PACKAGE
CASE 848D

2

The MPC9991 is a 3.3 V compatible, PLL based ECL/PECL clock driver. Using SiGe technology and a fully differential design ensures optimum skew and PLL jitter performance. The performance of the MPC9991 makes the device ideal for workstation, mainframe computer and telecommunication applications. With output frequencies up to 400 MHz and output skews less than 150 ps[1] the device meets the needs of the most demanding clock applications. The MPC9991 offers a differential ECL/PECL input for applications which need to lock to an existing clock signal. It also offers a secondary single–ended ECL/PECL clock for system test capabilities.

**Features**

- 13 differential outputs, PLL based clock generator
- SiGe technology supports minimum output skew (max. 150 ps[1])
- Supports up to three individual generated output clock frequencies with a maximum clock frequency up to 400 MHz
- External PLL feedback supports zero-delay capability
- Selectable SYNC pulse generation
- ECL/PECL compatible differential clock inputs and outputs
- Single 3.3V (PECL) or -3.3V (ECL) supply
- Ambient temperature range 0°C to +70°C
- Standard 52 lead LQFP package
- Pin and function compatible to the MPC991

**Functional Description**

The MPC9991 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9991 requires the connection of the differential PLL feedback output QFB to the differential feedback input FB_IN to close the PLL feedback path. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. The MPC9991 features frequency programmability between the three output banks outputs as well as the output to input relationships. Output frequency ratios of 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 4:3:1 and 4:3:2 can be realized. The three banks of outputs can each be programmed by the FSEL[3:0] pins of the device. There are 16 different output frequency configurations available in the device. Additionally, the device supports a separate configurable feedback output. This allows for the feedback frequency to be programmed independently of the other outputs, providing six input to output frequency ratios that can be configured by the FSEL_FB[2:0] inputs. The external feedback feature enables the use of the MPC9991 as a zero-delay buffer. The VCO_SEL pin provides an extended PLL input reference frequency range.

The SYNC pulse generator monitors the phase relationship between the QA[3:] and QC[2:0] output banks. The SYNC generator output signals the coincident edges of the two output banks. This feature is useful for non binary relationships between output frequencies (i.e., 3:2 or 4:3 relationships). The SYNC_SEL input switches the QD[1:0] outputs between the SYNC signals and an extensions to the QC bank of outputs. The REF_SEL pin selects the differential ECL/PECL compatible input pair or a single-ended ECL/PECL compatible input as the reference clock signal. The $\overline{\text{PLL\_EN}}$ control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply. The MPC9991 requires an external reset signal for start-up and for PLL recovery in the case the external feedback is interrupted. The MPC9991 is fully 3.3V (PECL) or -3.3V (ECL) compatible and requires no external loop filter components. All inputs accept PECL/ECL compatible differential signals while the outputs provide PECL/ECL compatible levels with the capability to drive terminated 50 Ω transmission lines. The device is pin and function compatible to the MPC991 and is packaged in a 52-lead LQFP package.

1. Final specification of this parameter is pending characterization.



**Rev 0**

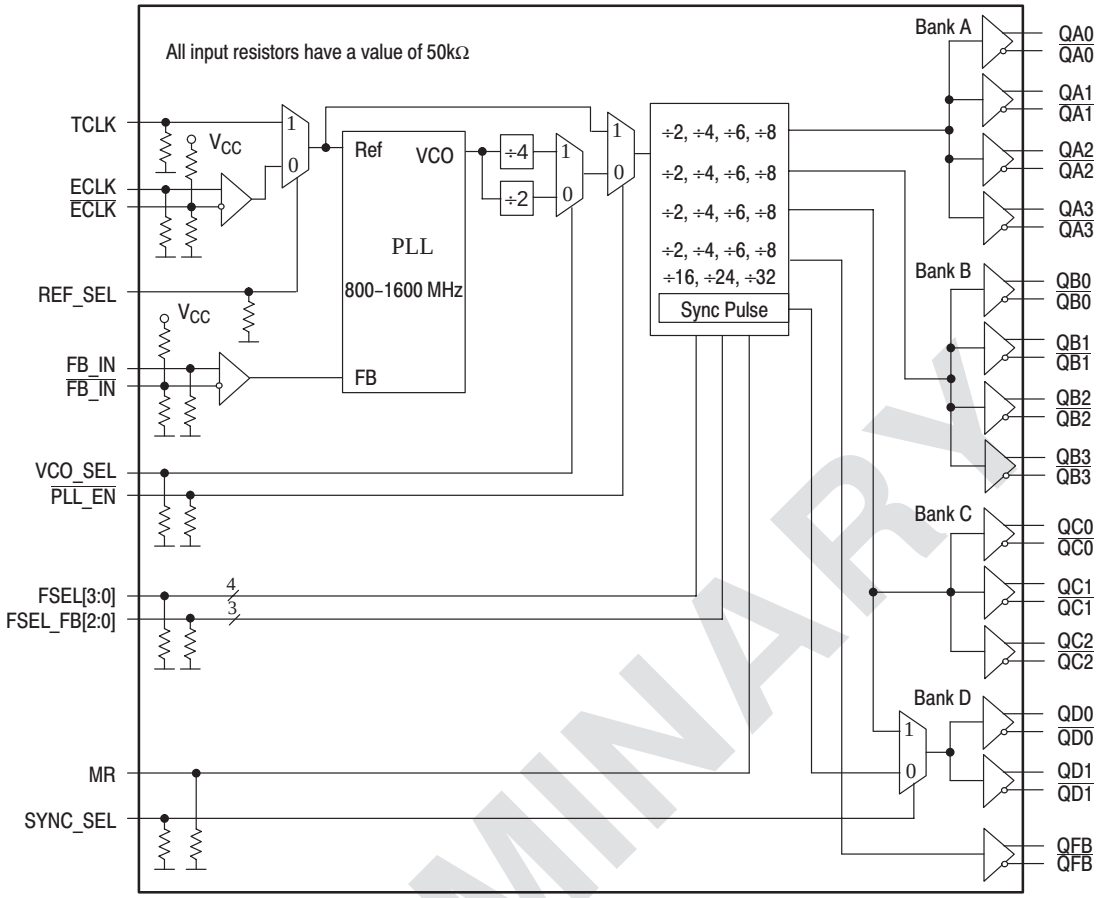



**Figure 1. MPC9991 Logic Diagram**



**FUNCTION TABLE**

| Control | Default | 0 | 1 |
|---|---|---|---|
| REF_SEL | 0 | Selects ECLK, $\overline{\text{ECLK}}$ as PLL refererence signal input | Selects TCKL as PLL reference signal input |
| VCO_SEL | 0 | Selects VCO÷2. (high input frequency range) | Selects VCO÷4. The VCO frequency is scaled by a factor of 4 (low input frequency range). |
| $\overline{\text{PLL\_EN}}$ | 0 | Normal operation mode with PLL enabled. | Test mode with the PLL bypassed. The reference clock is substituted for the internal VCO output. MPC9991 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable. |
| MR | 0 | Normal operation | Reset of the device. During reset the PLL feedback loop is open and the internal VCO is tied to its lowest frequency. The MPC9991 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLKx) |
| SYNC_SEL | 0 | QD[1:0] outputs generate a SYNC signal | QD[1:0] outputs generate clock signals that match the QC[2:0] outputs |
| VCO_SEL, FSEL[3:0] and FSEL_FB[2:0] control the operating PLL frequency range and input/output frequency ratios. See Table 2 and Table 3 for the device frequency configuration. | | | |

2

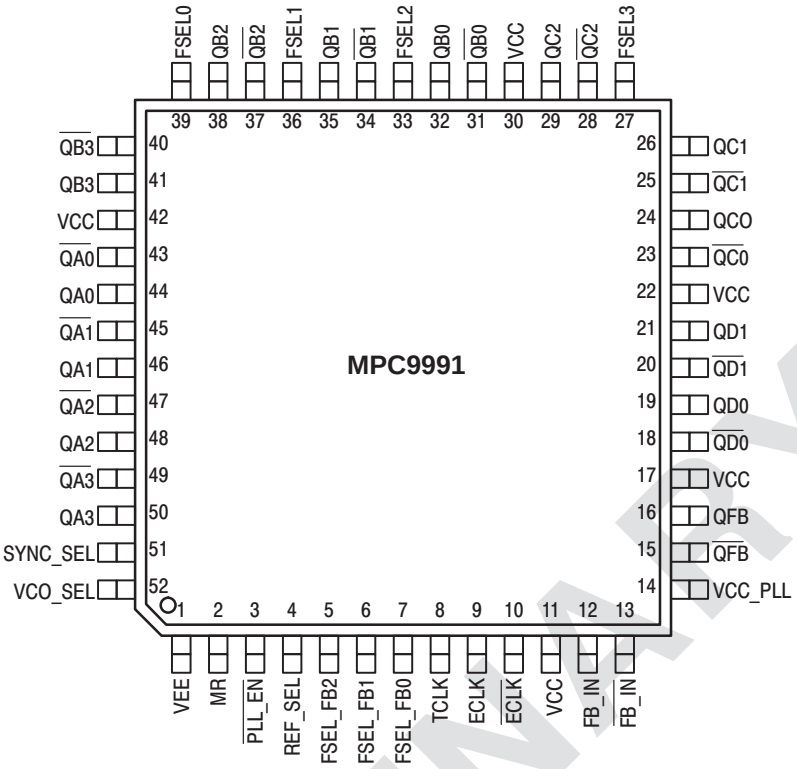



**Figure 2. MPC9991 52–Lead Package Pinout** (Top View)

**Table 1: PIN CONFIGURATION**

| Pin | I/O | Type | Function |
|---|---|---|---|
| ECLK, $\overline{\text{ECLK}}$ | Input | PECL/ECL | Differential reference clock signal input |
| TCLK | Input | PECL/ECL | Single-ended test clock input |
| FB_IN, $\overline{\text{FB\_IN}}$ | Input | PECL/ECL | Differential PLL feedback clock signal input, connect to QFB, $\overline{\text{QFB}}$ |
| VCO_SEL | Input | PECL/ECL | VCO operating frequency select |
| $\overline{\text{PLL\_EN}}$ | Input | PECL/ECL | PLL Enable/Bypass mode select |
| REF_SEL | Input | PECL/ECL | PLL reference signal input select |
| MR | Input | PECL/ECL | Device reset |
| FSEL[3:0] | Input | PECL/ECL | Output frequency divider select |
| FSEL_FB[2:0] | Input | PECL/ECL | Frequency divider select for the QFB output |
| SYNC_SEL | Input | PECL/ECL | QD output mode select |
| QA[0-3], $\overline{\text{QA[0-3]}}$ | Output | PECL/ECL | Differential clock outputs (bank A) |
| QB[0-3], $\overline{\text{QB[0-3]}}$ | Output | PECL/ECL | Differential clock outputs (bank B) |
| QC[0-2], $\overline{\text{QC[0-2]}}$ | Output | PECL/ECL | Differential clock outputs (bank C) |
| QD[0-1], $\overline{\text{QD[0-1]}}$ | Output | PECL/ECL | Differential clock/SYNC signal outputs (bank D) |
| QFB, $\overline{\text{QFB}}$ | Output | PECL/ECL | Differential PLL feedback clock output (connect to FB_IN, $\overline{\text{FB\_IN}}$) |
| VEE[a] | Supply | VEE | Negative power supply |
| $V_{CC}$ | Supply | VCC | Positive power supply. All $V_{CC}$ pins must be connected to the positive power supply for correct DC and AC operation |
| VCC_PLL | Supply | VCC | PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin VCC_PLL. Please see applications section for details |

a. In ECL mode (negative power supply mode), VEE is -3.3V and VCC is connected to GND (0V).
In PECL mode (positive power supply mode), VEE is connected to GND (0V) and VCC is +3.3V.
In both modes, the input and output levels are referenced to the most positive supply (VCC).

**Table 2: Output Divider PLL Feedback M (QFB)**

| VCO_SEL | FSEL_B2 | FSEL_FB1 | FSEL_FB0 | QFB |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | VCO÷4 |
| 0 | 0 | 0 | 1 | VCO÷8 |
| 0 | 0 | 1 | 0 | VCO÷12 |
| 0 | 0 | 1 | 1 | VCO÷16 |
| 0 | 1 | 0 | 0 | VCO÷16 |
| 0 | 1 | 0 | 1 | VCO÷32 |
| 0 | 1 | 1 | 0 | VCO÷48 |
| 0 | 1 | 1 | 1 | VCO÷64 |
| 1 | 0 | 0 | 0 | VCO÷8 |
| 1 | 0 | 0 | 1 | VCO÷16 |
| 1 | 0 | 1 | 0 | VCO÷24 |
| 1 | 0 | 1 | 1 | VCO÷32 |
| 1 | 1 | 0 | 0 | VCO÷32 |
| 1 | 1 | 0 | 1 | VCO÷64 |
| 1 | 1 | 1 | 0 | VCO÷96 |
| 1 | 1 | 1 | 1 | VCO÷128 |

**Table 3: Output Divider N (Bank A to Bank C)**

| VCO_SEL | FSEL3 | FSEL2 | FSEL1 | FSEL0 | QA[3:0] | QB[3:0] | QC[2:0] |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | VCO÷4 | VCO÷4 | VCO÷4 |
| 0 | 0 | 0 | 0 | 1 | VCO÷4 | VCO÷4 | VCO÷8 |
| 0 | 0 | 0 | 1 | 0 | VCO÷4 | VCO÷8 | VCO÷8 |
| 0 | 0 | 0 | 1 | 1 | VCO÷4 | VCO÷4 | VCO÷12 |
| 0 | 0 | 1 | 0 | 0 | VCO÷4 | VCO÷12 | VCO÷12 |
| 0 | 0 | 1 | 0 | 1 | VCO÷4 | VCO÷8 | VCO÷12 |
| 0 | 0 | 1 | 1 | 0 | VCO÷4 | VCO÷8 | VCO÷16 |
| 0 | 0 | 1 | 1 | 1 | VCO÷4 | VCO÷12 | VCO÷16 |
| 0 | 1 | 0 | 0 | 0 | VCO÷4 | VCO÷4 | VCO÷16 |
| 0 | 1 | 0 | 0 | 1 | VCO÷4 | VCO÷16 | VCO÷16 |
| 0 | 1 | 0 | 1 | 0 | VCO÷8 | VCO÷8 | VCO÷12 |
| 0 | 1 | 0 | 1 | 1 | VCO÷8 | VCO÷12 | VCO÷12 |
| 0 | 1 | 1 | 0 | 0 | VCO÷8 | VCO÷12 | VCO÷16 |
| 0 | 1 | 1 | 0 | 1 | VCO÷12 | VCO÷12 | VCO÷16 |
| 0 | 1 | 1 | 1 | 0 | VCO÷12 | VCO÷16 | VCO÷16 |
| 0 | 1 | 1 | 1 | 1 | VCO÷16 | VCO÷16 | VCO÷16 |
| 1 | 0 | 0 | 0 | 0 | VCO÷8 | VCO÷8 | VCO÷8 |
| 1 | 0 | 0 | 0 | 1 | VCO÷8 | VCO÷8 | VCO÷16 |
| 1 | 0 | 0 | 1 | 0 | VCO÷8 | VCO÷16 | VCO÷16 |
| 1 | 0 | 0 | 1 | 1 | VCO÷8 | VCO÷8 | VCO÷24 |
| 1 | 0 | 1 | 0 | 0 | VCO÷8 | VCO÷24 | VCO÷24 |
| 1 | 0 | 1 | 0 | 1 | VCO÷8 | VCO÷16 | VCO÷24 |
| 1 | 0 | 1 | 1 | 0 | VCO÷8 | VCO÷16 | VCO÷32 |
| 1 | 0 | 1 | 1 | 1 | VCO÷8 | VCO÷24 | VCO÷32 |
| 1 | 1 | 0 | 0 | 0 | VCO÷8 | VCO÷8 | VCO÷32 |
| 1 | 1 | 0 | 0 | 1 | VCO÷32 | VCO÷32 | VCO÷32 |
| 1 | 1 | 0 | 1 | 0 | VCO÷16 | VCO÷16 | VCO÷24 |
| 1 | 1 | 0 | 1 | 1 | VCO÷16 | VCO÷24 | VCO÷24 |
| 1 | 1 | 1 | 0 | 0 | VCO÷16 | VCO÷24 | VCO÷32 |
| 1 | 1 | 1 | 0 | 1 | VCO÷24 | VCO÷24 | VCO÷32 |

**Table 4: ABSOLUTE MAXIMUM RATINGS[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage Temperature | -65 | 125 | °C | |

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 5: GENERAL SPECIFICATIONS**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output Termination Voltage | | $V_{CC}$ – 2 | | V | |
| MM | ESD Protection (Machine Model) | TBD | | | V | |
| HBM | ESD Protection (Human Body Model) | TBD | | | V | |
| CDM | ESD Protection (Charged Device Model) | TBD | | | V | |
| LU | Latch–Up Immunity | 200 | | | mA | |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | Inputs |
| $\theta_{JC}$ | Thermal resistance (junction-to-ambient, junction-to-board, junction-to-case) | | TBD | | °C/W | |
| $T_J$ | Operating junction temperature[a] (continuous operation) MTBF = 9.1 years | 0 | | 110 | °C | |

a. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MPC9991 to be used in applications requiring industrial temperature range. It is recommended that users of the MPC9991 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

**Table 6: PECL DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $V_{EE}$ = GND, $T_A$ = 0°C to 70°C)[a]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Differential PECL clock inputs (ECLK, $\overline{\text{ECLK}}$ and FB_IN, $\overline{\text{FB\_IN}}$)[b] | | | | | | |
| $V_{PP}$ | AC differential input voltage[c] | 0.1 | | 1.3 | V | Differential operation |
| $V_{CMR}$ | Differential cross point voltage[d] | 1.0 | | $V_{CC}$-0.3 | V | Differential operation |
| Single-ended PECL clock inputs (TCLK, VCO_SEL, $\overline{\text{PLL\_EN}}$, MR, REF_SEL, SYNC_SEL, FSEL_FB[2:0], FSEL[3:0]) | | | | | | |
| $V_{IH}$ | Input High Voltage | TBD | | TBD | | |
| $V_{IL}$ | Input Low Voltage | TBD | | TBD | | |
| $I_{IN}$ | Input Current | | | ±TBD | µA | $V_{IN}$ = TBD or $V_{IN}$ = TBD |
| PECL clock outputs (QA[3:0], $\overline{\text{QA[3:0]}}$, QB[3:0], $\overline{\text{QB[3:0]}}$, QC[2:0], $\overline{\text{QC[2:0]}}$, QD[1:0], $\overline{\text{QD[1:0]}}$) | | | | | | |
| $V_{OH}$ | Output High Voltage | TBD | $V_{CC}$-1.005 | TBD | V | Termination 50Ω to $V_{TT}$ |
| $V_{OL}$ | Output Low Voltage | TDB | $V_{CC}$-1.705 | TBD | V | Termination 50Ω to $V_{TT}$ |
| Supply Current | | | | | | |
| $I_{EE}$ | Maximum Quiescent Supply Current without output termination current | | TBD | TBD | mA | $V_{EE}$ pin |
| $I_{CCe}$ | Maximum Quiescent Supply Current, outputs terminated 50Ω to $V_{TT}$ | | TBD | TBD | mA | $V_{CC}$ pins |

a. AC characteristics are design targets and pending characterization.
b. Clock inputs driven by PECL compatible signals.
c. $V_{PP}$ is the minimum differential input voltage swing required to maintain AC characteristics.
d. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.
e. $I_{CC}$ includes current through the output resistors (all outputs terminated to $V_{TT}$).

**Table 7: ECL DC CHARACTERISTICS** ($V_{EE}$ = –3.3V ± 5%, $V_{CC}$ = GND, $T_A$ = 0°C to 70°C)[a]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Differential ECL clock inputs (ECLK, $\overline{\text{ECLK}}$ and FB_IN, $\overline{\text{FB\_IN}}$)[b] | | | | | | |
| $V_{PP}$ | Differential input voltage[c] | 0.1 | | 1.3 | V | Differential operation |
| $V_{CMR}$ | Differential cross point voltage[d] | $V_{EE}$+1.0 | | -0.3 | V | Differential operation |
| $I_{IN}$ | Input Current[a] | | | ±150 | µA | $V_{IN}$ = $V_{IL}$ or $V_{IN}$ = $V_{IH}$ |
| Single-ended ECL clock inputs (TCLK, VCO_SEL, $\overline{\text{PLL\_EN}}$, MR, REF_SEL, SYNC_SEL, FSEL_FB[2:0], FSEL[3:0]) | | | | | | |
| $V_{IL}$ | Input Voltage Low | | | -1.46 | V | |
| $V_{IH}$ | Input Voltage High | -1.14 | | | V | |
| $I_{IN}$ | Input Current[e] | | | ±150 | µA | $V_{IN}$ = $V_{IL}$ or $V_{IN}$ = $V_{IH}$ |
| ECL clock outputs (QA[3:0], $\overline{\text{QA[3:0]}}$, QB[3:0], $\overline{\text{QB[3:0]}}$, QC[2:0], $\overline{\text{QC[2:0]}}$, QD[1:0], $\overline{\text{QD[1:0]}}$) | | | | | | |
| $V_{OH}$ | Output High Voltage | TBD | -1.005 | TBD | V | Termination 50Ω to $V_{TT}$ |
| $V_{OL}$ | Output Low Voltage | TBD | -1.705 | TBD | V | Termination 50Ω to $V_{TT}$ |
| Supply current and V | | | | | | |
| $I_{EE}$ | Maximum Quiescent Supply Current without output termination current | | TBD | TBD | mA | $V_{EE}$ pin |
| $I_{CCf}$ | Maximum Quiescent Supply Current, outputs terminated 50Ω to $V_{TT}$ | | TBD | TBD | mA | $V_{CC}$ pins |

a. DC characteristics are design targets and pending characterization.
b. Clock inputs driven by PECL compatible signals.
c. $V_{PP}$ (DC) is the minimum differential input voltage swing required to maintain device functionality.
d. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.
e. Input have internal pullup/pulldown resistors which affect the input current.
f. $I_{CC}$ includes current through the output resistors (all outputs terminated to $V_{TT}$).

**Table 8: AC CHARACTERISTICS** (ECL: $V_{EE}$ = –3.3V ± 5%, $V_{CC}$ = GND, or PECL: $V_{CC}$ = 3.3V ± 5%, $V_{EE}$ = GND, $T_A$ = 0°C to 70°C)[a] [b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input reference frequency | ÷4 feedback | 200.0 | | 400.0 | MHz | PLL locked |
| | | ÷8 feedback | 100.0 | | 200.0 | MHz | |
| | | ÷12 feedback | 66.6 | | 133.3 | MHz | |
| | | ÷16 feedback | 50.0 | | 100.0 | MHz | |
| | | ÷24 feedback | 33.3 | | 66.6 | MHz | |
| | | ÷32 feedback | 25.0 | | 50.0 | MHz | |
| | | ÷48 feedback | 16.6 | | 33.3 | MHz | |
| | | ÷64 feedback | 12.5 | | 25.0 | MHz | |
| | | ÷96 feedback | 8.3 | | 16.6 | MHz | |
| | | ÷128 feedback | 6.25 | | 12.5 | MHz | |
| | Input reference frequency in PLL bypass mode[c] | | | | TBD | MHz | PLL bypass |
| $f_{VCO}$ | VCO frequency range[d] | | 800 | | 1600 | MHz | |
| $f_{MAX}$ | Output Frequency | ÷4 output | 200.0 | | 400.0 | MHz | PLL locked |
| | | ÷8 output | 100.0 | | 200.0 | MHz | |
| | | ÷12 output | 66.6 | | 133.3 | MHz | |
| | | ÷16 output | 50.0 | | 100.0 | MHz | |
| | | ÷24 output | 33.3 | | 66.6 | MHz | |
| | | ÷32 output | 25.0 | | 50.0 | MHz | |
| $V_{PP}$ | Differential input voltage[e] (peak-to-peak) | | | 0.3 | 1.3 | V | |
| $V_{CMR}$ | Differential input crosspoint voltage[f] | PECL | | | $V_{CC}$-0.3 | V | |
| | | ECL | | | -0.3 | | |
| $V_{O(P-P)}$ | Differential output voltage (peak-to-peak) | | | 0.8 | TBD | V | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | | 60 | % | |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) | | | | | | PLL locked |
| | ECLK, $\overline{\text{ECLK}}$ to FB_IN, $\overline{\text{FB\_IN}}$ | | | ±150 | | ps | |
| | TCLK to FB_IN, $\overline{\text{FB\_IN}}$ | | | ±150 | | ps | |
| $t_{sk(O)}$ | Output-to-output Skew[g] | | | | 150 | ps | |
| DC | Output duty cycle | | 45 | 50 | 55 | % | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ)[h] | | TBD | | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | TBD | | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1 σ) | | TBD | | ps | |
| BW | PLL closed loop bandwidth[i] | | | | | kHz | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 10 | | ms | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.05 | | TBD | ns | 20% to 80% |

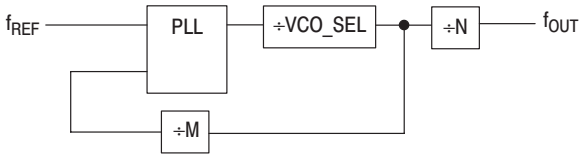
a. AC characteristics are design targets and pending characterization.
b. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
c. In bypass mode, the MPC9991 divides the input reference clock.
d. The input reference frequency must match the VCO lock range divided by the total feedback divider ratio: $f_{ref} = f_{VCO} \div (M \cdot VCO\_SEL)$.
e. $V_{PP}$ is the minimum differential input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
f. $V_{CMR}$ (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ (AC) range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ (AC) or $V_{PP}$ (AC) impacts the device propagation delay, device and part-to-part skew.
g. See application section for part-to-part skew calculation.
h. See application section for a jitter calculation for other confidence factors than 1 σ.
i. -3 dB point of PLL transfer characteristics.

## APPLICATIONS INFORMATION

### MPC9991 Configurations

Configuring the MPC9991 amounts to properly configuring the internal dividers to produce the desired output frequencies. The output frequency can be represented by this formula:

$$f_{OUT} = f_{REF} \cdot M \div N$$




where $f_{REF}$ is the reference frequency of the selected input clock source (ECLK or TCLK), M is the PLL feedback divider and N is a output divider. M is configured by the FSEL_FB[2:0] and N is configured for all output banks by the FSEL[3:0] inputs.

The reference frequency $f_{REF}$ and the selection of the feedback-divider M is limited by the specified VCO frequency range. $f_{REF}$ and M must be configured to match the VCO frequency range of 800 to 1600 MHz in order to achieve stable PLL operation:

$$f_{VCO,MIN} \leq (f_{REF} \cdot VCO\_SEL \cdot M) \leq f_{VCO,MAX}$$

The PLL post-divider VCO_SEL is either a divide-by-two or a divide-by-four and can be used to situate the VCO into the specified frequency range. This divider is controlled by the VCO_SEL pin. VCO_SEL effectively extends the usable input frequency range while it has no effect on the output to reference frequency ratio.

The output frequency for each bank can be derived from the VCO frequency and output divider:

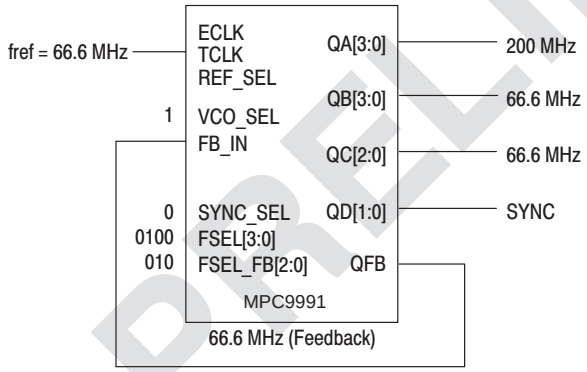
$$f_{QA[4:0]} = f_{VCO} \div (VCO\_SEL \cdot N_A)$$
$$f_{QB[4:0]} = f_{VCO} \div (VCO\_SEL \cdot N_B)$$
$$f_{QC[3:0]} = f_{VCO} \div (VCO\_SEL \cdot N_C)$$

**Table 9: MPC9991 Divider**

| Divider | Function | VCO_SEL | Values |
|---|---|---|---|
| M | PLL feedback FSEL_FB[2:0] | ÷2 | 4, 8, 12, 16, 32, 48, 64 |
| | | ÷4 | 8, 16, 24, 32, 64, 96, 128 |
| $N_A$ | Bank A Output Divider FSEL_A | ÷2 | 4, 8, 12, 16 |
| | | ÷4 | 8, 16, 24, 32 |
| $N_B$ | Bank B Output Divider FSEL_B | ÷2 | 4, 8, 12, 16 |
| | | ÷4 | 8, 16, 24, 32 |
| $N_C$ | Bank C Output Divider FSEL_C | ÷2 | 4, 8, 12, 16 |
| | | ÷4 | 8, 16, 24, 32 |

Table 9 shows the various PLL feedback and output dividers. The output dividers for the three output banks allow the user to configure the outputs into 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 4:3:1 and 4:3:2 frequency ratios. Figure 3 and Figure 4 display example configurations for the MPC9991:

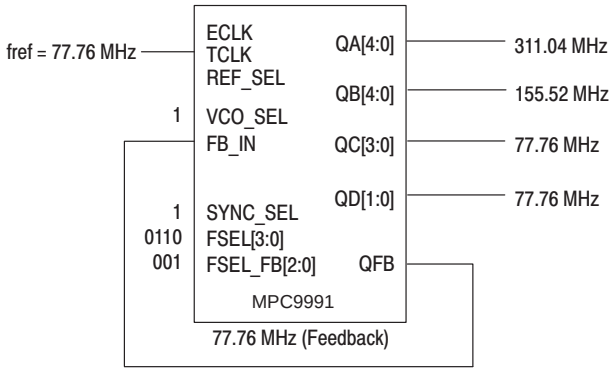
**Figure 3. Example Configuration**




MPC9991 example configuration (feedback of QFB = 66.6 MHz, VCO_SEL=÷4, M=6, $N_A$=2, $N_B$=6, $N_C$=6, $f_{VCO}$=1600 MHz).

| Frequency range | Min | Max |
|---|---|---|
| Input | 33.3 MHz | 66.6 MHz |
| QA outputs | 100 MHz | 200 MHz |
| QB outputs | 33.3 MHz | 66.6 MHz |
| QC outputs | 33.3 MHz | 66.6 MHz |

**Figure 4. Example Configuration**




MPC9991 example configuration (feedback of QFB = 77.76 MHz, VCO_SEL=÷2, M=8, $N_A$=2, $N_B$=4, $N_C$=8, $f_{VCO}$=1244.16 MHz).

| Frequency range | Min | Max |
|---|---|---|
| Input | 50 MHz | 100 MHz |
| QA outputs | 200 MHz | 400 MHz |
| QB outputs | 100 MHz | 200 MHz |
| QC outputs | 50 MHz | 100 MHz |
| QD outputs | 50 MHz | 100 MHz |

**SYNC Output Description**

The MPC9991 has a system synchronization pulse generator. In configurations with the output frequency relationships are not integer multiples of each other SYNC provides a signal for system synchronization purposes. The MPC9991 monitors the relationship between the A bank and the C bank of outputs. The SYNC output is asserted (logic high) depending on the placement of the clock edges of the QA and QC outputs. The QSYNC pulse width is equal to the period of the higher of the QA and QC output frequencies. Figure 5 shows various waveforms for the SYNC pulse. The SYNC signal is defined for all possible combinations of the bank A and bank C outputs. The SYNC signal is routed to the QD bank of outputs if the SYNC_SEL input is set to logic 0, otherwise the SYNC signal generation is disabled and the QD outputs match the QC output bank signals.



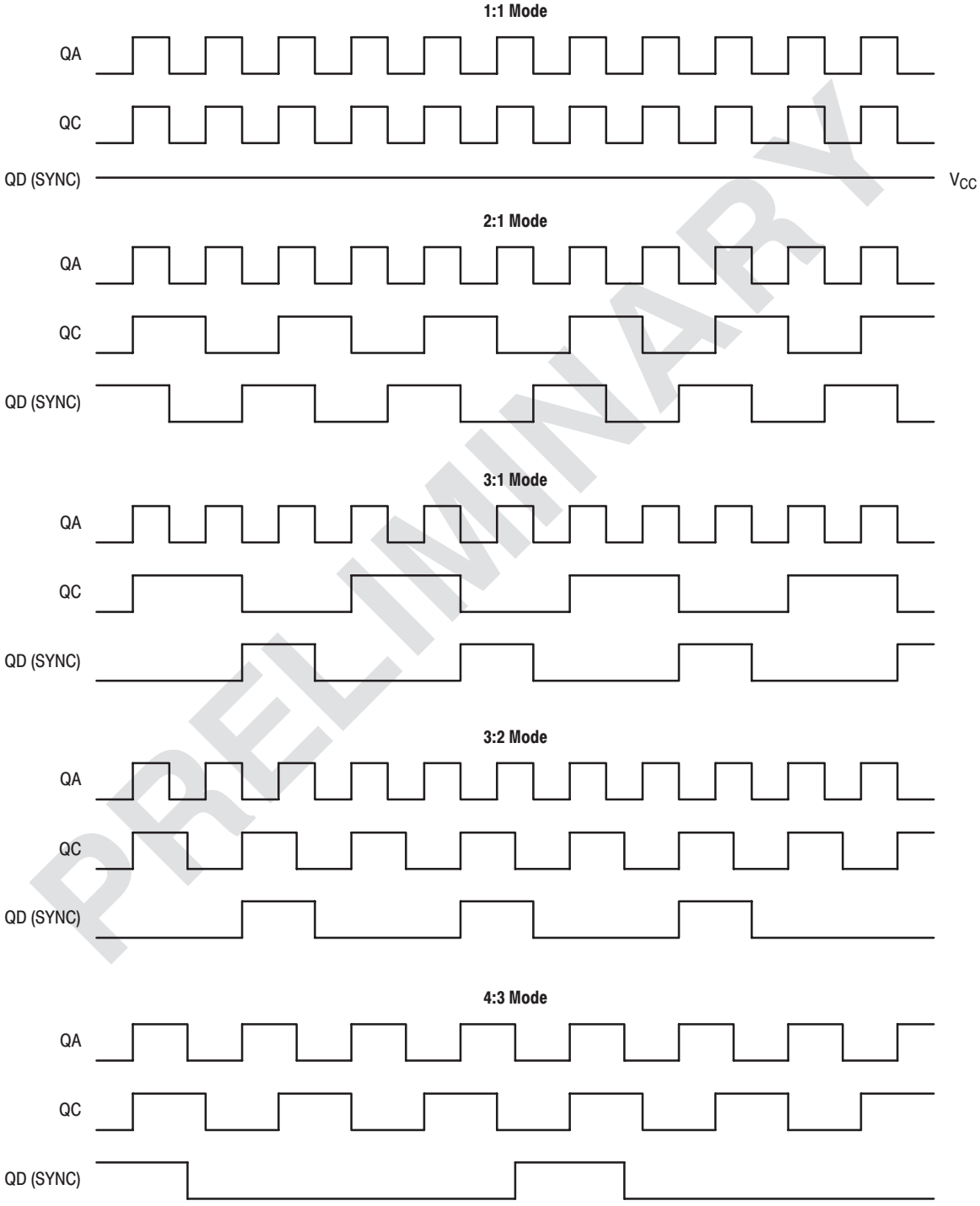



**Figure 5. QSYNC Timing Diagram**

### Power Supply Filtering

The MPC9991 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the $V_{CC\_PLL}$ power supply impacts the device characteristics, for instance I/O jitter. The MPC9991 provides separate power supplies for the output buffers ($V_{CC}$) and the phase-locked loop ($V_{CC\_PLL}$) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the $V_{CCA\_PLL}$ pin for the MPC9991. Figure 6 illustrates a typical power supply filter scheme. The MPC9991 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor $R_F$. From the data sheet the $I_{CC\_PLL}$ current (the current sourced through the $V_{CC\_PLL}$ pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V ($V_{CC}$=3.3V or $V_{CC}$=2.5V) must be maintained on the $V_{CC\_PLL}$ pin. The resistor $R_F$ shown in Figure 6 "$V_{CC\_PLL}$ Power Supply Filter" must have a resistance of 9-10Ω ($V_{CC}$=2.5V) to meet the voltage drop criteria.

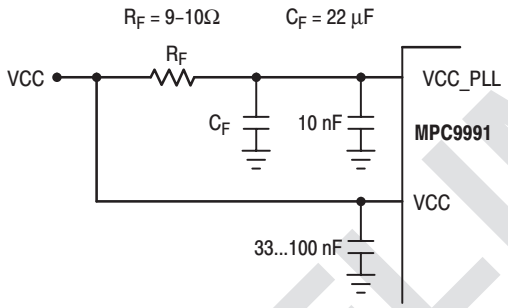



**Figure 6. $V_{CC\_PLL}$ Power Supply Filter**

The minimum values for $R_F$ and the filter capacitor $C_F$ are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 6 "$V_{CC\_PLL}$ Power Supply Filter", the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9991 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

### Using the MPC9991 in zero–delay applications

Nested clock trees are typical applications for the MPC9991. Designs using the MPC9991 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC9991 clock driver allows for its use as a zero delay buffer. One example configuration is to use a ÷4 output as a feedback to the PLL and configuring all other outputs to a divide-by-4 mode. The propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

### Calculation of part-to-part skew

The MPC9991 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9991 are connected together, the maximum overall timing uncertainty from the common CCLKx input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

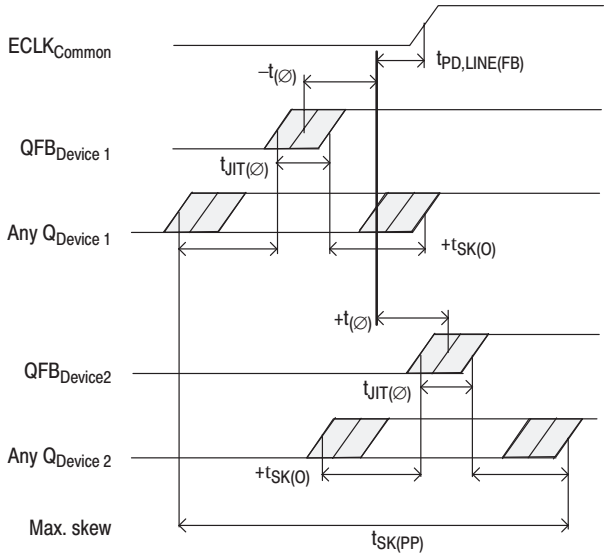



**Figure 7. MPC9991 max. device-to-device skew**

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 10.

**Table 10: Confidence Facter CF**

| CF | Probability of clock edge within the distribution |
|---|---|
| ± 1σ | 0.68268948 |
| ± 2σ | 0.95449988 |
| ± 3σ | 0.99730007 |
| ± 4σ | 0.99993663 |
| ± 5σ | 0.99999943 |
| ± 6σ | 0.99999999 |

2

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of -345 ps to 345 ps[1] relative to CCLK:

$t_{SK(PP)}$ = *[–150ps...150ps] + [–150ps...150ps] + [(15ps · –3)...(15ps · 3)] +* $t_{PD,\ LINE(FB)}$

$t_{SK(PP)}$ = *[–345ps...345ps] +* $t_{PD,\ LINE(FB)}$

Due to the frequency dependence of the I/O jitter, Figure 8 “Max. I/O Jitter versus frequency” can be used for a more precise timing performance analysis.

TBD
See MPC961C application section for an example I/O jitter characteristics

**Figure 8. Max. I/O Jitter versus frequency**

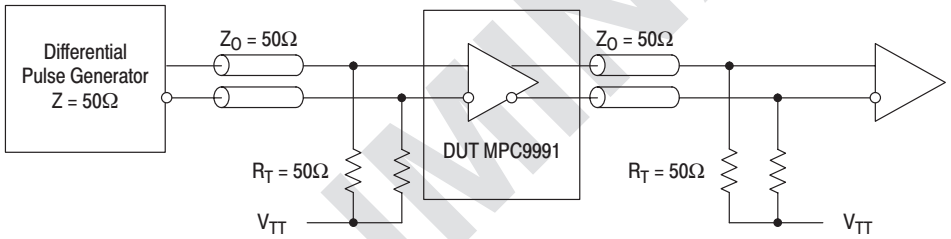



**Figure 9. MPC9991 AC test reference**

**Order Number: MPC9992/D**
**Rev 0, 12/2001**

*Product Preview*

# 3.3V Differential ECL/PECL PLL Clock Generator

**MPC9992**

**2**

**3.3V DIFFERENTIAL ECL/PECL PLL CLOCK GENERATOR**

**FA SUFFIX**
32 LEAD LQFP PACKAGE
CASE 873A

The MPC9992 is a 3.3 V compatible, PLL based PECL clock driver. Using SiGe technology and a fully differential design ensures optimum skew and PLL jitter performance. The performance of the MPC9992 makes the device ideal for workstation, mainframe computer and telecommunication applications. With output frequencies up to 400 MHz and output skews less than 150 ps[1] the device meets the needs of the most demanding clock applications. The MPC9992 offers a differential PECL input and a crystal oscillator interface. All control signals are LVCMOS compatible.

**Features**

- 7 differential outputs, PLL based clock generator
- SiGe technology supports minimum output skew (max. 150 ps[1])
- Supports up to two generated output clock frequencies with a maximum clock frequency up to 400 MHz
- Selectable crystal oscillator interface and PECL compatible clock input
- SYNC pulse generation
- PECL compatible differential clock inputs and outputs
- Single 3.3V (PECL) supply
- Ambient temperature range 0°C to +70°C
- Standard 32 lead LQFP package
- Pin and function compatible to the MPC992

**Functional Description**

The MPC9992 utilizes PLL technology to frequency lock its outputs onto an input reference clock. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. The MPC9992 features frequency programmability between the three output banks outputs as well as the output to input relationships. Output frequency ratios of 2:1, 3:1, 3:2 and 5:2 can be realized. The two banks of outputs and the feedback frequency divider can be programmed by the FSEL[2:0] pins of the device. The VCO_SEL pin provides an extended PLL input reference frequency range.

The SYNC pulse generator monitors the phase relationship between the QA[3:0] and QB[2:0] output banks. The SYNC generator output signals the coincident edges of the two output banks. This feature is useful for non binary relationships between output frequencies.

The REF_SEL pin selects the differential PECL compatible input pair or crystal oscillator interface as the reference clock signal. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply.

The MPC9992 requires an external reset signal for start-up and for PLL recovery in the case the external feedback is interrupted. Assertion of the reset signal forces all outputs to logic the low state.

The MPC9992 is fully 3.3V compatible and requires no external loop filter components. The differential clock input (PCLK) is PECL compatible and all control inputs accept LVCMOS compatible signals while the outputs provide PECL compatible levels with the capability to drive terminated 50 Ω transmission lines.

The device is pin and function compatible to the MPC992 and is packaged in a 32-lead LQFP package.

1. Final specification of this parameter is pending characterization.


**Rev 0**

2

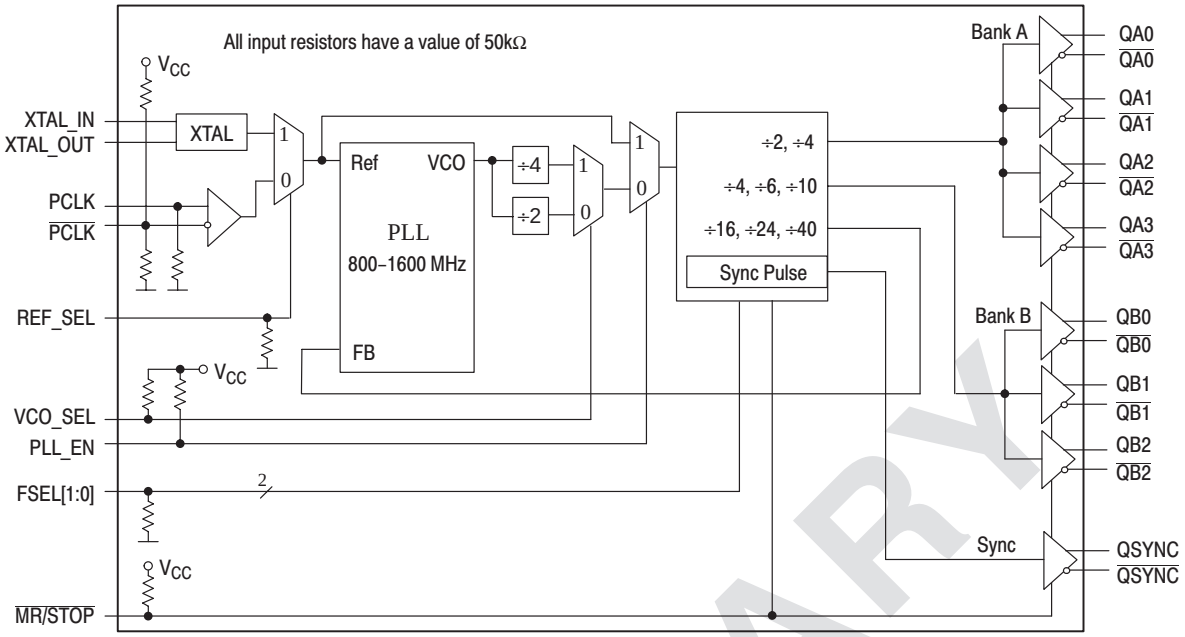



**Figure 1. MPC9992 Logic Diagram**

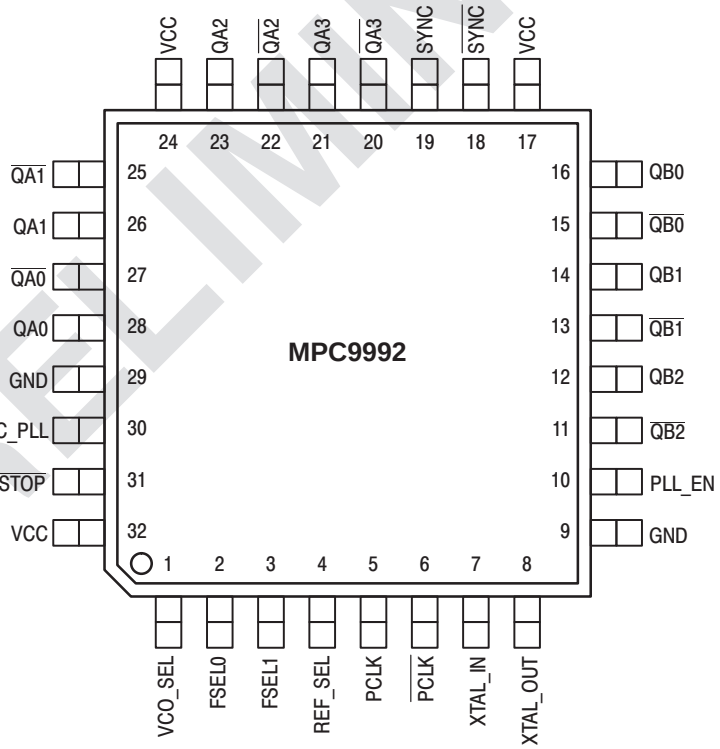



**Figure 2. MPC9992 32–Lead Package Pinout** (Top View)

**Table 1: MPC9992 PLL Configurations**

| VCO_SEL | FSEL_B1 | FSEL_F0 | $f_{REF}$ (MHz) | QA[3:0] ($N_A$) | QB[2:0] ($N_B$) | QB to QA Ratio | Internal Feedback (M · VCO_SEL) |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 16.6–33.3 | VCO÷8 (6 · $f_{REF}$) | VCO÷12 (4 · $f_{REF}$) | 3÷2 | VCO÷48 |
| 0 | 0 | 1 | 25–50 | VCO÷4 (8 · $f_{REF}$) | VCO÷8 (4 · $f_{REF}$) | 2÷1 | VCO÷32 |
| 0 | 1 | 0 | 10–20 | VCO÷8 (10 · $f_{REF}$) | VCO÷20 (4 · $f_{REF}$) | 5÷2 | VCO÷80 |
| 0 | 1 | 1 | 16.6–33.3 | VCO÷4 (12 · $f_{REF}$) | VCO÷12 (4 · $f_{REF}$) | 3÷1 | VCO÷48 |
| 1 | 0 | 0 | 8.3–16.6 | VCO÷16 (6 · $f_{REF}$) | VCO÷24 (4 · $f_{REF}$) | 3÷2 | VCO÷96 |
| 1 | 0 | 1 | 12.5–25 | VCO÷8 (8 · $f_{REF}$) | VCO÷16 (4 · $f_{REF}$) | 2÷1 | VCO÷64 |
| 1 | 1 | 0 | 5–10 | VCO÷16 (10 · $f_{REF}$) | VCO÷40 (4 · $f_{REF}$) | 5÷2 | VCO÷160 |
| 1 | 1 | 1 | 8.3–16.6 | VCO÷8 (12 · $f_{REF}$) | VCO÷24 (4 · $f_{REF}$) | 3÷1 | VCO÷96 |

**Table 2: FUNCTION TABLE (Configuration Controls)**

| Control | Default | 0 | 1 |
|---|---|---|---|
| REF_SEL | 0 | Selects PCLK, $\overline{\text{PCLK}}$ as PLL refererence signal input | Selects the crystal oscillator as PLL reference signal input |
| VCO_SEL | 0 | Selects VCO÷2. The VCO frequency is scaled by a factor of 2 (high input frequency range) | Selects VCO÷4. The VCO frequency is scaled by a factor of 4 (low input frequency range). |
| PLL_EN | 0 | Test mode with the PLL bypassed. The reference clock is substituted for the internal VCO output. MPC9992 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable. | Normal operation mode with PLL enabled. |
| $\overline{\text{MR/STOP}}$ | 0 | Reset of the device and output disable (output clock stop). The outputs are stopped in logic low state: Qx=L, $\overline{\text{Qx}}$=H. The MPC9992 requires reset at power-up and after any loss of PLL lock. The length of the reset pulse should be greater than one reference clock cycle | Normal operation |
| VCO_SEL and FSEL[1:0] control the operating PLL frequency range and input/output frequency ratios. See Table 1 for the device frequency configuration. | | | |

**Table 3: PIN CONFIGURATION**

| Pin | I/O | Type | Function |
|---|---|---|---|
| PCLK, $\overline{\text{PCLK}}$ | Input | PECL | Differential reference clock signal input |
| XTAL_IN, XTAL_OUT | | Analog | Crystal oscillator interface |
| VCO_SEL | Input | LVCMOS | VCO operating frequency select |
| PLL_EN | Input | LVCMOS | PLL Enable/Bypass mode select |
| REF_SEL | Input | LVCMOS | PLL reference signal input select |
| $\overline{\text{MR/STOP}}$ | Input | LVCMOS | Device reset and output clock disable (stop in logic low state) |
| FSEL[1:0] | Input | LVCMOS | Output and PLL feedback frequency divider select |
| QA[0-3], $\overline{\text{QA[0-3]}}$ | Output | PECL | Differential clock outputs (bank A) |
| QB[0-2], $\overline{\text{QB[0-2]}}$ | Output | PECL | Differential clock outputs (bank B) |
| QSYNC, $\overline{\text{QSYNC}}$ | Output | PECL | Differential clock outputs (bank C) |
| GND | Supply | GND | Negative power supply |
| VCC | Supply | VCC | Positive power supply. All $V_{CC}$ pins must be connected to the positive power supply for correct DC and AC operation |
| VCC_PLL | Supply | VCC | PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin VCC_PLL. Please see applications section for details |

**Table 4: ABSOLUTE MAXIMUM RATINGS**[a]

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage Temperature | -65 | 125 | °C | |

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 5: GENERAL SPECIFICATIONS**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output termination voltage | | $V_{CC}$ - 2 | | V | |
| MM | ESD Protection (Machine model) | TBD | | | V | |
| HBM | ESD Protection (Human body model) | TBD | | | V | |
| CDM | ESD Protection (Charged device model | TBD | | | V | |
| LU | Latch-up immunity | 200 | | | mA | |
| $C_{IN}$ | Input capacitance | | 4.0 | | pF | Inputs |
| $\theta_{JA}$ | Thermal resistance junction to ambient | | | | | |
| | JESD 51-3, single layer test board | | 83.1 | 86.0 | °C/W | Natural convection |
| | | | 73.3 | 75.4 | °C/W | 100 ft/min |
| | | | 68.9 | 70.9 | °C/W | 200 ft/min |
| | | | 63.8 | 65.3 | °C/W | 400 ft/min |
| | | | 57.4 | 59.6 | °C/W | 800 ft/min |
| | JESD 51-6, 2S2P multilayer test board | | 59.0 | 60.6 | °C/W | Natural convection |
| | | | 54.4 | 55.7 | °C/W | 100 ft/min |
| | | | 52.5 | 53.8 | °C/W | 200 ft/min |
| | | | 50.4 | 51.5 | °C/W | 400 ft/min |
| | | | 47.8 | 48.8 | °C/W | 800 ft/min |
| $\theta_{JC}$ | Thermal resistance junction to case | | 23.0 | 26.3 | °C/W | MIL-SPEC 883E Method 1012.1 |
| $T_J$ | Operating junction temperature[a] (continuous operation) MTBF = 9.1 years | 0 | | 110 | °C | |

a. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MPC9992 to be used in applications requiring industrial temperature range. It is recommended that users of the MPC9992 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

**Table 6: DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, GND = 0V, $T_A$ = 0°C to 70°C)[a]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Differential PECL clock inputs (PCLK, $\overline{PCLK}$)[b] | | | | | | |
| $V_{PP}$ | AC differential input voltage[c] | 0.1 | | 1.3 | V | Differential operation |
| $V_{CMR}$ | Differential cross point voltage[d] | 1.0 | | $V_{CC}$-0.3 | V | Differential operation |
| $I_{IN}$ | Input Current[e] | | | ±200 | µA | $V_{IN}$=$V_{CC}$ or GND |
| Single-ended PECL clock inputs (VCO_SEL, PLL_EN, $\overline{MR/STOP}$, REF_SEL, FSEL[1:0]) | | | | | | |
| $V_{IH}$ | Input high voltage | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | | | 0.8 | V | LVCMOS |
| $I_{IN}$ | Input Current[e] | | | ±200 | µA | $V_{IN}$=$V_{CC}$ or GND |
| PECL clock outputs (QA[3:0], $\overline{QA[3:0]}$, QB[2:0], $\overline{QB[2:0]}$, QSYNC, $\overline{QSYNC}$) | | | | | | |
| $V_{OH}$ | Output High Voltage | TBD | $V_{CC}$-1.005 | TBD | V | Termination 50Ω to $V_{TT}$ |
| $V_{OL}$ | Output Low Voltage | TDB | $V_{CC}$-1.705 | TBD | V | Termination 50Ω to $V_{TT}$ |
| Supply Current | | | | | | |
| $I_{CC\_PLL}$ | Maximum PLL Supply Current | | 3.0 | 5.0 | mA | $V_{CC\_PLL}$ pin |
| $I_{CCQ}$[f] | Maximum Quiescent Supply Current, outputs terminated 50Ω to $V_{TT}$ | | TBD | 1.0 | mA | $V_{CC}$ pins |

a. AC characteristics are design targets and pending characterization.
b. Clock inputs driven by PECL compatible signals.
c. $V_{PP}$ is the minimum differential input voltage swing required to maintain AC characteristics.
d. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.
e. Inputs have pull-down resistors affecting the input current.
f. $I_{CC}$ includes current through the output resistors (all outputs terminated to $V_{TT}$).

**Table 7: AC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, GND = 0V, $T_A$ = 0°C to +70°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input reference frequency | ÷32 feedback | 25.0 | | 50.0 | MHz | PLL locked |
| | | ÷48 feedback | 16.67 | | 33.3 | MHz | |
| | | ÷64 feedback | 12.5 | | 25.0 | MHz | |
| | | ÷80 feedback | 10.0 | | 20.0 | MHz | |
| | | ÷96 feedback | 8.33 | | 16.67 | MHz | |
| | | ÷160 feedback | 5.0 | | 10.0 | MHz | |
| | Input reference frequency in PLL bypass mode[c] | | | | TBD | MHz | PLL bypass |
| $f_{XTAL}$ | Crystal interface frequency range[d] | | 10 | | 25 | MHz | |
| $f_{VCO}$ | VCO frequency range[e] | | 800 | | 1600 | MHz | |
| $f_{MAX}$ | Output Frequency | ÷4 output | 200.0 | | 400.0 | MHz | PLL locked |
| | | ÷8 output | 100.0 | | 200.0 | MHz | |
| | | ÷12 output | 66.6 | | 133.3 | MHz | |
| | | ÷16 output | 50.0 | | 100.0 | MHz | |
| | | ÷20 output | 40.0 | | 80.0 | MHz | |
| | | ÷24 output | 33.3 | | 66.6 | MHz | |
| | | ÷48 output | 16.6 | | 33.3 | MHz | |
| $V_{PP}$ | Differential input voltage[f] (peak-to-peak) | | | 0.3 | 1.3 | V | |
| $V_{CMR}$ | Differential input crosspoint voltage[g] (PCLK) | | | | $V_{CC}$-0.3 | V | |
| $V_{O(P-P)}$ | Differential output voltage (peak-to-peak) | (PCLK) | | 0.8 | TBD | V | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | | 60 | % | |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) (PCLK, $\overline{PCLK}$ to FB_IN) | | | ±150 | | ps | PLL locked |
| $t_{sk(O)}$ | Output-to-output Skew[h] | | | | 150 | ps | |
| DC | Output duty cycle | | 45 | 50 | 55 | % | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ)[i] | | TBD | | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | TBD | | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1 σ) | | TBD | | ps | |
| BW | PLL closed loop bandwidth[j] | | | | | kHz | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 10 | | ms | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.05 | | TBD | ns | 20% to 80% |

a. AC characteristics are design targets and pending characterization.
b. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
c. In bypass mode, the MPC9992 divides the input reference clock.
d. The crystal frequency range must both meet the interface frequency range and VCO lock range divided by the feedback divider ratio: $f_{XTAL(min, max)} = f_{VCO(min, max)} \div (M \cdot VCO\_SEL)$ and 10 MHz ≤ $f_{XTAL}$ ≤ 25 MHz.
e. The input reference frequency must match the VCO lock range divided by the total feedback divider ratio: $f_{ref} = f_{VCO} \div (M \cdot VCO\_SEL)$
f. $V_{PP}$ is the minimum differential input voltage swing required to maintain AC characteristics including tpd and device-to-device skew
g. $V_{CMR}$ (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ (AC) range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ (AC) or $V_{PP}$ (AC) impacts the device propagation delay, device and part-to-part skew.
h. See application section for part-to-part skew calculation.
i. See application section for a jitter calculation for other confidence factors than 1 σ.
j. -3 dB point of PLL transfer characteristics.

## APPLICATIONS INFORMATION

### SYNC Output Description

The MPC9992 has a system synchronization pulse output QSYNC. In configurations with the output frequency relationships are not integer multiples of each other QSYNC provides a signal for system synchronization purposes. The MPC9992 monitors the relationship between the A bank and the B bank of outputs. The QSYNC output is asserted (logic high) one QA period in duration after the coincident rising edges of the QA and QB outputs. The placement of the pulse is dependent QA and QB output frequencies ratio. Table 2 shows the waveforms for the QSYNC output. The QSYNC output is defined for all possible combinations of the bank A and bank B outputs.



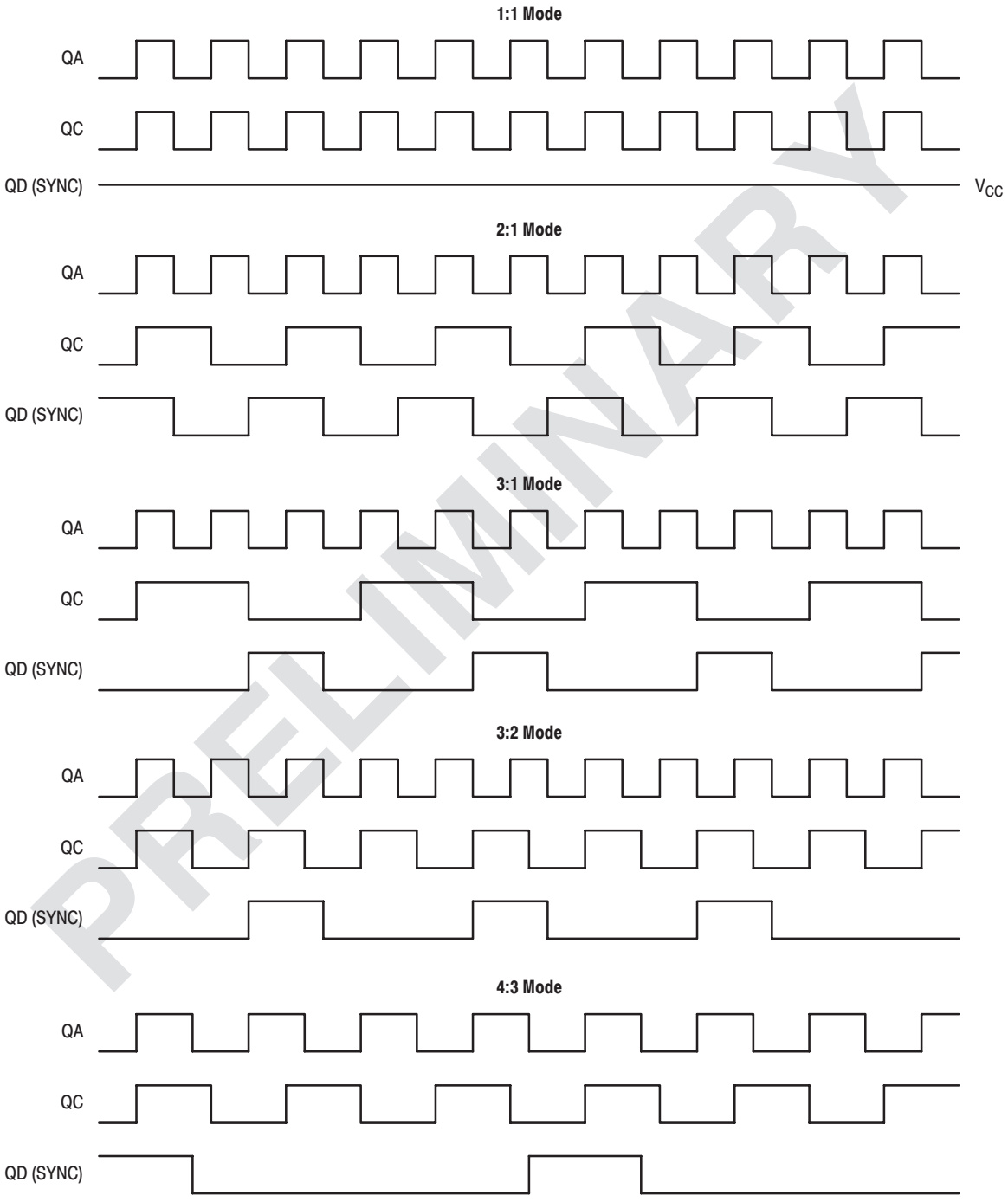



**Figure 3. QSYNC Timing Diagram**

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**Power Supply Filtering**

The MPC9992 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the $V_{CC\_PLL}$ power supply impacts the device characteristics, for instance I/O jitter. The MPC9992 provides separate power supplies for the output buffers ($V_{CC}$) and the phase-locked loop ($V_{CC\_PLL}$) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the $V_{CC\_PLL}$ pin for the MPC9992. Figure 4 illustrates a typical power supply filter scheme. The MPC9992 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor $R_F$. From the data sheet the $I_{CC\_PLL}$ current (the current sourced through the $V_{CC\_PLL}$ pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V ($V_{CC}$=3.3V or $V_{CC}$=2.5V) must be maintained on the $V_{CC\_PLL}$ pin. The resistor $R_F$ shown in Figure 4 "$V_{CC\_PLL}$ Power Supply Filter" must have a resistance of 9-10Ω ($V_{CC}$=2.5V) to meet the voltage drop criteria.

The minimum values for $R_F$ and the filter capacitor $C_F$ are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 4 "$V_{CC\_PLL}$ Power Supply Filter", the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9992 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

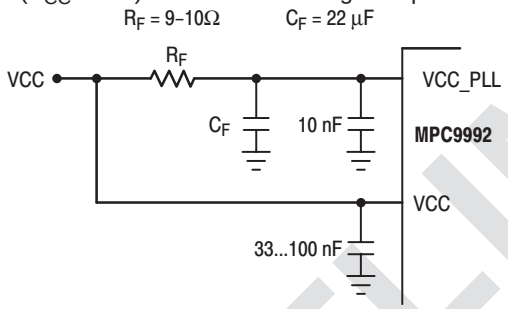



**Figure 4. $V_{CC\_PLL}$ Power Supply Filter**

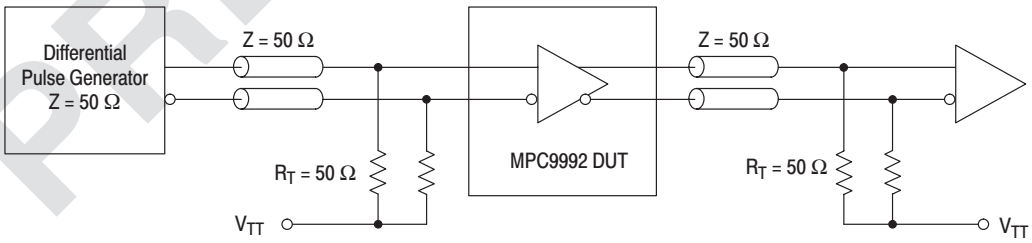



**Figure 5. MPC9992 AC test reference**

**Order Number: MPC9993/D**
**Rev 0, 12/2001**

**MPC9993**

2

*Product Preview*

# Intelligent Dynamic Clock Switch (IDCS) PLL Clock Driver

**FA SUFFIX**
32–LEAD LQFP PACKAGE
CASE 873A

The MPC9993 is a PLL clock driver designed specifically for redundant clock tree designs. The device receives two differential LVPECL clock signals from which it generates 5 new differential LVPECL clock outputs. Two of the output pairs regenerate the input signals frequency and phase while the other three pairs generate 2x, phase aligned clock outputs. External PLL feedback is used to also provide zero delay buffer performance.

**Features:**

- Fully Integrated PLL
- Intelligent Dynamic Clock Switch
- LVPECL Clock Outputs
- LVCMOS Control I/O
- 3.3V Operation
- 32–Lead LQFP Packaging
- SiGe technology supports near-zero output skew

**Functional Description**

The MPC9993 Intelligent Dynamic Clock Switch (IDCS) circuit continuously monitors both input CLK signals. Upon detection of a failure (CLK stuck HIGH or LOW for at least 1 period), the INP_BAD for that CLK will be latched (H). If that CLK is the primary clock, the IDCS will switch to the good secondary clock and phase/frequency alignment will occur with minimal output phase disturbance. The typical phase bump caused by a failed clock is eliminated. (See Application Information section).

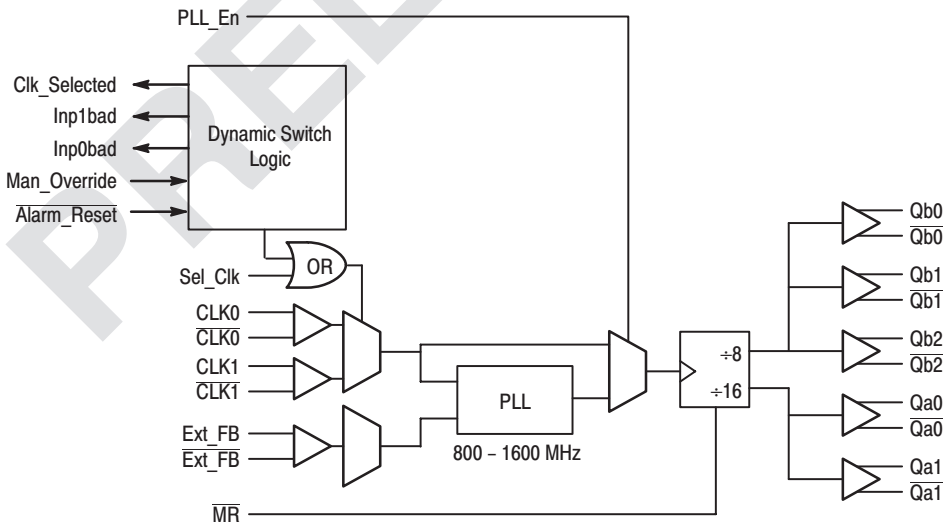



**Figure 1. Block Diagram**



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.
**Rev 0**

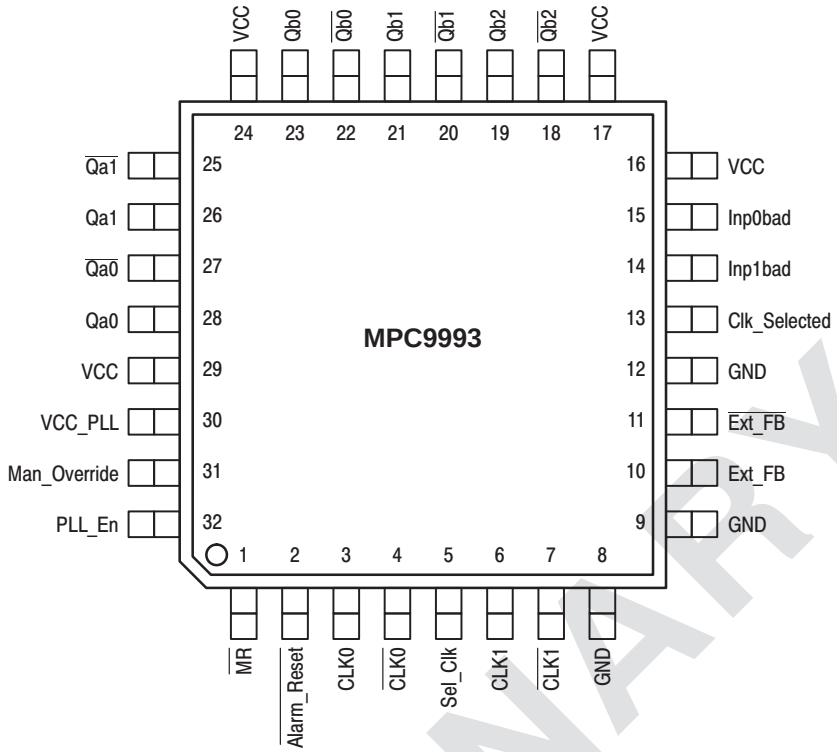



**Figure 2. 32–Lead Pinout** (Top View)



**PIN DESCRIPTIONS**

| Pin Name | I/O | Pin Definition |
|---|---|---|
| CLK0, $\overline{\text{CLK0}}$<br>CLK1, $\overline{\text{CLK1}}$ | LVPECL Input<br>LVPECL Input | Differential PLL clock reference (CLK0 pulldown, $\overline{\text{CLK0}}$ pullup)<br>Differential PLL clock reference (CLK1 pulldown, $\overline{\text{CLK1}}$ pullup) |
| Ext_FB, $\overline{\text{Ext\_FB}}$ | LVPECL Input | Differential PLL feedback clock (Ext_FB pulldown, $\overline{\text{Ext\_FB}}$ pullup) |
| Qa0:1, $\overline{\text{Qa0:1}}$ | LVPECL Output | Differential 1x output pairs |
| Qb0:2, $\overline{\text{Qb0:2}}$ | LVPECL Output | Differential 2x output pairs |
| Inp0bad | LVCMOS Output | Indicates detection of a bad input reference clock 0 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted |
| Inp1bad | LVCMOS Output | Indicates detection of a bad input reference clock 1 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted |
| Clk_Selected | LVCMOS Output | '0' if clock 0 is selected, '1' if clock 1 is selected |
| $\overline{\text{Alarm\_Reset}}$ | LVCMOS Input | '0' will reset the input bad flags and align Clk_Selected with Sel_Clk. The input is "one–shotted" (50kΩ pullup) |
| Sel_Clk | LVCMOS Input | '0' selects CLK0, '1' selects CLK1 (50kΩ pulldown) |
| Manual_Override | LVCMOS Input | '1' disables internal clock switch circuitry (50kΩ pulldown) |
| PLL_En | LVCMOS Input | '0' bypasses selected input reference around the phase–locked loop (50kΩ pullup) |
| $\overline{\text{MR}}$ | LVCMOS Input | '0' resets the internal dividers forcing Q outputs LOW. Asynchronous to the clock (50kΩ pullup) |
| VCCA | Power Supply | PLL power supply |
| VCC | Power Supply | Digital power supply |
| GNDA | Power Supply | PLL ground |
| GND | Power Supply | Digital ground |

## ABSOLUTE MAXIMUM RATINGS[a]

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -65 | 125 | °C | |

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

## GENERAL SPECIFICATIONS

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output termination voltage | | $V_{CC}$ - 2 | | V | |
| MM | ESD Protection (Machine model) | TBD | | | V | |
| HBM | ESD Protection (Human body model) | TBD | | | V | |
| CDM | ESD Protection (Charged device model | TBD | | | V | |
| LU | Latch-up immunity | 200 | | | mA | |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | Inputs |
| $\theta_{JA}$ | Thermal resistance junction to ambient | | | | | |
| | JESD 51-3, single layer test board | | 83.1 | 86.0 | °C/W | Natural convection |
| | | | 73.3 | 75.4 | °C/W | 100 ft/min |
| | | | 68.9 | 70.9 | °C/W | 200 ft/min |
| | | | 63.8 | 65.3 | °C/W | 400 ft/min |
| | | | 57.4 | 59.6 | °C/W | 800 ft/min |
| | JESD 51-6, 2S2P multilayer test board | | 59.0 | 60.6 | °C/W | Natural convection |
| | | | 54.4 | 55.7 | °C/W | 100 ft/min |
| | | | 52.5 | 53.8 | °C/W | 200 ft/min |
| | | | 50.4 | 51.5 | °C/W | 400 ft/min |
| | | | 47.8 | 48.8 | °C/W | 800 ft/min |
| $\theta_{JC}$ | Thermal resistance junction to case | | 23.0 | 26.3 | °C/W | MIL-SPEC 883E Method 1012.1 |
| | Operating junction temperature[a] (continuous operation) MTBF = 9.1 years | | | 110 | °C | |

a. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6226 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6226 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

**DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40° to +85°C)[a]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| LVCMOS control inputs ($\overline{OE}$, FSEL0, FSEL1, MR) | | | | | | |
| $V_{IL}$ | Input voltage low | | | 0.8 | V | |
| $V_{IH}$ | Input voltage high | 2.0 | | | V | |
| $I_{IN}$ | Input Current[b] | | | ±TBD | µA | $V_{IN}$ = $V_{CC}$ or $V_{IN}$ = GND |
| LVPECL clock inputs (CLK, $\overline{CLK}$)[c] | | | | | | |
| $V_{PP}$ | AC differential input voltage[d] | 0.1 | | 1.3 | V | Differential operation |
| $V_{CMR}$ | Differential cross point voltage[e] | 1.0 | | $V_{CC}$-0.3 | V | Differential operation |
| $V_{IH}$ | Input high voltage | TBD | | TBD | | |
| $V_{IL}$ | Input low voltage | TBD | | TBD | | |
| $I_{IN}$ | Input Current | | | ±TBD | µA | $V_{IN}$ = TBD or $V_{IN}$ = TBD |
| LVPECL clock outputs (QA0-4, $\overline{QA0\text{-}4}$, QB0-4, $\overline{QB0\text{-}4}$) | | | | | | |
| $V_{OH}$ | Output High Voltage | TBD | $V_{CC}$-1.005 | TBD | V | Termination 50Ω to $V_{TT}$ |
| $V_{OL}$ | Output Low Voltage | TBD | $V_{CC}$-1.705 | TBD | V | Termination 50Ω to $V_{TT}$ |
| | | | | | | |
| $I_{CC}$ | Maximum Power Supply VCC pins | | | TBD | mA | |
| $I_{CCA}$ | Maximum PLL Power Supply VCC_PLL pin | | | TBD | mA | |

a. AC characterisitics are design targets and pending characterization.
b. Input have internal pullup/pulldown resistors which affect the input current.
c. Clock inputs driven by LVPECL compatible signals.
d. $V_{PP}$ is the minimum differential input voltage swing required to maintain AC characteristic.
e. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.

**AC CHARACTERISTICS** ($T_A$ = –40°C to 85°C, $V_{CC}$ = 3.3V ± 5%) (Note 5.)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{VCO}$ | PLL VCO Lock Range | 800 | | 1600 | MHz |
| $t_{pwi}$ | | 25 | | 75 | % |
| $t_{pd}$ | Propagation Delay (Note 1.) CLKn to Q (Bypass)<br>CLKn to Ext_FB (Locked (Note 2.)) | | | TBD<br>TBD | ns<br>ps |
| $V_{PP}$ | Differential input voltage (peak-to-peak) | | 0.3 | 1.3 | V |
| $V_{CMR}$ | Differential input crosspoint voltage | | | $V_{CC}$-0.3 | V |
| $t_r/t_f$ | Output Rise/Fall Time | | | TBD | ps |
| $t_{skew}$ | Output Skew Within Bank<br>All Outputs | | | 35<br>50 | ps |
| $\Delta_{pe}$ | Maximum Phase Error Deviation | | | TBD (Note 3.)<br>TBD (Note 4.) | ps |
| $\Delta_{per/cycle}$ | Rate of Change of Periods 75MHz Output (Note 1., 3.)<br>150MHz Output (Note 1., 3.)<br>75MHz Output (Note 1., 4.)<br>150MHz Output (Note 1., 4.) | | 20<br>10<br>200<br>100 | 50<br>25<br>400<br>200 | ps/cycle |
| $t_{pw}$ | Output Duty Cycle | 45 | | 55 | % |
| $t_{jitter}$ | Cycle–to–Cycle Jitter, Standard Deviation (RMS) (Note 1.) | | | 20 | ps |
| $t_{lock}$ | Maximum PLL Lock Time | | | 10 | ms |

1. Guaranteed, not production tested.
2. Static phase offset between the selected reference clock and the feedback signal.
3. Specification holds for a clock switch between two signals no greater than 400ps out of phase. Delta period change per cycle is averaged over the clock switch excursion. (See Applications Information section on page 311 for more detail)
4. Specification holds for a clock switch between two signals no greater than ±π out of phase. Delta period change per cycle is averaged over the clock switch excursion.
5. PECL output termination is 50 ohms to $V_{CC}$ – 2.0V.

## APPLICATIONS INFORMATION

The MPC9993 is a dual clock PLL with on–chip Intelligent Dynamic Clock Switch (IDCS) circuitry.

### Definitions

**primary clock:** The input CLK selected by Sel_Clk.
**secondary clock:** The input CLK NOT selected by Sel_Clk.
**PLL reference signal:** The CLK selected as the PLL reference signal by Sel_Clk or IDCS. (IDCS can override Sel_Clk).

### Status Functions

**Clk_Selected:** Clk_Selected (L) indicates CLK0 is selected as the PLL reference signal. Clk_Selected (H) indicates CLK1 is selected as the PLL reference signal.
**INP_BAD:** Latched (H) when it's CLK is stuck (H) or (L) for at least one Ext_FB period (Pos to Pos or Neg to Neg). Cleared (L) on assertion of $\overline{\text{Alarm\_Reset}}$.

### Control Functions

**Sel_Clk:** Sel_Clk (L) selects CLK0 as the primary clock. Sel_Clk (H) selects CLK1 as the primary clock.
**$\overline{\text{Alarm\_Reset}}$:** Asserted by a negative edge. Generates a one–shot reset pulse that clears INPUT_BAD latches and Clk_Selected latch.
**PLL_En:** While (L), the PLL reference signal is substituted for the VCO output.
**$\overline{\text{MR}}$:** While (L), internal dividers are held in reset which holds all Q outputs LOW.

### Man Override (H)

(IDCS is disabled, PLL functions normally). PLL reference signal (as indicated by Clk_Selected) will always be the CLK selected by Sel_Clk. The status function INP_BAD is active in Man Override (H) and (L).

### Man Override (L)

(IDCS is enabled, PLL functions enhanced). The first CLK to fail will latch it's INP_BAD (H) status flag and select the other input as the Clk_Selected for the PLL reference clock. Once latched, the Clk_Selected and INP_BAD remain latched until assertion of $\overline{\text{Alarm\_Reset}}$ which clears all latches (INP_BADs are cleared and Clk_Selected = Sel_Clk). NOTE: If both CLKs are bad when $\overline{\text{Alarm\_Reset}}$ is asserted, both INP_BADs will be latched (H) after one Ext_FB period and Clk_Selected will be latched (L) indicating CLK0 is the PLL reference signal. While neither INP_BAD is latched (H), the Clk_Selected can be freely changed with Sel_Clk. Whenever a CLK switch occurs, (manually or by IDCS), following the next negative edge of the newly selected PLL reference signal, the next positive edge pair of Ext_FB and the newly selected PLL reference signal will slew to alignment.

To calculate the overall uncertainty between the input CLKs and the outputs from multiple MPC9993's, the following procedure should be used. Assuming that the input CLKs to all MPC9993's are exactly in phase, the total uncertainty will be the sum of the static phase offset, max I/O jitter, and output to output skew.

During a dynamic switch, the output phase between two devices may be increased for a short period of time. If the two input CLKs are 400ps out of phase, a dynamic switch of an MPC9993 will result in an instantaneous phase change of 400ps to the PLL reference signal without a corresponding change in the output phase (due to the limited response of the PLL). As a result, the I/O phase of a device, undergoing this switch, will initially be 400ps and diminish as the PLL slews to its new phase alignment. This transient timing issue should be considered when analyzing the overall skew budget of a system.

### Hot insertion and withdrawal

In PECL applications, a powered up driver will experience a low impedance path through an MPC9993 input to its powered down VCC pins. In this case, a 100 ohm series resistance should be used in front of the input pins to limit the driver current. The resistor will have minimal impact on the rise and fall times of the input signals.

### Acquiring Frequency Lock

1. While the MPC9993 is receiving a valid CLK signal, assert Man_Override HIGH.
2. The PLL will phase and frequency lock within the specified lock time.
3. Apply a HIGH to LOW transition to Alarm_Reset to reset Input Bad flags.
4. De–assert Man_Override LOW to enable Intelligent Dynamic Clock Switch mode.

# Chapter Three
# Clock Synthesizer Data Sheets

3

**Clock Synthesizer Device Index**

# High Frequency Clock Synthesizer

**MC12429**

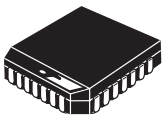
**See Upgrade Product – MPC9229**

**HIGH FREQUENCY PLL CLOCK SYNTHESIZER**



The MC12429 is a general purpose synthesized clock source. Its internal VCO will operate over a range of frequencies from 200 to 400MHz. The differential PECL output can be configured to be the VCO frequency divided by 1, 2, 4, or 8. With the output configured to divide the VCO frequency by 1, and with a 16.000MHz external quartz crystal used to provide the reference frequency, the output frequency can be specified in 1MHz steps. The PLL loop filter is fully integrated so that no external components are required. The output frequency is configured using a parallel or serial interface.

- 25 to 400MHz Differential PECL Outputs
- ±25 ps Peak–to–Peak Output Jitter
- Fully Integrated Phase–Locked Loop
- Minimal Frequency Over–Shoot
- Synthesized Architecture
- Serial 3–Wire Interface
- Parallel Interface for Power–Up
- Quartz Crystal Interface
- 28–Lead PLCC and 32–Lead LQFP Packages
- Operates from 3.3V or 5.0V Power Supply



**FN SUFFIX**
28–LEAD PLCC PACKAGE
CASE 776–02

**FA SUFFIX**
32–LEAD LQFP PACKAGE
CASE 873A–02

**Functional Description**

The internal oscillator uses the external quartz crystal as the basis of its frequency reference. The output of the reference oscillator is divided by 16 before being sent to the phase detector. With a 16MHz crystal, this provides a reference frequency of 1MHz. Although this data sheet illustrates functionality only for a 16MHz crystal, any crystal in the 10–25MHz range can be used.

The VCO within the PLL operates over a range of 200 to 400MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The output of this loop divider is also applied to the phase detector.

The phase detector and loop filter attempt to force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve loop lock.

The output of the VCO is also passed through an output divider before being sent to the PECL output driver. This output divider (N divider) is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle.

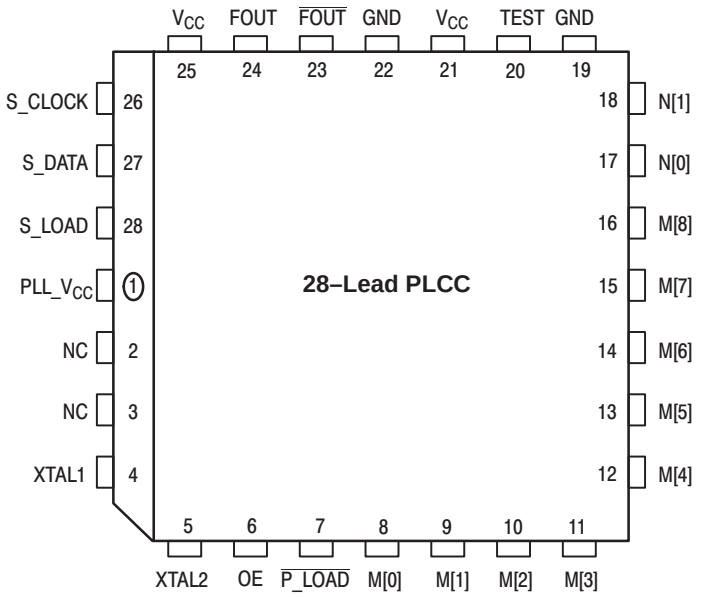
The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated in 50Ω to $V_{CC}$ – 2.0V. The positive reference for the output driver and the internal logic is separated from the power supply for the phase–locked loop to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. Normally, on system reset, the $\overline{\text{P\_LOAD}}$ input is held LOW until sometime after power becomes valid. On the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[8:0] and N[1:0] inputs to reduce component count in the application of the chip.

The serial interface centers on a fourteen bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH–to–LOW edge of the S_LOAD input. See the programming section for more information.

The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. See the programming section for more information.

**Rev 7**




| N[1:0] | Output Division |
|---|---|
| 0 0 | 1 |
| 0 1 | 2 |
| 1 0 | 4 |
| 1 1 | 8 |

**Figure 1. 28–Lead** (Top View)

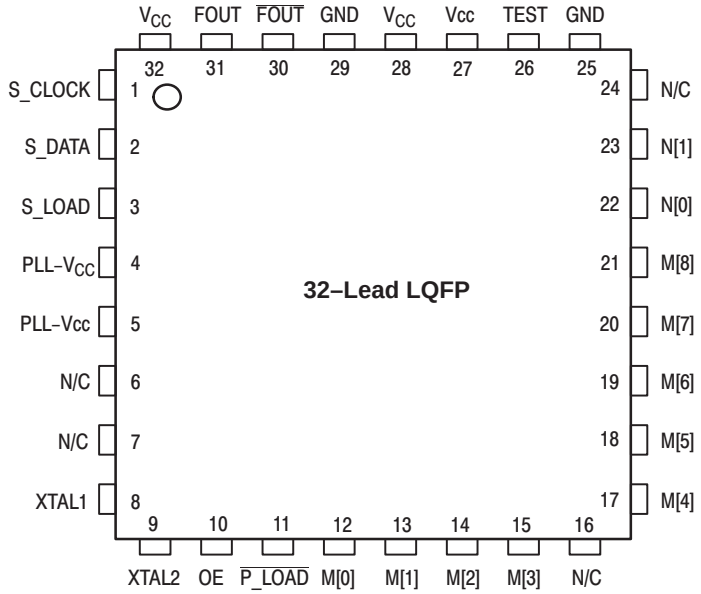



**Figure 2. 32–Lead Pinout** (Top View)

**PIN DESCRIPTIONS**

| Pin Name | Function |
|---|---|
| **Inputs** | |
| XTAL1, XTAL2 | These pins form an oscillator when connected to an external series–resonant crystal. |
| S_LOAD<br>(Int. Pulldown) | This pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH, thus the data must be stable on the HIGH–to–LOW transition of S_LOAD for proper operation. |
| S_DATA<br>(Int. Pulldown) | This pin acts as the data input to the serial configuration shift registers. |
| S_CLOCK<br>(Int. Pulldown) | This pin serves to clock the serial configuration shift registers. Data from S_DATA is sampled on the rising edge. |
| $\overline{\text{P\_LOAD}}$<br>(Int. Pullup) | This pin loads the configuration latches with the contents of the parallel inputs .The latches will be transparent when this signal is LOW, thus the parallel data must be stable on the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$ for proper operation. $\overline{\text{P\_LOAD}}$ is state sensitive. |
| M[8:0]<br>(Int. Pullup) | These pins are used to configure the PLL loop divider. They are sampled on the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$. M[8] is the MSB, M[0] is the LSB. |
| N[1:0]<br>(Int. Pullup) | These pins are used to configure the output divider modulus. They are sampled on the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$. |
| OE<br>(Int. Pullup) | Active HIGH Output Enable. The Enable is synchronous to eliminate possibility of runt pulse generation on the $F_{OUT}$ output. |
| **Outputs** | |
| $F_{OUT}$, $\overline{F_{OUT}}$ | These differential positive–referenced ECL signals (PECL) are the output of the synthesizer. |
| TEST | The function of this output is determined by the serial configuration bits T[2:0]. |
| **Power** | |
| $V_{CC}$ | This is the positive supply for the internal logic and the output buffer of the chip, and is connected to +3.3V or 5.0V ($V_{CC}$ = PLL_$V_{CC}$). Current drain through $V_{CC} \approx$ 85mA. |
| PLL_$V_{CC}$ | This is the positive supply for the PLL, and should be as noise–free as possible for low–jitter operation. This supply is connected to +3.3V or 5.0V ($V_{CC}$ = PLL_$V_{CC}$). Current drain through PLL_$V_{CC} \approx$ 15mA. |
| GND | These pins are the negative supply for the chip and are normally all connected to ground. |

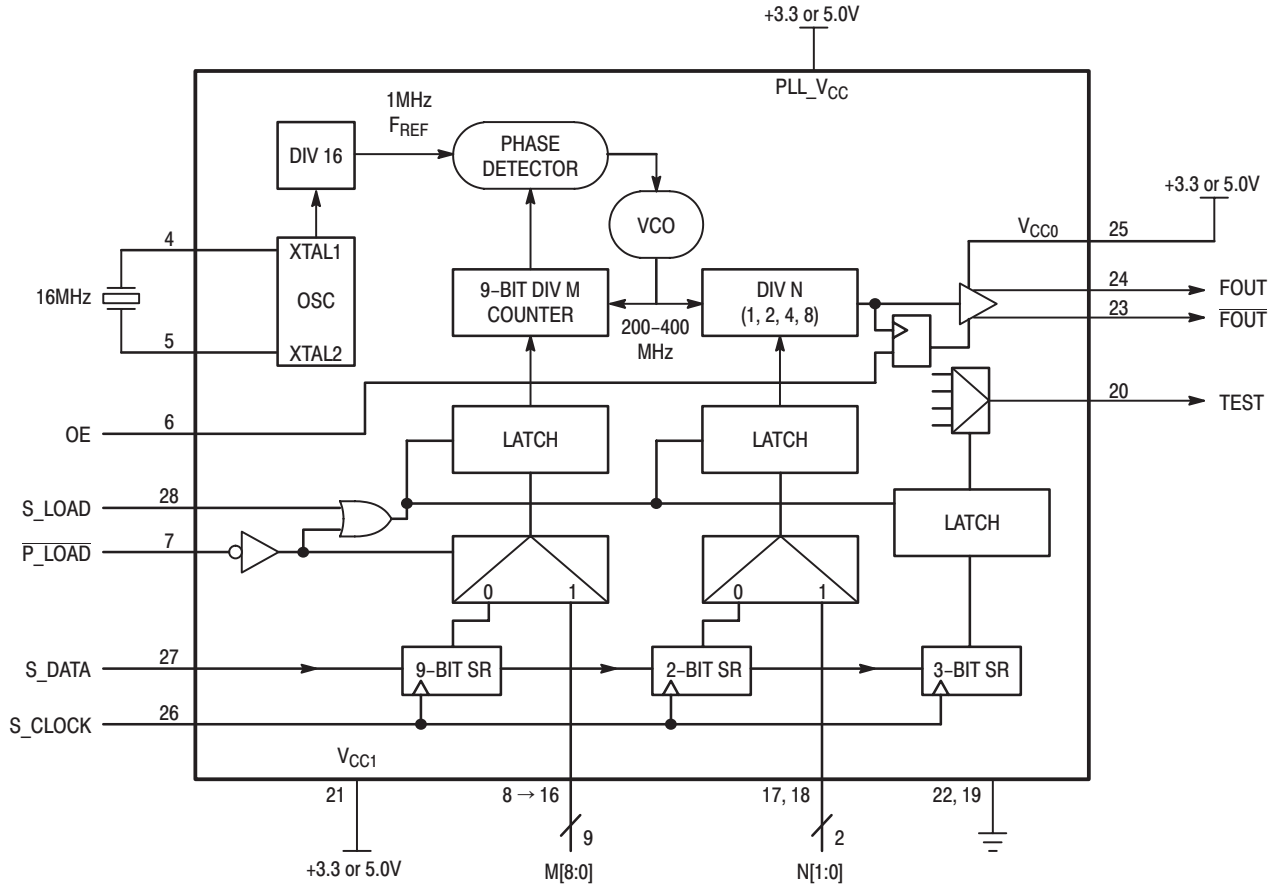



**Figure 3. MC12429 Block Diagram (28–Lead PLCC Pinout)**

3

## PROGRAMMING INTERFACE

Programming the device amounts to properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can by represented by this formula:

$$FOUT = (F_{XTAL} \div 16) \times M \div N \qquad (1)$$

Where $F_{XTAL}$ is the crystal frequency, M is the loop divider modulus, and N is the output divider modulus. Note that it is possible to select values of M such that the PLL is unable to achieve loop lock. To avoid this, always make sure that M is selected to be $200 \leq M \leq 400$ for a 16MHz input reference.

Assuming that a 16MHz reference frequency is used the above equation reduces to:

$$FOUT = M \div N$$

Substituting the four values for N (1, 2, 4, 8) yields:

**TABLE A: Output Frequency Range**

| N | $F_{OUT}$ | OUTPUT FREQUENCY RANGE |
|---|---|---|
| 1 | M | 200 – 400 MHZ |
| 2 | M / 2 | 100 – 200 MHZ |
| 4 | M / 4 | 50 – 100 MHZ |
| 8 | M / 8 | 25 – 50 MHZ |

From these ranges the user will establish the value of N required, then the value of M can be calculated based on the appropriate equation above. For example if an output frequency of 131MHz was desired the following steps would be taken to identify the appropriate M and N values. 131MHz falls within the frequency range set by an N value of 2 so N [1:0] = 01. For N = 2 FOUT = M ÷ 2 and M = 2 x FOUT. Therefore M = 131 x 2 = 262, so M[8:0] = 100000110. Following this same procedure a user can generate any whole frequency desired between 25 and 400MHz. Note that for N > 2 fractional values of FOUT can be realized. The size of the programmable frequency steps (and thus the indicator of the fractional output frequencies acheivable) will be equal to FXTAL ÷ 16 ÷ N.

For input reference frequencies other than 16MHz the set of appropriate equations can be deduced from equation 1. For computer applications another useful frequency base would be 16.666MHz. From this reference one can generate a family of output frequencies at multiples of the 33.333MHz PCI clock. As an example to generate a 133.333MHz clock from a 16.666MHz reference the following M and N values would be used:

$$FOUT = 16.666 \div 16 \times M \div N = 1.0416 \times M \div N$$

$$\text{Let } N = 2, \quad M = 133.3333 \div 1.0416 \times 2 = 256$$

The value for M falls within the constraints set for PLL stability, therefore N[1:0] = 01 and M[8:0} = 10000000. If the value for M

fell outside of the valid range a different N value would be selected to try to move M in the appropriate direction.

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the $\overline{\text{P\_LOAD}}$ signal such that a LOW to HIGH transition will latch the information present on the M[8:0] and N[1:0] inputs into the M and N counters. When the $\overline{\text{P\_LOAD}}$ signal is LOW the input latches will be transparent and any changes on the M[8:0] and N[1:0] inputs will affect the FOUT output pair. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 14 bit shift register. Note that the $\overline{\text{P\_LOAD}}$ signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1 and M8). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 4 illustrates the timing diagram for both a parallel and a serial load of the MC12429 synthesizer.

M[8:0] and N[1:0] are normally specified once at power–up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine–tune the clock as the ability to control the serial interface becomes available.

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents FOUT, the CMOS output may not be able to toggle fast enough for some of the higher output frequencies. The T2, T1 and T0 control bits are preset to ‘000’ when $\overline{\text{P\_LOAD}}$ is LOW so that the PECL FOUT outputs are as jitter–free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Most of the signals available on the TEST output pin are useful only for performance verification of the MC12429 itself. However the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MC12429 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the FOUT differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clock tree. Figure 5 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 250MHz or less. This means the fastest the FOUT pin can be toggled via the S_CLOCK is 125MHz as the minimum divide ratio of the N counter is 2. Note that the M counter output on the TEST output will not be a 50% duty cycle due to the way the divider is implemented.

| **T2** | **T1** | **T0** | **TEST** (Pin 20) |
|---|---|---|---|
| 0 | 0 | 0 | SHIFT REGISTER OUT |
| 0 | 0 | 1 | HIGH |
| 0 | 1 | 0 | FREF |
| 0 | 1 | 1 | M COUNTER OUT |
| 1 | 0 | 0 | FOUT |
| 1 | 0 | 1 | LOW |
| 1 | 1 | 0 | MCNT |
| 1 | 1 | 1 | FOUT/4 |

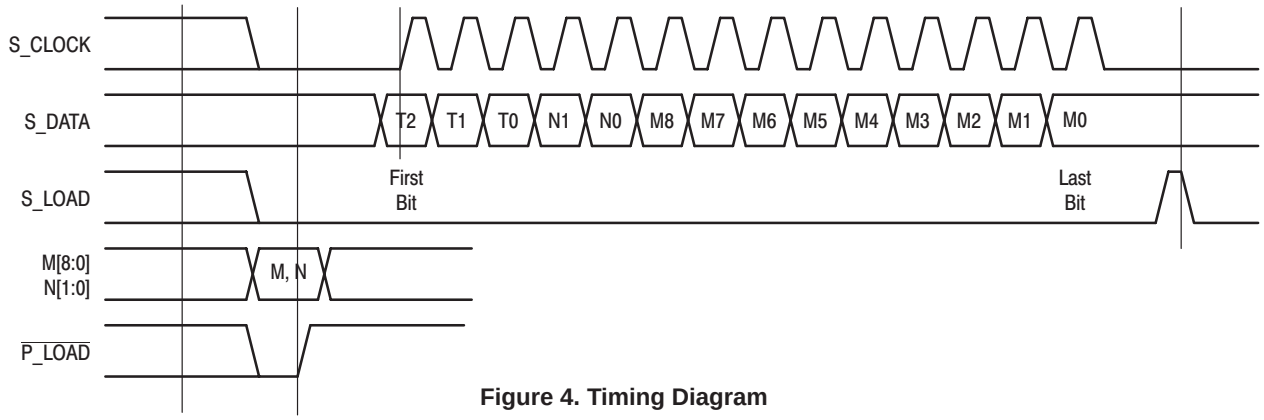
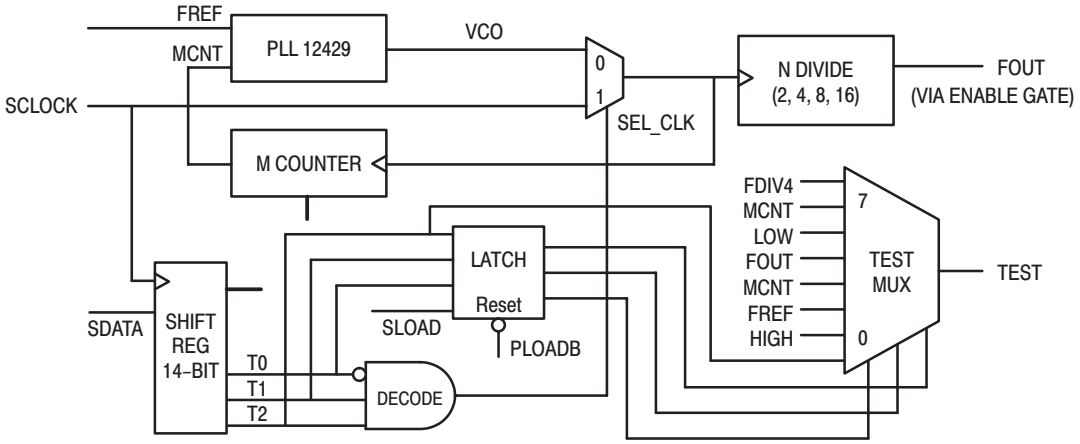



**Figure 4. Timing Diagram**




- T2=T1=1, T0=0: Test Mode (PLL bypass)
- SCLOCK is selected, MCNT is on TEST output, SCLOCK DIVIDE BY N is on FOUT pin

PLOADB acts as reset for test pin latch. When latch reset T2 data is shifted out TEST pin.

**Figure 5. Serial Test Clock Block Diagram (PLL bypass)**

3

**DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ±5%)

| | | 0°C | | | 25°C | | | 70°C | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** | **Condition** |
| $V_{IH}$ | Input HIGH Voltage | 2.2 | | | 2.2 | | | 2.2 | | | V | |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | | | 0.8 | | | 0.8 | V | |
| $I_{IN}$ | Input Current | | | 1.0 | | | 1.0 | | | 1.0 | mA | |
| $V_{OH}$ | Output HIGH Voltage TEST | 2.5 | | | 2.5 | | | 2.5 | | | V | $I_{OH}$ = –0.8mA |
| $V_{OL}$ | Output LOW Voltage TEST | | | 0.4 | | | 0.4 | | | 0.4 | V | $I_{OL}$ = 0.8mA |
| $V_{OH}$ | Output HIGH Voltage[1.] FOUT, $\overline{FOUT}$ | 2.28 | | 2.60 | 2.32 | | 2.49 | 2.38 | | 2.565 | V | $V_{CCO}$ = 3.3V[2.] |
| $V_{OL}$ | Output LOW Voltage[1.] FOUT, $\overline{FOUT}$ | 1.35 | | 1.67 | 1.35 | | 1.67 | 1.35 | | 1.70 | V | $V_{CCO}$ = 3.3V[2.] |
| $I_{CC}$ | Power Supply Current $V_{CC}$<br>PLL_$V_{CC}$ | | 85<br>15 | 100<br>20 | | 85<br>15 | 100<br>20 | | 85<br>15 | 100<br>20 | mA | |

1. 50Ω to $V_{CC}$ – 2.0V termination.
2. Output levels will vary 1:1 with $V_{CC0}$ variation.

**DC CHARACTERISTICS** ($V_{CC}$ = 5.0V ±5%)

| | | 0°C | | | 25°C | | | 70°C | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** | **Condition** |
| $V_{IH}$ | Input HIGH Voltage | 3.5 | | | 3.5 | | | 3.5 | | | V | |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | | | 0.8 | | | 0.8 | V | |
| $I_{IN}$ | Input Current | | | 1.0 | | | 1.0 | | | 1.0 | mA | |
| $V_{OH}$ | Output HIGH Voltage TEST | 2.5 | | | 2.5 | | | 2.5 | | | V | $I_{OH}$ = –0.8mA |
| $V_{OL}$ | Output LOW Voltage TEST | | | 0.4 | | | 0.4 | | | 0.4 | V | $I_{OL}$ = 0.8mA |
| $V_{OH}$ | Output HIGH Voltage[1.] FOUT, $\overline{FOUT}$ | 3.98 | | 4.30 | 4.02 | | 4.19 | 4.08 | | 4.265 | V | $V_{CCO}$ = 5.0V[2.] |
| $V_{OL}$ | Output LOW Voltage[1.] FOUT, $\overline{FOUT}$ | 3.05 | | 3.37 | 3.05 | | 3.37 | 3.05 | | 3.40 | V | $V_{CCO}$ = 5.0V[2.] |
| $I_{CC}$ | Power Supply Current $V_{CC}$<br>PLL_$V_{CC}$ | | 85<br>15 | 100<br>20 | | 85<br>15 | 100<br>20 | | 85<br>15 | 100<br>20 | mA | |

1. 50Ω to $V_{CC}$ – 2.0V termination.
2. Output levels will vary 1:1 with $V_{CC0}$ variation.

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V to 5.0V ±5%)

| Symbol | Characteristic | | Min | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $F_{MAXI}$ | Maximum Input Frequency | S_CLOCK<br>Xtal Oscillator | <br>10 | 10<br>20 | MHz | Note 3. |
| $F_{MAXO}$ | Maximum Output Frequency | VCO (Internal)<br>FOUT | 200<br>25 | 400<br>400 | MHz | Note 4. |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 10 | ms | |
| $t_{jitter}$ | Period Deviation (Peak–to–Peak) | | | ±25 | ps | Note 4.,<br>See Applications Section |
| $t_s$ | Setup Time | S_DATA to S_CLOCK<br>S_CLOCK to S_LOAD<br>M, N to $\overline{P\_LOAD}$ | 20<br>20<br>20 | | ns | |
| $t_h$ | Hold Time | S_DATA to S_CLOCK<br>M, N to $\overline{P\_LOAD}$ | 20<br>20 | | ns | |
| $tpw_{MIN}$ | Minimum Pulse Width | S_LOAD<br>$\overline{P\_LOAD}$ | 50<br>50 | | ns | Note 4. |
| $t_r$, $t_f$ | Output Rise/Fall | FOUT | 300 | 800 | ps | 20%–80%, Note 4. |

3. 10MHz is the maximum frequency to load the feedback devide registers. S_CLOCK can be switched at higher frequencies when used as a test clock in TEST_MODE 6.
4. 50Ω to $V_{CC}$ – 2.0V pulldown.

## APPLICATIONS INFORMATION

### Using the On–Board Crystal Oscillator

The MC12429 features a fully integrated on–board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MC12429 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required. Because the series resonant design is affected by capacitive loading on the xtal terminals loading variation introduced by crystals from different vendors could be a potential issue. For crystals with a higher shunt capacitance it may be required to place a resistance across the terminals to suppress the third harmonic. Although typically not required it is a good idea to layout the PCB with the provision of adding this external resistor. The resistor value will typically be between 500 and 1KΩ.

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately most crystals are characterized in a parallel resonant mode. Fortunately there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result a parallel resonant crystal can be used with the MC12429 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application this level of inaccuracy is immaterial. Table 1 below specifies the performance requirements of the crystals to be used with the MC12429.

**Table 5. Recommended Crystal Specifications**

| Parameter | Value |
|---|---|
| Crystal Cut | Fundamental AT Cut |
| Resonance | Series Resonance* |
| Frequency Tolerance | ±75ppm at 25°C |
| Frequency/Temperature Stability | ±150pm 0 to 70°C |
| Operating Range | 0 to 70°C |
| Shunt Capacitance | 5–7pF |
| Equivalent Series Resistance (ESR) | 50 to 80Ω |
| Correlation Drive Level | 100μW |
| Aging | 5ppm/Yr (First 3 Years) |

* See accompanying text for series versus parallel resonant discussion.

### Power Supply Filtering

The MC12429 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MC12429 provides separate power supplies for the digital ciruitry ($V_{CC}$) and the internal PLL (PLL_VCC) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the PLL_VCC pin for the MC12429.

Figure 6 illustrates a typical power supply filter scheme. The MC12429 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the PLL_VCC pin of the MC12429. From the data sheet the $I_{PLL\_VCC}$ current (the current sourced through the PLL_VCC pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the PLL_VCC pin very little DC voltage drop can be tolerated when a 3.3V $V_{CC}$ supply is used. The resistor shown in Figure 6 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

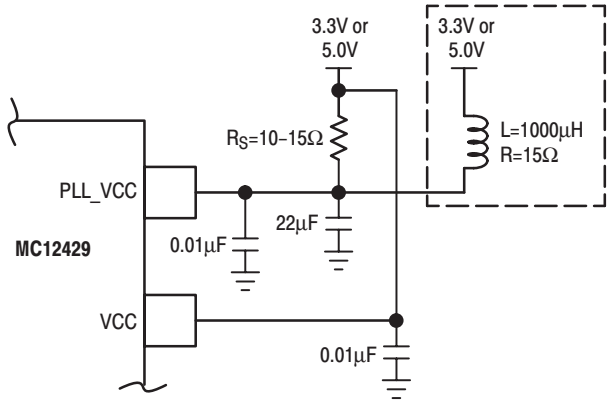



**Figure 6. Power Supply Filter**

A higher level of attenuation can be acheived by replacing the resistor with an appropriate valued inductor. Figure 6 shows a 1000μH choke, this value choke will show a significant impedance at 10KHz frequencies and above. Because of the current draw and the voltage that must be maintained on the PLL_VCC pin a low DC resistance inductor is required (less than 15Ω). Generally the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering.

The MC12429 provides sub–nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 7 shows a representaive board layout for the MC12429. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in

Figure 7 is the low impedance connections between VCC and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the 12429 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors.



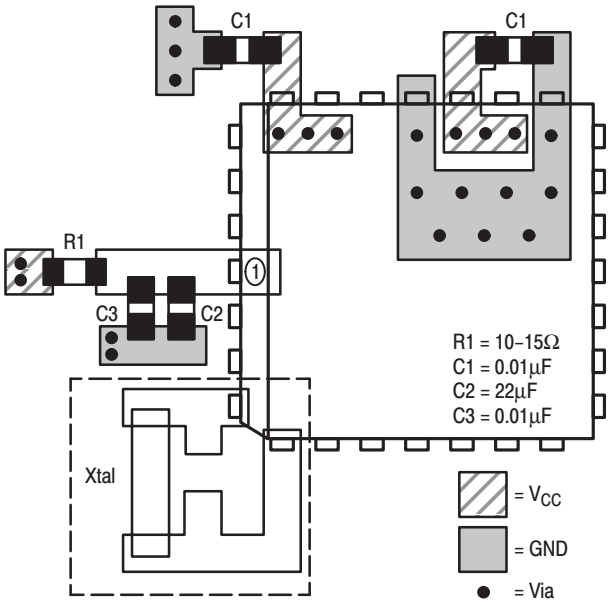



**Figure 7. PCB Board Layout for MC12429 (28 PLCC)**

Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on–board oscillator. Note the provisions for placing a resistor across the crystal oscillator terminals as discussed in the crystal oscillator section of this data sheet.

Although the MC12429 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Jitter Performance of the MC12429**

The MC12429 exhibits long term and cycle–to–cycle jitter which rivals that of SAW based oscillators. This jitter performance comes with the added flexibility one gets with a synthesizer over a fixed frequency oscillator.

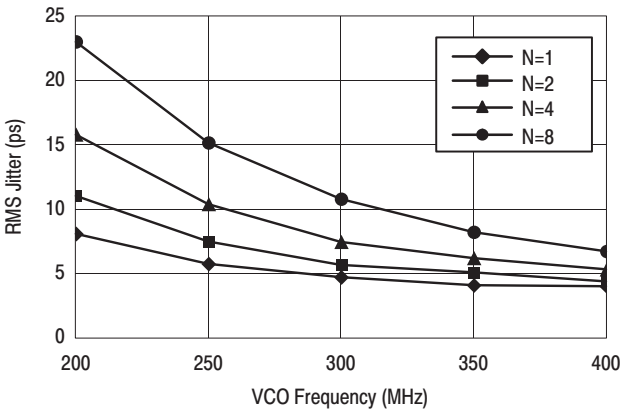



**Figure 8. RMS PLL Jitter versus VCO Frequency**

Figure 8 illustrates the RMS jitter performance of the MC12429 across its specified VCO frequency range. Note that the jitter is a function of both the output frequency as well as the VCO frequency, however the VCO frequency shows a much stronger dependence. The data presented has not been compensated for trigger jitter, this fact provides a measure of guardband to the reported data.

The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak–to–peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. All of the jitter data reported on the MC12429 was collected in this manner.

Figure 9 shows the jitter as a function of the output frequency. For the 12429 this information is probably of more importance. The flat line represents an RMS jitter value that corresponds to an 8 sigma ±25ps peak–to–peak long term period jitter. The graph shows that for output frequencies from 87.5 to 400MHz the jitter falls within the ±25ps peak–to–peak specification. The general trend is that as the output frequency is decreased the output edge jitter will increase.

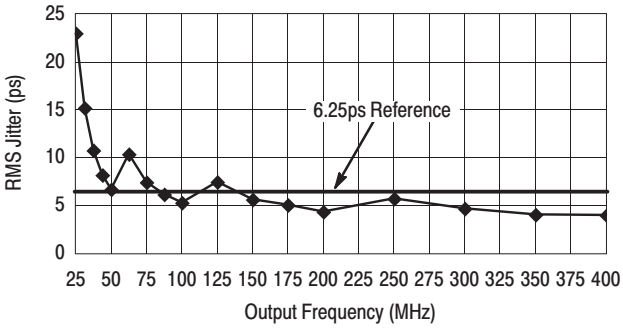



**Figure 9. RMS Jitter versus Output Frequency**

The jitter data presented should provide users with enough information to determine the effect on their overall timing budget. The jitter performance meets the needs of most system designs while adding the flexibility of frequency margining and field upgrades. These features are not available with a fixed frequency SAW oscillator.

**Order Number: MC12430/D**
**Rev. 5, 09/2001**

# High Frequency Clock Synthesizer

**MC12430**

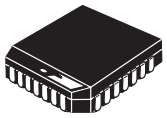
**See Upgrade Product – MPC9230**

**HIGH FREQUENCY PLL CLOCK SYNTHESIZER**



The MC12430 is a general purpose synthesized clock source. Its internal VCO will operate over a range of frequencies from 400 to 800 MHz. The differential PECL output can be configured to be the VCO frequency divided by 1, 2, 4 or 8. With the output configured to divide the VCO frequency by 2, and with a 16.000 MHz external quartz crystal used to provide the reference frequency, the output frequency can be specified in 1 MHz steps. The PLL loop filter is fully integrated so that no external components are required. The synthesizer output frequency is configured using a parallel or serial interface.

- 50 to 800 MHz Differential PECL Outputs
- ±25 ps Peak–to–Peak Output Jitter
- Fully Integrated Phase–Locked Loop
- Minimal Frequency Over–Shoot
- Synthesized Architecture
- Serial 3–Wire Interface
- Parallel Interface for Power–Up
- Quartz Crystal Interface
- 28–Lead PLCC and 32–Lead LQFP Packages
- Operates from 3.3 V or 5.0V Power Supply



**FN SUFFIX**
28–LEAD PLCC PACKAGE
CASE 776–02

**FA SUFFIX**
32–LEAD LQFP PACKAGE
CASE 873A–02

**Functional Description**

The internal oscillator uses the external quartz crystal as the basis of its frequency reference. The output of the reference oscillator is divided by 16 before being sent to the phase detector. With a 16 MHz crystal, this provides a reference frequency of 1 MHz. Although this data sheet illustrates functionality only for a 16 MHz crystal, any crystal in the 10–20 MHz range can be used.

The VCO within the PLL operates over a range of 400 to 800 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The output of this loop divider is applied to the phase detector.

The phase detector and loop filter attempt to force the VCO output frequency to be M x 2 times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve loop lock.

The output of the VCO is also passed through an output divider before being sent to the PECL output driver. This output divider (N divider) is configured through either the serial or the parallel interfaces and can provide one of four division ratios (1, 2, 4 or 8). This divider extends performance of the part while providing a 50% duty cycle.

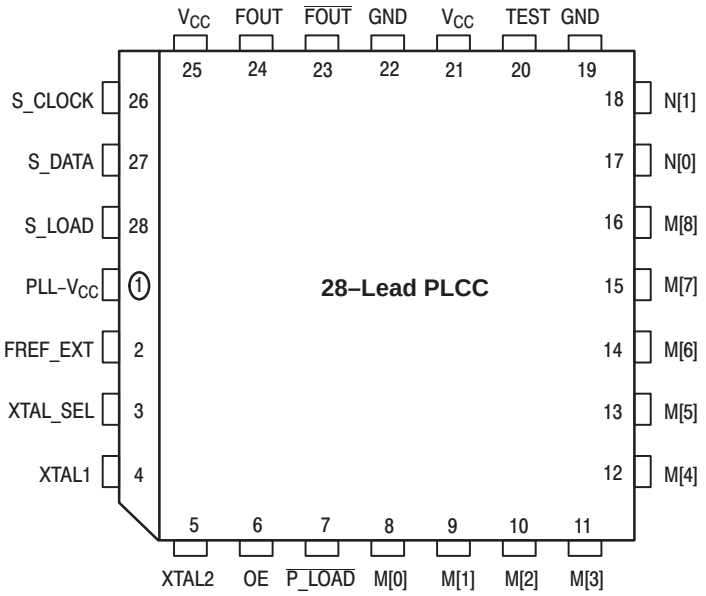
The output driver is driven differentially from the output divider and is capable of driving a pair of transmission lines terminated in 50Ω to $V_{CC}$ – 2.0 V. The positive reference for the output driver and the internal logic is separated from the power supply for the phase–locked loop to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. Normally, on system reset, the $\overline{\text{P\_LOAD}}$ input is held LOW until sometime after power becomes valid. On the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[8:0] and N[1:0] inputs to reduce component count in the application of the chip.

The serial interface centers on a fourteen bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH–to–LOW edge of the S_LOAD input. See the programming section for more information.

The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. See the programming section for more information.

**Rev 5**




| N[1:0] | Output Division |
|---|---|
| 0 0 | 2 |
| 0 1 | 4 |
| 1 0 | 8 |
| 1 1 | 1 |

| Input | 0 | 1 |
|---|---|---|
| XTAL_SEL<br>OE | FREF_EXT<br>Disabled | XTAL<br>Enabled |

**Figure 1. 28–Lead Pinout** (Top View)

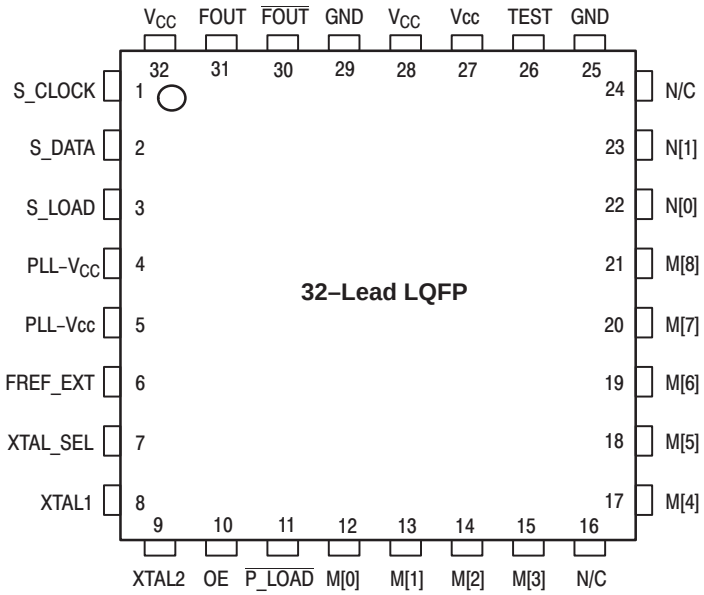



**Figure 2. 32–Lead Pinout** (Top View)

**PIN DESCRIPTIONS**

| Pin Name | Function |
|---|---|
| **Inputs** | |
| XTAL1, XTAL2 | These pins form an oscillator when connected to an external series–resonant crystal. |
| S_LOAD (Int. Pulldown) | This pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH, thus the data must be stable on the HIGH–to–LOW transition of S_LOAD for proper operation. |
| S_DATA (Int. Pulldown) | This pin acts as the data input to the serial configuration shift registers. |
| S_CLOCK (Int. Pulldown) | This pin serves to clock the serial configuration shift registers. Data from S_DATA is sampled on the rising edge. |
| $\overline{\text{P\_LOAD}}$ (Int. Pullup) | This pin loads the configuration latches with the contents of the parallel inputs .The latches will be transparent when this signal is LOW, thus the parallel data must be stable on the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$ for proper operation. $\overline{\text{P\_LOAD}}$ is state sensitive. |
| M[8:0] (Int. Pullup) | These pins are used to configure the PLL loop divider. They are sampled on the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$. M[8] is the MSB, M[0] is the LSB. |
| N[1:0] (Int. Pullup) | These pins are used to configure the output divider modulus. They are sampled on the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$. |
| OE (Int. Pullup) | Active HIGH Output Enable. The Enable is synchronous to eliminate possibility of runt pulse generation on the $F_{OUT}$ output. |
| **Outputs** | |
| $F_{OUT}$, $\overline{F_{OUT}}$ | These differential positive–referenced ECL signals (PECL) are the output of the synthesizer. |
| TEST | The function of this output is determined by the serial configuration bits T[2:0]. The output is single–ended ECL. |
| **Power** | |
| $V_{CC}$ | This is the positive supply for the internal logic and the output buffer of the chip, and is connected to +3.3V or 5.0V ($V_{CC}$ = PLL_$V_{CC}$). Current drain through $V_{CC} \approx 85$ mA. |
| PLL_$V_{CC}$ | This is the positive supply for the PLL, and should be as noise–free as possible for low–jitter operation. This supply is connected to +3.3V or 5.0V ($V_{CC}$ = PLL_$V_{CC}$). Current drain through PLL_$V_{CC} \approx 15$ mA. |
| GND | These pins are the negative supply for the chip and are normally all connected to ground. |
| **Other** | |
| FREF_EXT (Int. Pulldown) | LVCMOS/CMOS input which can be used as the PLL reference. |
| XTAL_SEL (Int. Pullup) | LVCMOS/CMOS input that selects between the crystal and the FREF_EXT source for the PLL reference signal. A HIGH selects the crystal input. |

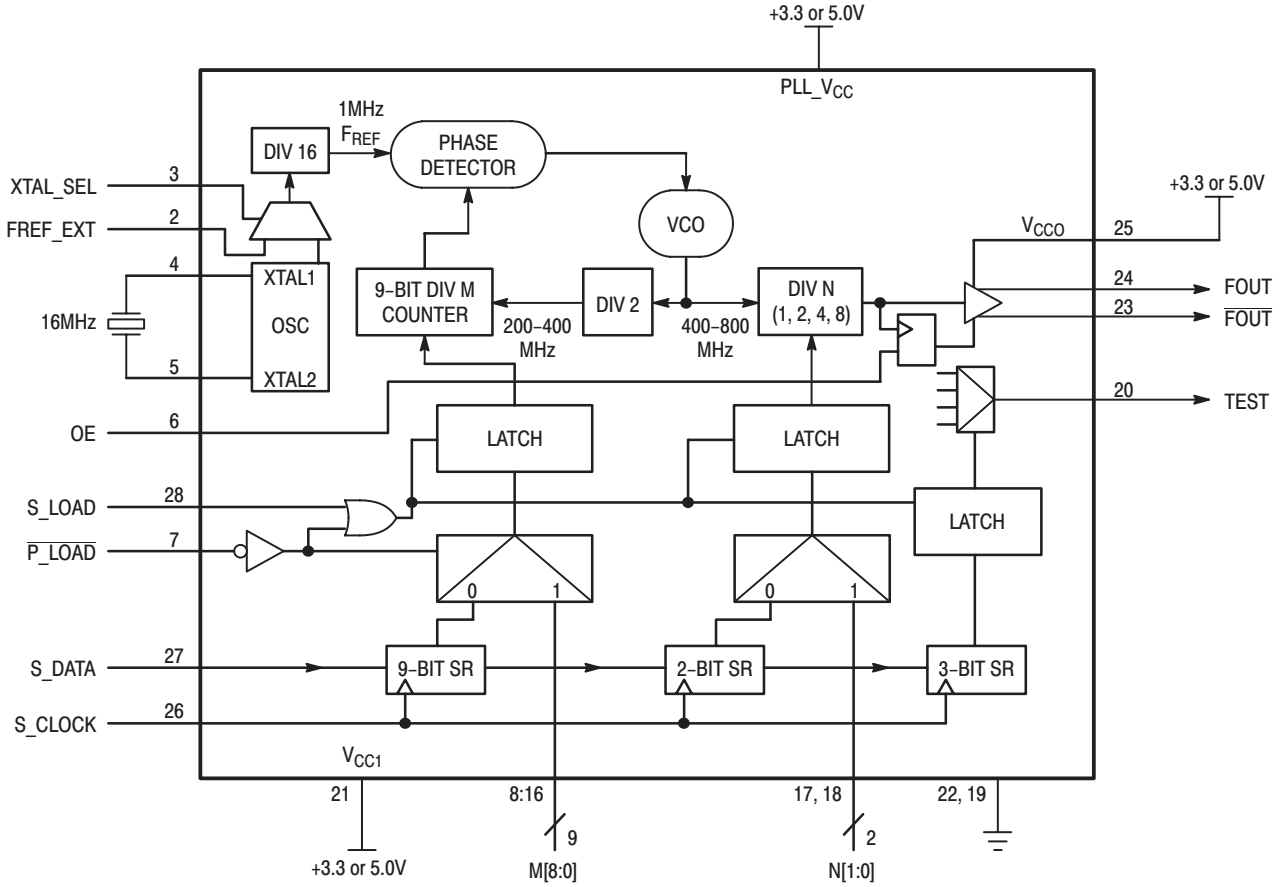



**Figure 3. MC12430 Block Diagram (28–Lead PLCC Pinout)**

## PROGRAMMING INTERFACE

Programming the device amounts to properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can by represented by this formula:

$$FOUT = (F_{XTAL} \div 16) \times M \times 2 \div N \qquad (1)$$

Where $F_{XTAL}$ is the crystal frequency, M is the loop divider modulus, and N is the output divider modulus. Note that it is possible to select values of M such that the PLL is unable to achieve loop lock. To avoid this, always make sure that M is selected to be $200 \leq M \leq 400$ for any input reference.

Assuming that a 16 MHz reference frequency is used, the above equation reduces to:

$$FOUT = 2 \times M \div N$$

Substituting the four values for N (1, 2, 4, 8) yields:

**Output Frequency Range**

| N | FOUT | OUTPUT FREQUENCY RANGE |
|---|---|---|
| 1 | 2 x M | 400 – 800 MHZ |
| 2 | M | 200 – 400 MHZ |
| 4 | M ÷ 2 | 100 – 200 MHZ |
| 8 | M ÷ 4 | 50 – 100 MHZ |

From these ranges, the user will establish the value of N required, then the value of M can be calculated based on the appropriate equation above. For example, if an output frequency of 131 MHz was desired, the following steps would be taken to identify the appropriate M and N values. 131MHz falls within the frequency range set by an N value of 4 so N [1:0] = 01. For N = 4, FOUT = M ÷ 2 and M = 2 x FOUT. Therefore, M = 131 x 2 = 262, so M[8:0] = 100000110. Following this same procedure, a user can generate any whole frequency desired between 50 and 800MHz. Note that for N > 2 fractional values of FOUT can be realized. The size of the programmable frequency steps (and thus the indicator of the fractional output frequencies achievable) will be equal to FXTAL ÷ 8 ÷ N.

For input reference frequencies other than 16 MHz, the set of appropriate equations can be deduced from equation 1. For computer applications, another useful frequency base would be 16.666 MHz. From this reference, one can generate a family of output frequencies at multiples of the 33.333 MHz PCI clock. As an example, to generate a 133.333 MHz clock from a 16.666 MHz reference, the following M and N values would be used:

FOUT = 16.666 ÷ 16 x M x 2 ÷ N = 1.04166 x M x 2 ÷ N

Let N = 4, M = 133.3333 ÷ 1.04166 x 2 = 256

The value for M falls within the constraints set for PLL stability, therefore, N[1:0] = 01 and M[8:0] = 10000000. If the value for M fell outside of the valid range, a different N value would be selected to try to move M in the appropriate direction.

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the $\overline{\text{P\_LOAD}}$ signal such that a LOW to HIGH transition will latch the information present on the M[8:0] and N[1:0] inputs into the M and N counters. When the $\overline{\text{P\_LOAD}}$ signal is LOW, the input latches will be transparent and any changes on the M[8:0] and N[1:0] inputs will affect the FOUT output pair. To use the serial port, the S_CLOCK signal samples the information on the S_DATA line and loads it into a 14 bit shift register. Note that the $\overline{\text{P\_LOAD}}$ signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data stream on the S_DATA input. For each register, the most significant bit is loaded first (T2, N1 and M8). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 4 illustrates the timing diagram for both a parallel and a serial load of the MC12430 synthesizer.

M[8:0] and N[1:0] are normally specified once at power–up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine–tune the clock as the ability to control the serial interface becomes available.

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. The T2, T1 and T0 control bits are preset to '000' when $\overline{\text{P\_LOAD}}$ is LOW so that the PECL FOUT outputs are as jitter–free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Most of the signals available on the TEST output pin are useful only for performance verification of the MC12430 itself. However, the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MC12430 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the FOUT differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clock tree. Figure 5 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level, the input frequency is limited to 250 MHz or less. This means the fastest the FOUT pin can be toggled via the S_CLOCK is 250MHz as the minimum divide ratio of the N counter is 1. Note that the M counter output on the TEST output will not be a 50% duty cycle due to the way the divider is implemented.

| T2 | T1 | T0 | **TEST** (Pin 20) |
|---|---|---|---|
| 0 | 0 | 0 | SHIFT REGISTER OUT |
| 0 | 0 | 1 | HIGH |
| 0 | 1 | 0 | FREF |
| 0 | 1 | 1 | M COUNTER OUT/2 |
| 1 | 0 | 0 | FOUT |
| 1 | 0 | 1 | LOW |
| 1 | 1 | 0 | M COUNTER/2 in PLL Bypass Mode |
| 1 | 1 | 1 | FOUT/4 |

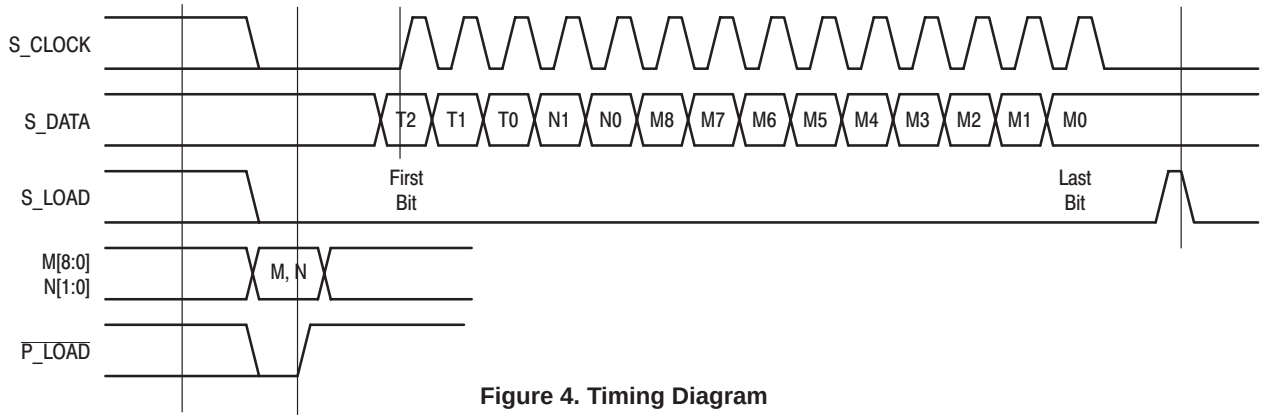
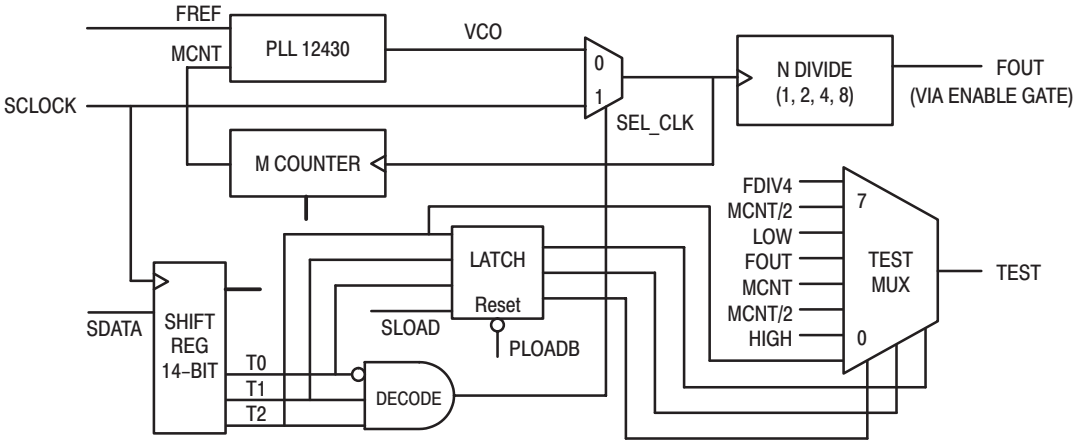



**Figure 4. Timing Diagram**




- T2=T1=1, T0=0: Test Mode (PLL Bypass)
- SCLOCK is selected, MCNT/2 is on TEST output, SCLOCK DIVIDE BY N is on FOUT pin

PLOADB acts as reset for test pin latch. When latch reset T2 data is shifted out TEST pin.

**Figure 5. Serial Test Clock Block Diagram**

**DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ±5%)

| | | 0°C | | | 25°C | | | 70°C | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** | **Condition** |
| $V_{IH}$ | Input HIGH Voltage | 2.2 | | | 2.2 | | | 2.2 | | | V | |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | | | 0.8 | | | 0.8 | V | |
| $I_{IN}$ | Input Current | | | 1.0 | | | 1.0 | | | 1.0 | mA | |
| $V_{OH}$ | Output HIGH Voltage TEST | 2.5 | | | 2.5 | | | 2.5 | | | V | $I_{OH}$ = –0.8mA |
| $V_{OL}$ | Output LOW Voltage TEST | | | 0.4 | | | 0.4 | | | 0.4 | V | $I_{OL}$ = 0.8mA |
| $V_{OH}$ | Output HIGH Voltage[1.] FOUT, $\overline{FOUT}$ | 2.28 | | 2.60 | 2.32 | | 2.49 | 2.38 | | 2.565 | V | $V_{CCO}$ = 3.3V[2.3.] |
| $V_{OL}$ | Output LOW Voltage[1.] FOUT, $\overline{FOUT}$ | 1.35 | | 1.67 | 1.35 | | 1.67 | 1.35 | | 1.70 | V | $V_{CCO}$ = 3.3V[2.3.] |
| $I_{CC}$ | Power Supply Current $V_{CC}$<br>$PLL\_V_{CC}$ | | 90<br>15 | 110<br>20 | | 90<br>15 | 110<br>20 | | 90<br>15 | 110<br>20 | mA | |

1. See applications information section for output level versus frequency information.
2. Output levels will vary 1:1 with $V_{CCO}$ variation.
3. 50 Ω to $V_{CC}$ – 2.0 V termination.

**DC CHARACTERISTICS** ($V_{CC}$ = 5.0V ±5%)

| | | 0°C | | | 25°C | | | 70°C | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** | **Condition** |
| $V_{IH}$ | Input HIGH Voltage | 3.5 | | | 3.5 | | | 3.5 | | | V | |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | | | 0.8 | | | 0.8 | V | |
| $I_{IN}$ | Input Current | | | 1.0 | | | 1.0 | | | 1.0 | mA | |
| $V_{OH}$ | Output HIGH Voltage TEST | 2.5 | | | 2.5 | | | 2.5 | | | V | $I_{OH}$ = –0.8 mA |
| $V_{OL}$ | Output LOW Voltage TEST | | | 0.4 | | | 0.4 | | | 0.4 | V | $I_{OL}$ = 0.8 mA |
| $V_{OH}$ | Output HIGH Voltage[1.] FOUT, $\overline{FOUT}$ | 3.98 | | 4.30 | 4.02 | | 4.19 | 4.08 | | 4.265 | V | $V_{CCO}$ = 5.0 V[2.3.] |
| $V_{OL}$ | Output LOW Voltage[1.] FOUT, $\overline{FOUT}$ | 3.05 | | 3.37 | 3.05 | | 3.37 | 3.05 | | 3.40 | V | $V_{CCO}$ = 5.0 V[2.3.] |
| $I_{CC}$ | Power Supply Current $V_{CC}$<br>$PLL\_V_{CC}$ | | 90<br>15 | 110<br>20 | | 90<br>15 | 110<br>20 | | 90<br>15 | 110<br>20 | mA | |

1. See applications information section for output level versus frequency information.
2. Output levels will vary 1:1 with $V_{CCO}$ variation.
3. 50 Ω to $V_{CC}$ – 2.0V termination.

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V to 5.0V ±5%)

| Symbol | Characteristic | | Min | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $F_{MAXI}$ | Maximum Input Frequency | S_CLOCK<br>Xtal Oscillator<br>FREF_EXT | <br>10<br>10 | 10<br>20<br>Note 2. | MHz | Note 1. |
| $F_{MAXO}$ | Maximum Output Frequency | VCO (Internal)<br>FOUT | 400<br>50 | 800<br>800 | MHz | Note 4. |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 10 | ms | |
| $t_{jitter}$ | Period Deviation (Peak–to–Peak) Note 3. | | | ±25<br>±65 | ps | N = 2, 4, 8; Note 4.<br>N = 1; Note 4. |
| $t_s$ | Setup Time | S_DATA to S_CLOCK<br>S_CLOCK to S_LOAD<br>M, N to P_LOAD | 20<br>20<br>20 | | ns | |
| $t_h$ | Hold Time | S_DATA to S_CLOCK<br>M, N to P_LOAD | 20<br>20 | | ns | |
| $tpw_{MIN}$ | Minimum Pulse Width | S_LOAD<br>P_LOAD | 50<br>50 | | ns | |
| $t_r$, $t_f$ | Output Rise/Fall | FOUT | 300 | 800 | ps | 20%–80%; Note 4. |

1. 10MHz is the maximum frequency to load the feedback divide registers. S_CLOCK can be switched at higher frequencies when used as a test clock in TEST_MODE 6.
2. Maximum frequency on FREF_EXT is a function of the internal M counter limitations. The phase detector can handle up to 100MHz on the input, but the M counter must remain in the valid range of 200 ≤ M ≤ 400. See the Programming Interface section on page 326 of this data sheet for more details.
3. See Applications Information below for additional information.
4. 50Ω to $V_{CC}$ – 2.0 V pull–down.

3

## APPLICATIONS INFORMATION

### Using the On–Board Crystal Oscillator

The MC12430 features a fully integrated on–board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MC12430 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required.

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately, most crystals are characterized in a parallel resonant mode. Fortunately, there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result, a parallel resonant crystal can be used with the MC12430 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application, this level of inaccuracy is immaterial. Table 1 below specifies the performance requirements of the crystals to be used with the MC12430.

**Table 1. Recommended Crystal Specifications**

| Parameter | Value |
|---|---|
| Crystal Cut | Fundamental AT Cut |
| Resonance | Series Resonance* |
| Frequency Tolerance | ±75ppm at 25°C |
| Frequency/Temperature Stability | ±150ppm 0 to 70°C |
| Operating Range | 0 to 70°C |
| Shunt Capacitance | 5–7 pF |
| Equivalent Series Resistance (ESR) | 50 to 80Ω |
| Correlation Drive Level | 100 μW |
| Aging | 5 ppm/Yr (First 3 Years) |

* See accompanying text for series versus parallel resonant discussion.

3

**Power Supply Filtering**

The MC12430 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MC12430 provides separate power supplies for the digital circuitry ($V_{CC}$) and the internal PLL (PLL_VCC) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the PLL_VCC pin for the MC12430.

Figure 6 illustrates a typical power supply filter scheme. The MC12430 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the PLL_VCC pin of the MC12430. From the data sheet, the $I_{PLL\_VCC}$ current (the current sourced through the PLL_VCC pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0 V must be maintained on the PLL_VCC pin, very little DC voltage drop can be tolerated when a 3.3 V $V_{CC}$ supply is used. The resistor shown in Figure 6 must have a resistance of 10–15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

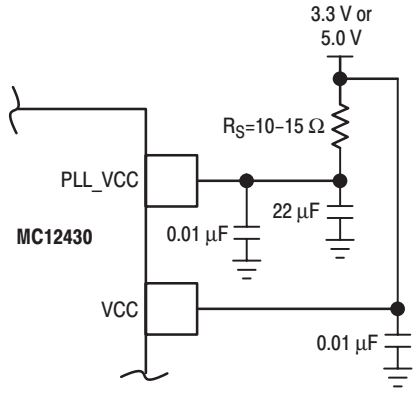



**Figure 6. Power Supply Filter**

A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000µH choke will show a significant impedance at 10 KHz frequencies and above. Because of the current draw and the voltage that must be maintained on the PLL_VCC pin, a low DC resistance inductor is required (less than 15 Ω). Generally, the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering.

The MC12430 provides sub–nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 7 shows a representative board layout for the MC12430. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 7 is the low impedance connections between VCC and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the 12430 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors.

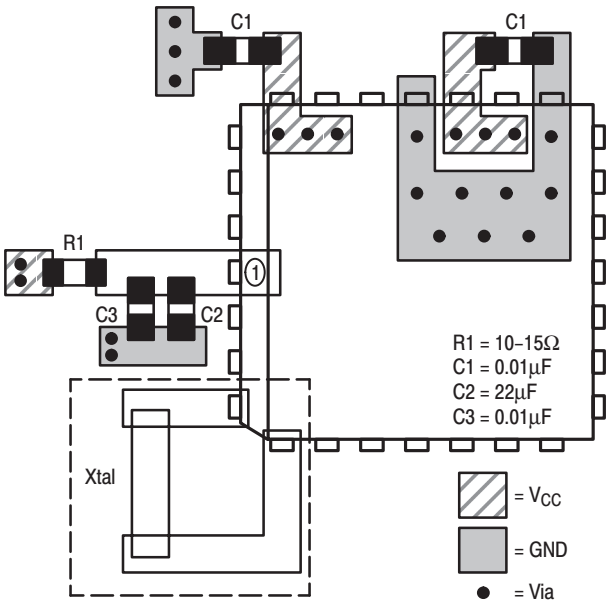



**Figure 7. PCB Board Layout for MC12430 (28 PLCC)**

Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on–board oscillator.

Although the MC12430 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Jitter Performance of the MC12430**

The MC12430 exhibits long term and cycle–to–cycle jitter which rivals that of SAW based oscillators. This jitter perfor-

mance comes with the added flexibility one gets with a synthesizer over a fixed frequency oscillator.

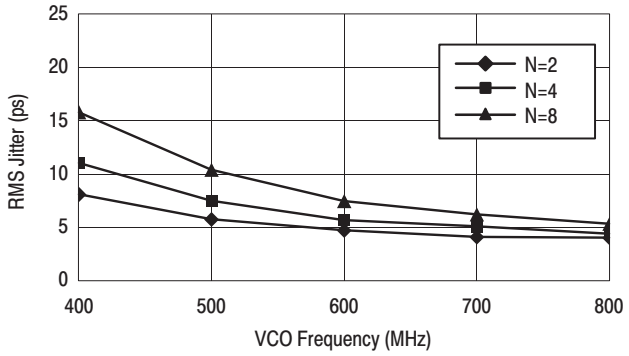



**Figure 8. RMS PLL Jitter versus VCO Frequency**

Figure 8 illustrates the RMS jitter performance of the MC12430 across its specified VCO frequency range. Note that the jitter is a function of both the output frequency as well as the VCO frequency, however the VCO frequency shows a much stronger dependence. The data presented has not been compensated for trigger jitter, this fact provides a measure of guardband to the reported data.

The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak–to–peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. The oscilloscope cannot collect adjacent pulses, rather it collects pulses from a very large sample of pulses.

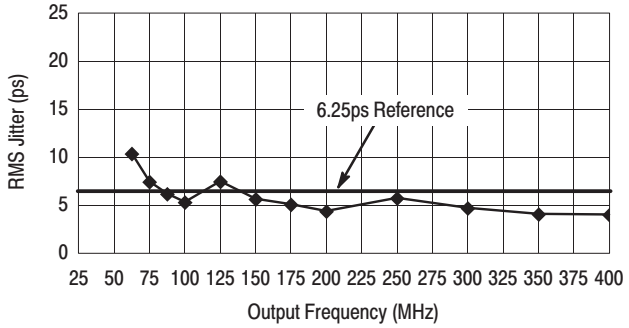



**Figure 9. RMS Jitter versus Output Frequency**

Figure 9 shows the jitter as a function of the output frequency. For the 12430, this information is probably of more importance. The flat line represents an RMS jitter value that corresponds to an 8 sigma ±25 ps peak–to–peak long term period jitter. The graph shows that for output frequencies from 87.5 to 400 MHz the jitter falls within the ±25 ps peak–to–peak specification. The general trend is that as the output frequency is decreased the output edge jitter will increase.

The jitter data from Figure 8 and Figure 9 do not include the performance of the 12430 when the output is in the divide by 1 mode. In divide by one mode, the MC12430 output jitter distribution is bimodal. Since a bimodal distribution cannot be accurately represented with an rms value, peak–to–peak values of jitter for the divide by one mode are presented.

Figure 10 shows the peak–to–peak jitter of the 12430 output in divide by one mode as a function of output frequency. Notice that as with the other modes the jitter improves with increasing frequency. The ±65 ps shown in the data sheet table represents a conservative value of jitter, especially for the higher VCO, and thus output frequencies.

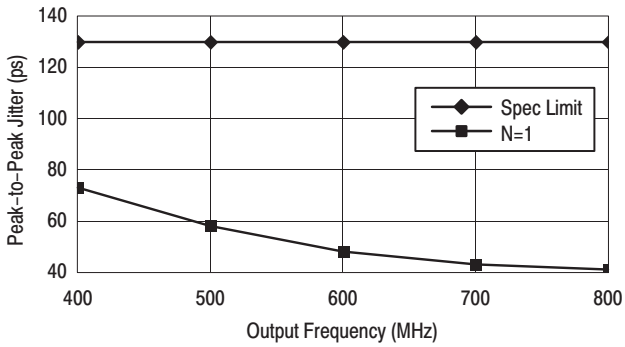



**Figure 10. Peak–to–Peak Jitter versus Output Frequency**

The jitter data presented should provide users with enough information to determine the effect on their overall timing budget. The jitter performance meets the needs of most system designs while adding the flexibility of frequency margining and field upgrades. These features are not available with a fixed frequency SAW oscillator.

### Output Voltage Swing vs Frequency

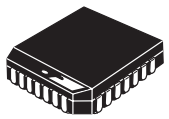
In the divide by one mode, the output rise and fall times will limit the peak to peak output voltage swing. For a 400 MHz output, the peak to peak swing of the 12430 output will be approximately 700 mV. This swing will gradually degrade as the output frequency increases, at 800 MHz the output swing will be reduced to approximately 500 mV. For a worst case analysis, it would be safe to assume that the 12430 output will always generate at least a 500mV output swing. Note that most high speed ECL receivers require only a few hundred millivolt input swings for reliable operation. As a result, the output generated by the 12430 will, under all conditions, be sufficient for clocking standard ECL devices. Note that if a larger swing is required the MC12430 could drive a clock fanout buffer like the MC100EP111.

**Order Number: MC12439/D**
**Rev. 6, 09/2001**

# High Frequency Clock Synthesizer

**MC12439**
**See Upgrade Product – MPC9239**

**HIGH FREQUENCY PLL CLOCK SYNTHESIZER**



**FN SUFFIX**
28–LEAD PLCC PACKAGE
CASE 776–02

The MC12439 is a general purpose synthesized clock source. Its internal VCO will operate over a range of frequencies from 400 to 800 MHz. The differential PECL output can be configured to be the VCO frequency divided by 1, 2, 4, or 8. With the output configured to divide the VCO frequency by 1, and with a 16.66 MHz external quartz crystal used to provide the reference frequency, the output frequency can be specified in 16.66MHz steps. The output frequency is configured using a parallel or serial interface.

- 50 to 800 MHz Differential PECL Outputs
- ±25 ps Typical Peak–to–Peak Output Jitter
- Minimal Frequency Over–Shoot
- Synthesized Architecture
- Serial 3–Wire Interface
- Parallel Interface for Power–Up
- Quartz Crystal Interface
- 28–Lead PLCC Package
- Operates from 3.3 V or 5.0V Power Supply

**Functional Description**

The internal oscillator uses the external quartz crystal as the basis of its frequency reference. The output of the reference oscillator is divided by 2 before being sent to the phase detector. With a 16.66 MHz crystal, this provides a reference frequency of 8.33 MHz. Although this data sheet illustrates functionality only for a 16 MHz and 16.66MHz crystal, any crystal in the 10–20 MHz range can be used. In addition to the crystal, an LVCMOS input can also be used as the PLL reference. The reference is selected via the XTAL_SEL input pin.

The VCO within the PLL operates over a range of 400 to 800 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The output of this loop divider is also applied to the phase detector.

The phase detector and loop filter attempt to force the VCO output frequency to be 2 x M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve loop lock.

The output of the VCO is also passed through an output divider before being sent to the PECL output driver. This output divider is configured through either the serial or the parallel interfaces and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle.

The output driver is driven differentially from the output divider and is capable of driving a pair of transmission lines terminated in 50 Ω to $V_{CC}$ – 2.0 V.

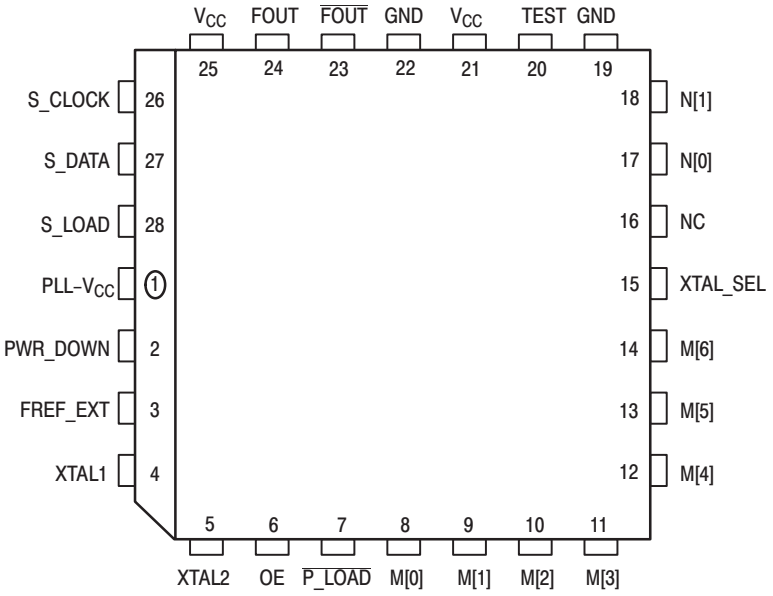
The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[6:0] and N[1:0] inputs to configure the internal counters. Normally, on system reset, the $\overline{\text{P\_LOAD}}$ input is held LOW until sometime after power becomes valid. On the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[6:0] and N[1:0] inputs to reduce component count in the application of the chip.

The serial interface centers on a twelve bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH–to–LOW edge of the S_LOAD input. See the programming section for more information.

The TEST output reflects various internal node values and is controlled by the T[2:0] bits in the serial data stream. See the programming section for more information.

The PWR_DOWN pin, when asserted, will synchronously divide the FOUT by 16. The power down sequence is clocked by the PLL reference clock, thereby causing the frequency reduction to happen relatively slowly. Upon de–assertion of the PWR_DOWN pin, the FOUT input will step back up to its programmed frequency in four discrete increments.

**Rev 6**




| N[1:0] | Output Division |
|---|---|
| 0 0 | 2 |
| 0 1 | 4 |
| 1 0 | 8 |
| 1 1 | 1 |

| Input | 0 | 1 |
|---|---|---|
| PWR_DOWN | FOUT | FOUT/16 |
| XTAL_SEL | FREF_EXT | XTAL |
| OE | Disabled | Enabled |

**28–Lead Pinout** (Top View)

**PIN DESCRIPTIONS**

| Pin Name | Type | Function |
|---|---|---|
| **Inputs** | | |
| XTAL1, XTAL2 | — | These pins form an oscillator when connected to an external series–resonant crystal. |
| S_LOAD | Int. Pulldown | This pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH, thus the data must be stable on the HIGH–to–LOW transition of S_LOAD for proper operation. |
| S_DATA | Int. Pulldown | This pin acts as the data input to the serial configuration shift registers. |
| S_CLOCK | Int. Pulldown | This pin serves to clock the serial configuration shift registers. Data from S_DATA is sampled on the rising edge. |
| $\overline{\text{P\_LOAD}}$ | Int. Pullup | This pin loads the configuration latches with the contents of the parallel inputs .The latches will be transparent when this signal is LOW, thus the parallel data must be stable on the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$ for proper operation. |
| M[6:0] | Int. Pullup | These pins are used to configure the PLL loop divider. They are sampled on the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$. M[6] is the MSB, M[0] is the LSB. |
| N[1:0] | Int. Pullup | These pins are used to configure the output divider modulus. They are sampled on the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$. $\overline{\text{P\_LOAD}}$ is state sensitive. |
| OE | Int. Pullup | Active HIGH Output Enable. |
| **Outputs** | | |
| $F_{OUT}$, $\overline{F_{OUT}}$ | — | These differential positive–referenced ECL signals (PECL) are the output of the synthesizer. |
| TEST | — | The function of this output is determined by the serial configuration bits T[2:0]. |
| **Power** | | |
| $V_{CC}$ | — | This is the positive supply for the chip, and is connected to +3.3 V or 5.0 V ($V_{CC}$ = PLL_$V_{CC}$). |
| PLL_$V_{CC}$ | — | This is the positive supply for the PLL and should be as noise–free as possible for low–jitter operation. This supply is connected to +3.3 V or 5.0 V ($V_{CC}$ = PLL_$V_{CC}$). |
| GND | — | These pins are the negative supply for the chip and are normally all connected to ground. |
| **Other** | | |
| PWR_DOWN | Int. Pulldown | LVCMOS input that forces the FOUT output to synchronously reduce its frequency by a factor of 16. |
| FREF_EXT | Int. Pulldown | LVCMOS input which can be used as the PLL reference frequency. |
| XTAL_SEL | Int. Pullup | LVCMOS input that selects between the XTAL and FREF_EXT PLL reference inputs. A HIGH selects the XTAL input. |

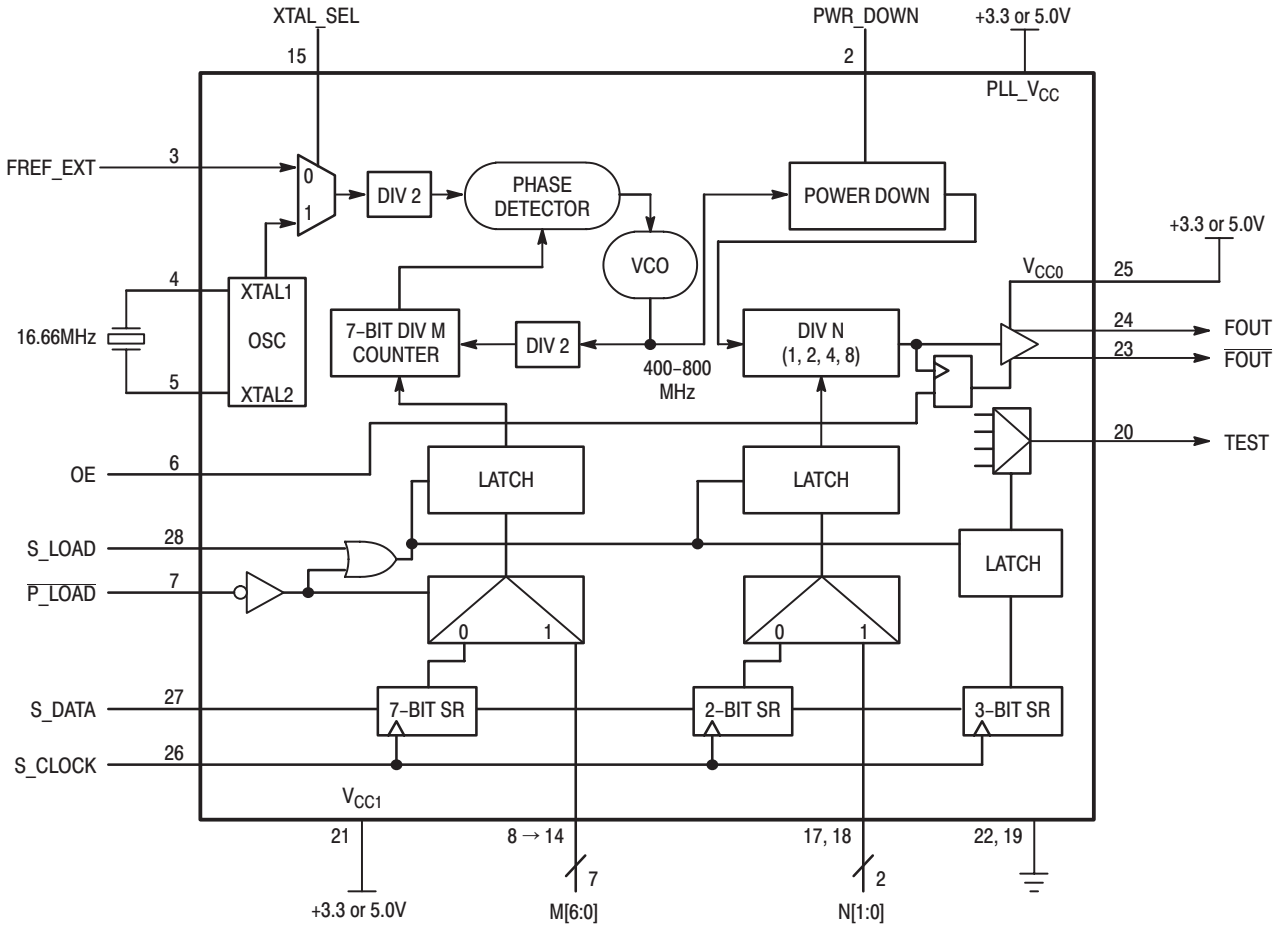



**Figure 1. MC12439 Block Diagram**

## PROGRAMMING INTERFACE

Programming the device amounts to properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can by represented by this formula:

$$FOUT = F_{XTAL} \times M \div N \qquad (1)$$

Where $F_{XTAL}$ is the crystal frequency, M is the loop divider modulus, and N is the output divider modulus. Note that it is possible to select values of M such that the PLL is unable to achieve loop lock. To avoid this, always make sure that M is selected to be $25 \le M \le 50$ for a 16MHz input reference.

For input references other than 16MHz, the valid M values can be calculated from the valid VCO range of 400–800MHz.

Assuming that a 16MHz reference frequency is used, the above equation reduces to:

$$FOUT = 16 \times M \div N$$

Substituting the four values for N (1, 2, 4, 8) yields:

**Output Frequency Range**

| N | FOUT | OUTPUT FREQUENCY RANGE |
|---|---|---|
| 1 | 16 x M | 400 – 800 MHZ |
| 2 | 8 x M | 200 – 400 MHZ |
| 4 | 4 x M | 100 – 200 MHZ |
| 8 | 2 x M | 50 – 100 MHZ |

From these ranges, the user will establish the value of N required, then the value of M can be calculated based on the appropriate equation above. For example, if an output frequency of 384MHz was desired, the following steps would be taken to identify the appropriate M and N values. 384 MHz falls within the frequency range set by an N value of 2, so N [1:0] = 00. For N = 2, $F_{OUT}$ = 8M and M = $F_{OUT} \div 8$. Therefore, M = 384 ÷ 8 = 48, so M[8:0] = 0110000.

For input reference frequencies other than 16MHz, the set of appropriate equations can be deduced from equation 1. For computer applications, another useful frequency base would be 16.666MHz. From this reference, one can generate a family of output frequencies at multiples of the 33.333 MHz PCI clock. As an example, to generate a 533.333MHz clock from a 16.666MHz reference, the following M and N values would be used:

$$FOUT = 16.666 \times M \div N$$

Let N = 1, M = 533.333 ÷ 16.666 = 32

The value for M falls within the constraints set for PLL stability ($400 \div 16.666 \le M \le 800 \div 16.666$; $24 \le M \le 48$), therefore N[1:0] = 11 and M[6:0} = 0100000. If the value for M fell outside of the valid range, a different N value would be selected to try to move M in the appropriate direction.

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the $\overline{P\_LOAD}$ signal such that a LOW to HIGH transition will latch the information present on the M[6:0] and N[1:0] inputs into the M and N counters. When the $\overline{P\_LOAD}$ signal is LOW, the input latches will be transparent and any changes on the M[6:0] and

N[1:0] inputs will affect the FOUT output pair. To use the serial port, the S_CLOCK signal samples the information on the S_DATA line and loads it into a 12 bit shift register. Note that the $\overline{\text{P\_LOAD}}$ signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data stream on the S_DATA input. For each register, the most significant bit is loaded first (T2, N1 and M6). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 2 illustrates the timing diagram for both a parallel and a serial load of the MC12439 synthesizer.

M[6:0] and N[1:0] are normally specified once at power–up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine–tune the clock as the ability to control the serial interface becomes available.

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents $F_{OUT}$, the CMOS output may not be able to toggle fast enough for some of the higher output frequencies. The T2, T1 and T0 control bits are preset to '000' when $\overline{\text{P\_LOAD}}$ is LOW so that the PECL FOUT outputs are as jitter–free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Most of the signals available on the TEST output pin are useful only for performance verification of the MC12439 itself. However the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110, the MC12439 is placed in PLL bypass mode. In this mode, the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the $F_{OUT}$ differential pair and the M counter drives the TEST output pin. In this mode, the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clock tree. Figure 3 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level, the input frequency is limited to 250 MHz or less. This means the fastest the FOUT pin can be toggled via the S_CLOCK is 250 MHz as the minimum divide ratio of the N counter is 1. Note that the M counter output on the TEST output will not be a 50% duty cycle due to the way the divider is implemented.

| **T2** | **T1** | **T0** | **TEST** (Pin 20) |
|---|---|---|---|
| 0 | 0 | 0 | SHIFT REGISTER OUT |
| 0 | 0 | 1 | HIGH |
| 0 | 1 | 0 | FREF |
| 0 | 1 | 1 | M COUNTER OUT/2 |
| 1 | 0 | 0 | FOUT |
| 1 | 0 | 1 | LOW |
| 1 | 1 | 0 | M COUNTER/2 in PLL Bypass Mode |
| 1 | 1 | 1 | FOUT/4 |

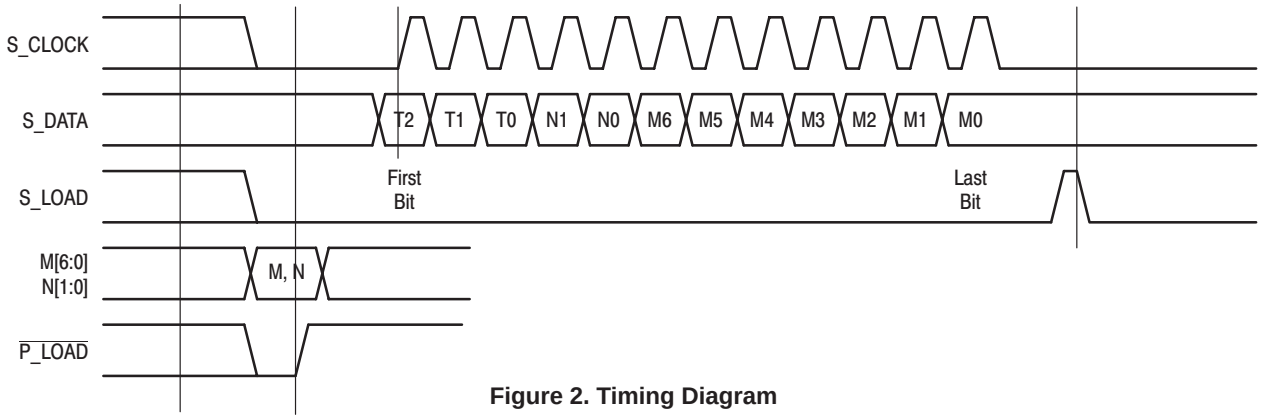
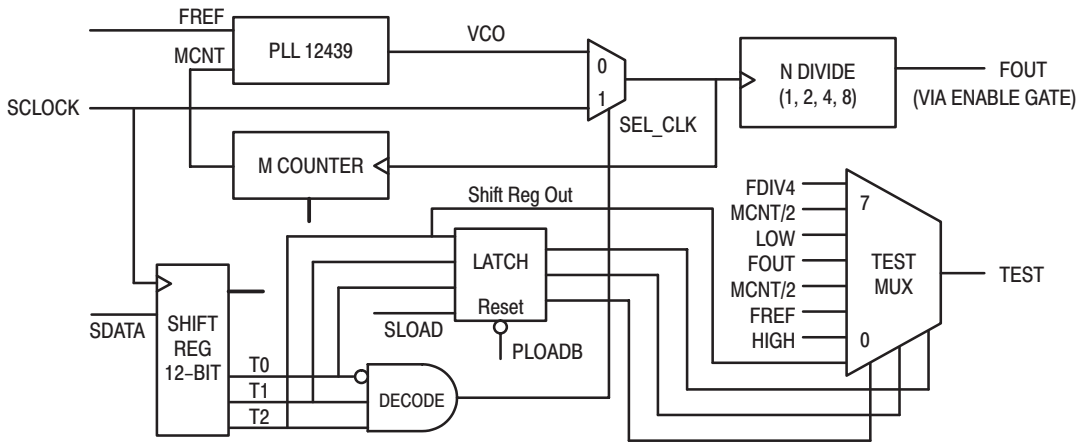



**Figure 2. Timing Diagram**

3




- T2 = T1 = 1, T0 = 0: Test Mode (PLL Bypass)
- SCLOCK is selected, MCNT/2 is on TEST output, SCLOCK DIVIDE BY N is on FOUT pin

PLOADB acts as reset for test pin latch. When latch reset T2 data is shifted out TEST pin.

**Figure 3. Serial Test Clock Block Diagram**

**DC CHARACTERISTICS** ($V_{CC}$ = 3.3 V ±5%)

| Symbol | Characteristic | 0°C | | | 25°C | | | 70°C | | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | | 2.0 | | | 2.0 | | | V | |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | | | 0.8 | | | 0.8 | V | |
| $I_{IN}$ | Input Current | | | 1.0 | | | 1.0 | | | 1.0 | mA | |
| $I_{OH}$ | Output HIGH Current[1] FOUT, $\overline{FOUT}$ | | | 50 | | | 50 | | | 50 | mA | Continuous |
| $V_{OH}$ | Output HIGH Voltage TEST | 2.5 | | | 2.5 | | | 2.5 | | | V | $I_{OH}$ = –0.8mA |
| $V_{OL}$ | Output LOW Voltage TEST | | | 0.4 | | | 0.4 | | | 0.4 | V | $I_{OL}$ = 0.8mA |
| $V_{OH}$ | Output HIGH Voltage[2] FOUT, $\overline{FOUT}$ | 2.28 | | 2.60 | 2.32 | | 2.49 | 2.38 | | 2.565 | V | $V_{CCO}$ = 3.3V[3,4] |
| $V_{OL}$ | Output LOW Voltage[2] FOUT, $\overline{FOUT}$ | 1.35 | | 1.67 | 1.35 | | 1.67 | 1.35 | | 1.70 | V | $V_{CCO}$ = 3.3V[3,4] |
| $I_{CC}$ | Power Supply Current $V_{CC}$<br>PLL_$V_{CC}$ | | 90<br>15 | 110<br>20 | | 90<br>15 | 110<br>20 | | 90<br>15 | 110<br>20 | mA | |

1. Maximum $I_{OH}$ spec implies the device can drive 25Ω impedance with the PECL outputs.
2. See Applications Information section for output level versus frequency information.
3. Output levels will vary 1:1 with $V_{CC}$ variation.
4. 50Ω to $V_{CC}$ – 2.0V termination.

**DC CHARACTERISTICS** ($V_{CC}$ = 5.0 V ±5%)

| Symbol | Characteristic | 0°C | | | 25°C | | | 70°C | | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| $V_{IH}$ | Input HIGH Voltage | 3.5 | | | 3.5 | | | 3.5 | | | V | |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | | | 0.8 | | | 0.8 | V | |
| $I_{IN}$ | Input Current | | | 1.0 | | | 1.0 | | | 1.0 | mA | |
| $I_{OH}$ | Output HIGH Current[1] FOUT, $\overline{FOUT}$ | | | 50 | | | 50 | | | 50 | mA | Continuous |
| $V_{OH}$ | Output HIGH Voltage TEST | 3.8 | | | 3.8 | | | 3.8 | | | V | $I_{OH}$ = –0.8 mA |
| $V_{OL}$ | Output LOW Voltage TEST | | | 0.4 | | | 0.4 | | | 0.4 | V | $I_{OL}$ = 0.8 mA |
| $V_{OH}$ | Output HIGH Voltage[2] FOUT, $\overline{FOUT}$ | 3.98 | | 4.30 | 4.02 | | 4.19 | 4.08 | | 4.265 | V | $V_{CCO}$ = 5.0 V[3,4] |
| $V_{OL}$ | Output LOW Voltage[2] FOUT, $\overline{FOUT}$ | 3.05 | | 3.37 | 3.05 | | 3.37 | 3.05 | | 3.40 | V | $V_{CCO}$ = 5.0 V[3,4] |
| $I_{CC}$ | Power Supply Current $V_{CC}$<br>PLL_$V_{CC}$ | | 90<br>15 | 110<br>20 | | 90<br>15 | 110<br>20 | | 90<br>15 | 110<br>20 | mA | |

1. Maximum $I_{OH}$ spec implies the device can drive 25Ω impedance with the PECL outputs.
2. See applications information section for output level versus frequency information.
3. Output levels will vary 1:1 with $V_{CC0}$ variation.
4. 50Ω to $V_{CC}$ – 2.0V termination.

**AC CHARACTERISTICS** ($T_A$ = 0 to 70°C; $V_{CC}$ = 3.3 to 5.0V ±5%)

| Symbol | Characteristic | | Min | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $F_{MAXI}$ | Maximum Input Frequency | S_CLOCK<br>Xtal Oscillator<br>FREF_EXT | <br>10<br>10 | 10<br>20<br>Note 5. | MHz | |
| $F_{MAXO}$ | Maximum Output Frequency | VCO (Internal)<br>FOUT | 400<br>50 | 900<br>800 | MHz | Note 7. |
| $t_{LOCK}$ | Maximum PLL Lock Time | | 1 | 10 | ms | |
| $t_{jitter}$ | Period Deviation (Peak–to–Peak) (Note 6.) | | | ±25<br>±65 | ps | N = 2,4,8; Note 7.<br>N = 1; Note 7. |
| $t_s$ | Setup Time | S_DATA to S_CLOCK<br>S_CLOCK to S_LOAD<br>M, N to P_LOAD | 20<br>20<br>20 | | ns | |
| $t_h$ | Hold Time | S_DATA to S_CLOCK<br>M, N to P_LOAD | 20<br>20 | | ns | |
| $tpw_{MIN}$ | Minimum Pulse Width | S_LOAD<br>P_LOAD | 50<br>50 | | ns | Note 7. |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 300 | 800 | ps | Note 7. |

5. Maximum frequency on FREF_EXT is a function of the internal M counter limitations. The phase detector can handle up to 100 MHz on the input, but the M counter must remain in the valid range of 25 ≤ M ≤ 50. See the programming section in this data sheet for more details.
6. See Applications Information section for additional information.
7. 50 Ω to $V_{CC}$ – 2.0 V pulldown.

## APPLICATIONS INFORMATION

### Using the On–Board Crystal Oscillator

The MC12439 features a fully integrated on–board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs, the user is advised to mount the crystal as close to the MC12439 as possible to avoid any board level parasitics. To facilitate co–location, surface mount crystals are recommended but not required.



The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately, most crystals are characterized in a parallel resonant mode. Fortunately, there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result, a parallel resonant crystal can be used with the MC12439 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application, this level of inaccuracy is immaterial. Table 1 below specifies the performance requirements of the crystals to be used with the MC12439.

**Table 1. Crystal Specifications**

| Parameter | Value |
|---|---|
| Crystal Cut | Fundamental AT Cut |
| Resonance | Series Resonance* |
| Frequency Tolerance | ±75 ppm at 25°C |
| Frequency/Temperature Stability | ±150 pm 0 to 70°C |
| Operating Range | 0 to 70°C |
| Shunt Capacitance | 5–7 pF |
| Equivalent Series Resistance (ESR) | 50 to 80 Ω |
| Correlation Drive Level | 100 μW |
| Aging | 5 ppm/Yr (First 3 Years) |

* See accompanying text for series versus parallel resonant discussion.

### Power Supply Filtering

The MC12439 is a mixed analog/digital product, and as such, it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MC12439 provides separate power supplies for the digital circuitry ($V_{CC}$) and the internal PLL (PLL_VCC) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies, a second level of isolation may be required. The simplest form of isolation is a power supply filter on the PLL_VCC pin for the MC12439.

Figure 4 illustrates a typical power supply filter scheme. The MC12439 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the PLL_$V_{CC}$ pin of the MC12439. From the data sheet, the $I_{PLL\_VCC}$ current (the current sourced through the PLL_VCC pin) is typically 15mA (20 mA maximum), assuming that a minimum of 3.0 V must be maintained on the PLL_VCC pin very little DC voltage drop can be tolerated when a 3.3 V $V_{CC}$ supply is used. The resistor shown in Figure 4 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

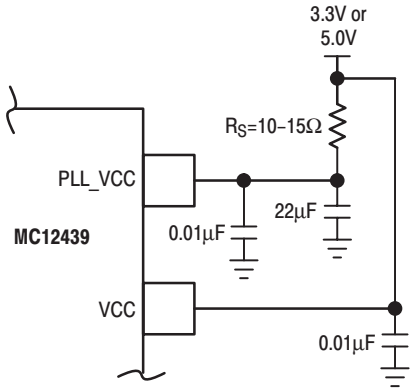



**Figure 4. Power Supply Filter**

A higher level of attenuation can be acheived by replacing the resistor with an appropriate valued inductor. A 1000 μH choke will show a significant impedance at 10 kHz frequencies and above. Because of the current draw and the voltage that must be maintained on the PLL_VCC pin, a low DC resistance inductor is required (less than 15 Ω). Generally, the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering.

The MC12439 provides sub–nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 5 shows a representative board layout for the MC12439. There exist many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 5 is the low impedance connections between $V_{CC}$ and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the 12439 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the

leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors.

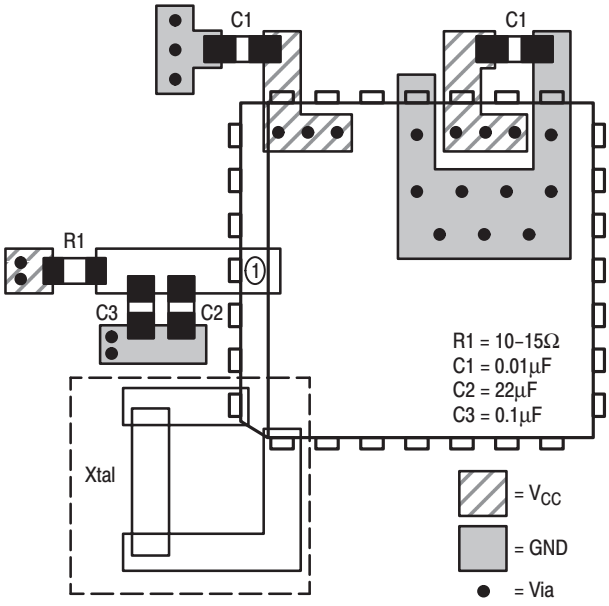



**Figure 5. PCB Board Layout for MC12439**

Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit, and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on–board oscillator.

Although the MC12439 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Jitter Performance of the MC12439**

The MC12439 exhibits long term and cycle–to–cycle jitter which rivals that of SAW based oscillators. This jitter performance comes with the added flexibility one gets with a synthesizer over a fixed frequency oscillator.

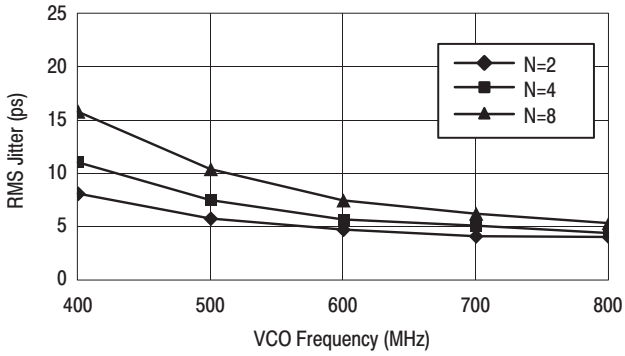



**Figure 6. RMS PLL Jitter versus VCO Frequency**

Figure 6 illustrates the RMS jitter performance of the MC12439 across its specified VCO frequency range. Note that the jitter is a function of both the output frequency as well as the VCO frequency, however the VCO frequency shows a much stronger dependence. The data presented has not been compensated for trigger jitter, this fact provides a measure of guardband to the reported data.

The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak–to–peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. The oscilloscope cannot collect adjacent pulses, rather it collects pulses from a very large sample of pulses.

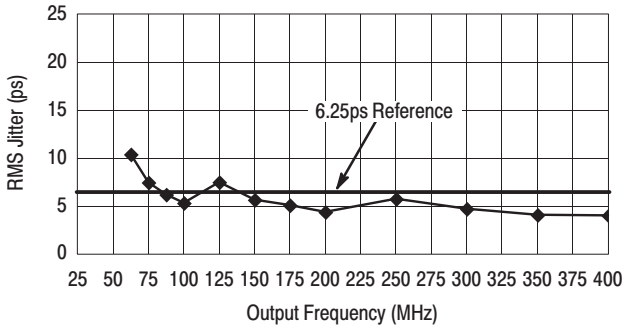



**Figure 7. RMS Jitter versus Output Frequency**

Figure 7 shows the jitter as a function of the output frequency. For the 12439, this information is probably of more importance. The flat line represents an RMS jitter value that corresponds to an 8 sigma ±25 ps peak–to–peak long term period jitter. The graph shows that for output frequencies from 87.5 to 400 MHz the jitter falls within the ±25 ps peak–to–peak specification. The general trend is that as the output frequency is decreased, the output edge jitter will increase.

The jitter data from Figure 6 does not include the performance of the 12439 when the output is in the divide by 1 mode. In divide by one mode, the MC12439 output jitter distribution is bimodal. Since a bimodal distribution cannot be acurately represented with an rms value, peak–to–peak values of jitter for the divide by one mode are presented.

Figure 8 shows the peak–to–peak jitter of the 12439 output in divide by one mode as a function of output frequency. Notice

that as with the other modes, the jitter improves with increasing frequency. The ±65 ps shown in the data sheet table represents a conservative value of jitter, especially for the higher VCO, and thus output frequencies.

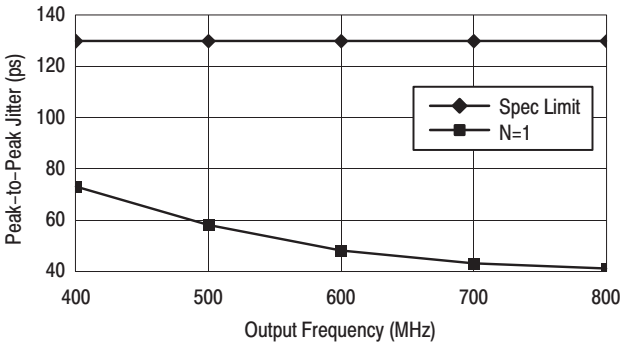



**Figure 8. Peak–to–Peak Jitter versus Output Frequency**

The jitter data presented should provide users with enough information to determine the effect on their overall timing budget. The jitter performance meets the needs of most system designs while adding the flexibility of frequency margining and field upgrades. These features are not available with a fixed frequency SAW oscillator.

**Output Voltage Swing vs Frequency**

In the divide by one mode, the output rise and fall times will limit the peak to peak output voltage swing. For a 400 MHz output, the peak to peak swing of the 12439 output will be approximately 700 mV. This swing will gradually degrade as the output frequency increases, at 800 MHz the output swing will be reduced to approximately 500 mV. For a worst case analysis, it would be safe to assume that the 12439 output will always generate at least a 400mV output swing. Note that most high speed ECL receivers require only a few hundred millivolt input swings for reliable operation. As a result, the output generated by the 12439 will, under all conditions, be sufficient for clocking standard ECL devices. Note that if a larger swing is desired, the MC12439 could drive the clock fanout buffer MC100EP111.

**Order Number: MPC9229/D**
**Rev 0, 11/2001**

*Preliminary Information*

# 450 MHz Low Voltage PECL Clock Synthesizer

**MPC9229**

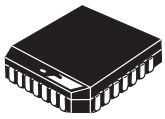
**450 MHZ LOW VOLTAGE CLOCK SYNTHESIZER**

3

The MPC9229 is a 3.3V compatible, PLL based clock synthesizer targeted for high performance clock generation in mid-range to high-performance telecom, networking and computing applications. With output frequencies from 25 MHz to 450 MHz[1] and the support of differential PECL output signals the device meets the needs of the most demanding clock applications.

**Features**

- 25 MHz to 450 MHz synthesized clock output signal
- Differential PECL output
- LVCMOS compatible control inputs
- On-chip crystal oscillator for reference frequency generation
- 3.3V power supply
- Fully integrated PLL
- Minimal frequency overshoot
- Serial 3-wire programming interface
- Parallel programming interface for power-up
- 32 lead LQFP and 28 PLCC packaging
- SiGe Technology
- Ambient temperature range 0°C to +70°C
- Pin and function compatible to the MC12429



**FN SUFFIX**
28–LEAD PLCC PACKAGE
CASE 776

**FA SUFFIX**
32 LEAD LQFP PACKAGE
CASE 873A

**Functional Description**

The internal crystal oscillator uses the external quartz crystal as the basis of its frequency reference. The frequency of the internal crystal oscillator is divided by 16 and then multiplied by the PLL. The VCO within the PLL operates over a range of 800 to 1800 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The crystal oscillator frequency $f_{XTAL}$, the PLL feedback-divider M and the PLL post-divider N determine the output frequency.

The feedback path of the PLL is internal. The PLL adjusts the VCO output frequency to be 4·M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve phase lock. The PLL will be stable if the VCO frequency is within the specified VCO frequency range (800 to 1800 MHz). The M-value must be programmed by the serial or parallel interface.

The PLL post-divider N is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle. The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated 50Ω to $V_{CC}$ – 2.0V. The positive supply voltage for the internal PLL is separated from the power supply for the core logic and output drivers to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. It is recommended on system reset to hold the $\overline{\text{P\_LOAD}}$ input LOW until power becomes valid. On the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[8:0] and N[1:0] inputs prevent the LVCMOS compatible control inputs from floating.

The serial interface centers on a fourteen bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH–to–LOW edge of the S_LOAD input. See the programming section for more information. The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. In order to minimize the PLL jitter, it is recommended to avoid active signal on the TEST output.



**Rev 0**

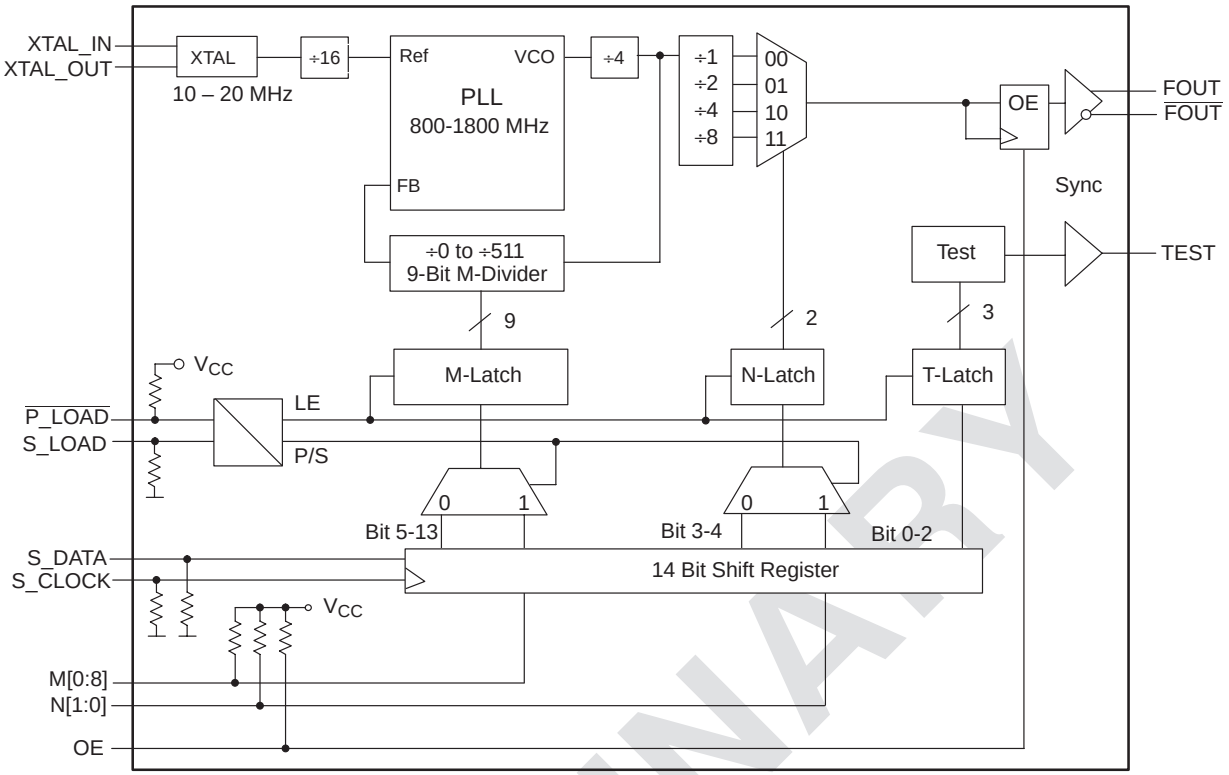



**Figure 1. MPC9229 Logic Diagram**

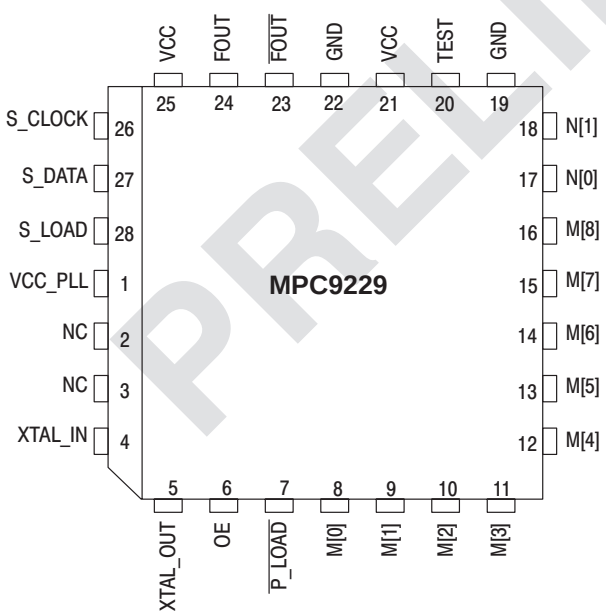



**Figure 2. MPC9229 28–Lead Package Pinout**
(Top View)

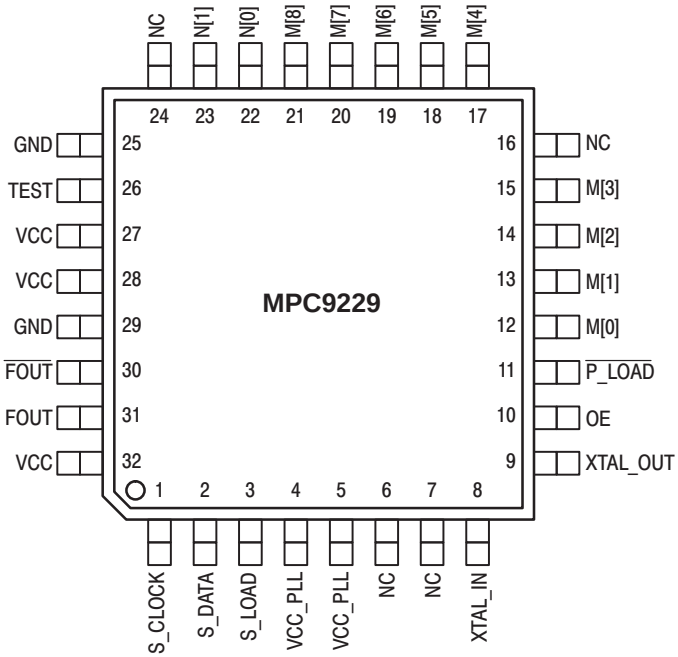



**Figure 3. MPC9229 32–Lead PLCC Pinout**
(Top View)

**Table 1. Pin Configuration**

| Pin | I/O | Default | Type | Function |
|---|---|---|---|---|
| XTAL_IN, XTAL_OUT | | | Analog | Crystal oscillator interface |
| FOUT, $\overline{\text{FOUT}}$ | Output | | LVPECL | Differential clock output |
| TEST | Output | | LVCMOS | Test and device diagnosis output |
| S_LOAD | Input | 0 | LVCMOS | Serial configuration control input.<br>This inputs controls the loading of the configuration latches with the contents of the shift register. The latches will be transparent when this signal is high, thus the data must be stable on the high-to-low transition. |
| $\overline{\text{P\_LOAD}}$ | Input | 1 | LVCMOS | Parallel configuration control input.<br>This input controls the loading of the configuration latches with the content of the parallel inputs (M and N). The latches will be transparent when this signal is low, thus the parallel data must be stable on the low-to-high transition of $\overline{\text{P\_LOAD}}$.<br>$\overline{\text{P\_LOAD}}$ is state sensitive |
| S_DATA | Input | 0 | LVCMOS | Serial configuration data input. |
| S_CLOCK | Input | 0 | LVCMOS | Serial configuration clock input. |
| M[0:8] | Input | 1 | LVCMOS | Parallel configuration for PLL feedback divider (M).<br>M is sampled on the low-to-high transition of $\overline{\text{P\_LOAD}}$. |
| N[1:0] | Input | 1 | LVCMOS | Parallel configuration for Post-PLL divider (N).<br>N is sampled on the low-to-high transition of $\overline{\text{P\_LOAD}}$ |
| OE | Input | 1 | LVCMOS | Output enable (active high)<br>The output enable is synchronous to the output clock to eliminate the possibility of runt pulses on the $F_{OUT}$ output. OE = L low stops $F_{OUT}$ in the logic low state ($F_{OUT}$ = L, $\overline{\text{FOUT}}$ = H) |
| GND | Supply | Supply | Ground | Negative power supply (GND) |
| $V_{CC}$ | Supply | Supply | $V_{CC}$ | Positive power supply for I/O and core. All $V_{CC}$ pins must be connected to the positive power supply for correct operation |
| VCC_PLL | Supply | Supply | $V_{CC}$ | PLL positive power supply (analog power supply) |

**Table 2. Output frequency range and PLL Post-divider N**

| N | | Output division | Output frequency range |
|---|---|---|---|
| **1** | **0** | | |
| 0 | 0 | 1 | 200 - 450 MHz |
| 0 | 1 | 2 | 100 - 225 MHz |
| 1 | 0 | 4 | 50 - 112.5 MHz |
| 1 | 1 | 8 | 25 - 56.25 MHz |

**Table 3. General Specifications**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output termination voltage | | $V_{CC}$ - 2 | | V | |
| MM | ESD protection (Machine model) | 200 | | | V | |
| HBM | ESD protection (Human body model) | 2000 | | | V | |
| LU | Latch-up immunity | 200 | | | mA | |
| $C_{IN}$ | Input capacitance | | 4.0 | | pF | Inputs |
| $\theta_{JA}$ | LQFP 32 Thermal resistance junction to ambient | | | | | |
| | JESD 51-3, single layer test board | | 83.1 | 86.0 | °C/W | Natural convection |
| | | | 73.3 | 75.4 | °C/W | 100 ft/min |
| | | | 68.9 | 70.9 | °C/W | 200 ft/min |
| | | | 63.8 | 65.3 | °C/W | 400 ft/min |
| | | | 57.4 | 59.6 | °C/W | 800 ft/min |
| | JESD 51-6, 2S2P multilayer test board | | 59.0 | 60.6 | °C/W | Natural convection |
| | | | 54.4 | 55.7 | °C/W | 100 ft/min |
| | | | 52.5 | 53.8 | °C/W | 200 ft/min |
| | | | 50.4 | 51.5 | °C/W | 400 ft/min |
| | | | 47.8 | 48.8 | °C/W | 800 ft/min |
| $\theta_{JC}$ | LQFP 32 Thermal resistance junction to case | | 23.0 | 26.3 | °C/W | MIL-SPEC 883E Method 1012.1 |

**Table 4. Absolute Maximum Ratings**[a]

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -65 | 125 | °C | |

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 5. DC Characteristics** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = 0°C to +70°C)[a]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| LVCMOS control inputs ($\overline{P\_LOAD}$, S_LOAD, S_DATA, S_CLOCK, M[0:8], N[0:1], OE) | | | | | | |
| $V_{IH}$ | Input high voltage | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | | | 0.8 | V | LVCMOS |
| $I_{IN}$ | Input Current[b] | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| Differential clock output $F_{OUT}$[c] | | | | | | |
| $V_{OH}$ | Output High Voltage | 2.28 | | 2.56 | V | LVPECL |
| $V_{OL}$ | Output Low Voltage | 1.35 | | 1.70 | V | LVPECL |
| Test and diagnosis output TEST | | | | | | |
| $V_{OH}$ | Output High Voltage | 2.0 | | | V | $I_{OH}$ = -0.8 mA |
| $V_{OL}$ | Output Low Voltage | | | 0.55 | V | $I_{OL}$ = 0.8 mA |
| Supply current | | | | | | |
| $I_{CC\_PLL}$ | Maximum PLL Supply Current | | | 20 | mA | $V_{CC\_PLL}$ Pins |
| $I_{CC}$ | Maximum Supply Current | | | 100 | mA | All $V_{CC}$ Pins |

a All AC characteristics are design targets and subject to change upon device characterization.
b. Inputs have pull-down resistors affecting the input current.
c. Outputs terminated 50Ω to $V_{TT}$ = $V_{CC}$ - 2V.

**Table 6. AC Characteristics** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = 0°C to +70°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{XTAL}$ | Crystal interface frequency range | | 10 | | 20 | MHz | |
| $f_{VCO}$ | VCO frequency range[c] | | 800 | | 1800 | MHz | |
| $f_{MAX}$ | Output Frequency | N = 00 (÷1)<br>N = 01 (÷2)<br>N = 10 (÷4)<br>N = 11 (÷8) | 200<br>100<br>50<br>25 | | 450<br>225<br>112.5<br>56.25 | MHz<br>MHz<br>MHz<br>MHz | |
| DC | Output duty cycle | | 45 | 50 | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.05 | | TBD | ns | 20% to 80% |
| $f_{S\_CLOCK}$ | Serial interface programming clock frequency[d] | | 0 | | 10 | MHz | |
| $t_{P,MIN}$ | Minimum pulse width | (S_LOAD, $\overline{\text{P\_LOAD}}$) | 50 | | | ns | |
| $t_S$ | Setup Time | S_DATA to S_CLOCK<br>S_CLOCK to $\overline{\text{S\_LOAD}}$<br>M, N to $\overline{\text{P\_LOAD}}$ | 20<br>20<br>20 | | | ns<br>ns<br>ns | |
| $t_S$ | Hold Time | S_DATA to S_CLOCK<br>M, N to $\overline{\text{P\_LOAD}}$ | 20<br>20 | | | ns<br>ns | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ)[e] | | TBD | TBD | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | | ±25 | ps | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | | 10 | ms | |

a All AC characteristics are design targets and subject to change upon device characterization.
b AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
c The input frequency $f_{XTAL}$ and the PLL feedback divider M must match the VCO frequency range: $f_{VCO} = f_{XTAL} \cdot M \div 4$.
d The frequency of S_CLOCK is limited to 10 MHz in serial programming mode. S_CLOCK can be switched at higher frequencies when used as test clock in test mode 6. See application section for more details.
e See application section for a jitter calculation for other confidence factors than 1 σ.



3

**Programming the MPC9229**

Programming the MPC9229 amounts to properly configuring the internal PLL dividers to produce the desired synthesized frequency at the output. The output frequency can be represented by this formula:

$f_{OUT} = (f_{XTAL} \div 16) \cdot (4 \cdot M) \div (4 \cdot N)$ or (1)
$f_{OUT} = (f_{XTAL} \div 16) \cdot M \div N$ (2)

where $f_{XTAL}$ is the crystal frequency, M is the PLL feedback-divider and N is the PLL post-divider. The input frequency and the selection of the feedback divider M is limited by the VCO-frequency range. $f_{XTAL}$ and M must be configured to match the VCO frequency range of 800 to 1800 MHz in order to achieve stable PLL operation:

$M_{MIN} = 4 \cdot f_{VCO,MIN} \div f_{XTAL}$ and (3)
$M_{MAX} = 4 \cdot f_{VCO,MAX} \div f_{XTAL}$ (4)

For instance, the use of a 16 MHz input frequency requires the configuration of the PLL feedback divider between M=200 and M = 450. Table 7 shows the usable VCO frequency and M divider range for other example input frequencies. Assuming that a 16 MHz input frequency is used, equation (2) reduces to:

$f_{OUT} = M \div N$ (5)

**Table 7. MPC9229 Frequency Operating Range**

| | | VCO frequency for an crystal interface frequency of | | | | | | Output frequency for $f_{XTAL}$=16 MHz and for N = | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **M** | **M[8:0]** | **10** | **12** | **14** | **16** | **18** | **20** | **1** | **2** | **4** | **16** |
| 160 | 010100000 | | | | | | 800 | | | | |
| 170 | 010101010 | | | | | | 850 | | | | |
| 180 | 010110100 | | | | | 810 | 900 | | | | |
| 190 | 010111110 | | | | | 855 | 950 | | | | |
| 200 | 011001000 | | | | 800 | 900 | 1000 | 200 | 100 | 50 | 25 |
| 210 | 011010010 | | | | 840 | 945 | 1050 | 210 | 105 | 52.5 | 26.25 |
| 220 | 011011100 | | | | 880 | 990 | 1100 | 220 | 110 | 55 | 27.50 |
| 230 | 011100110 | | | 805 | 920 | 1035 | 1150 | 230 | 115 | 57.5 | 28.75 |
| 240 | 011110000 | | | 840 | 960 | 1080 | 1200 | 240 | 120 | 60 | 30 |
| 250 | 011111010 | | | 875 | 100 | 1125 | 1250 | 250 | 125 | 62.5 | 31.25 |
| 260 | 100000100 | | | 910 | 1040 | 1170 | 1300 | 260 | 130 | 65 | 32.50 |
| 270 | 100001110 | | 810 | 945 | 1080 | 1215 | 1350 | 270 | 135 | 67.5 | 33.75 |
| 280 | 100011000 | | 840 | 980 | 1120 | 1260 | 1400 | 280 | 140 | 70 | 35 |
| 290 | 100100010 | | 870 | 1015 | 1160 | 1305 | 1450 | 290 | 145 | 72.5 | 36.25 |
| 300 | 100101100 | | 900 | 1050 | 1200 | 1350 | 1500 | 300 | 150 | 75 | 37.5 |
| 310 | 100110110 | | 930 | 1085 | 1240 | 1395 | 1550 | 310 | 155 | 77.5 | 38.75 |
| 320 | 101000000 | 800 | 960 | 1120 | 1280 | 1440 | 1600 | 320 | 160 | 80 | 40 |
| 330 | 101001010 | 825 | 990 | 1155 | 1320 | 1485 | 1650 | 330 | 165 | 82.5 | 41.25 |
| 340 | 101010100 | 850 | 1020 | 1190 | 1360 | 1530 | 1700 | 340 | 170 | 85 | 42.5 |
| 350 | 101011110 | 875 | 1050 | 1225 | 1400 | 1575 | 1750 | 350 | 175 | 87.5 | 43.75 |
| 360 | 101101000 | 900 | 1080 | 1260 | 1440 | 1620 | 1800 | 360 | 180 | 90 | 45 |
| 370 | 101110010 | 925 | 1110 | 1295 | 1480 | 1665 | | 370 | 185 | 92.5 | 46.25 |
| 380 | 101111100 | 950 | 1140 | 1330 | 1520 | 1710 | | 380 | 190 | 95 | 47.5 |
| 390 | 110000110 | 975 | 1170 | 1365 | 1560 | 1755 | | 390 | 195 | 97.5 | 48.75 |
| 400 | 110010000 | 1000 | 1200 | 1400 | 1600 | 1800 | | 400 | 200 | 100 | 50 |
| 410 | 110011010 | 1025 | 1230 | 1435 | 1640 | | | 410 | 205 | 102.5 | 51.25 |
| 420 | 110100100 | 1050 | 1260 | 1470 | 1680 | | | 420 | 210 | 105 | 52.5 |
| 430 | 110101110 | 1075 | 1290 | 1505 | 1720 | | | 430 | 215 | 107.5 | 53.75 |
| 440 | 110111000 | 1100 | 1320 | 1540 | 1760 | | | 440 | 220 | 110 | 55 |
| 450 | 111000010 | 1125 | 1350 | 1575 | 1800 | | | 450 | 225 | 112.5 | 56.25 |
| 510 | 111111110 | 1275 | 1530 | 1610 | | | | | | | |

Substituting N for the four available values for N (1, 2, 4, 8) yields:

**Table 8. Output Frequency Range for $f_{XTAL}$ = 16 MHz**

| N | | | $F_{OUT}$ | $F_{OUT}$ range | $F_{OUT}$ step |
|---|---|---|---|---|---|
| 1 | 0 | Value | | | |
| 0 | 0 | 1 | M | 200 - 450 MHz | 1 MHz |
| 0 | 1 | 2 | M÷2 | 100 - 225 MHz | 500 kHz |
| 1 | 0 | 4 | M÷4 | 50 - 112.5 MHz | 250 kHz |
| 1 | 1 | 8 | M÷8 | 25 - 56.25 MHz | 125 kHz |

### Example frequency calculation for an 16 MHz input frequency

If an output frequency of 131 MHz was desired the following steps would be taken to identify the appropriate M and N values. According to Table 8, 131 MHz falls in the frequency set by an value of 2 so N[1:0] = 01. For N = 2 the output frequency is $F_{OUT}$ = M ÷ 2 and M = $F_{OUT}$ x 2. Therefore M = 2 x 131 = 262, so M[8:0] = 100000110. Following this procedure a user can generate any whole frequency between 25 MHz and 450 MHz. Note than for N > 2 fractional values of can be realized. The size of the programmable frequency steps (and thus the indicator of the fractional output frequencies achievable) will be equal to:

$$f_{STEP} = f_{XTAL} \div 16 \div N \quad (6)$$

### Using the parallel and serial interface

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the $\overline{\text{P\_LOAD}}$ signal such that a LOW to HIGH transition will latch the information present on the M[8:0] and N[1:0] inputs into the M and N counters. When the $\overline{\text{P\_LOAD}}$ signal is LOW the input latches will be transparent and any changes on the M[8:0] and N[1:0] inputs will affect the FOUT output pair. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 14 bit shift register. Note that the $\overline{\text{P\_LOAD}}$ signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1 and M8). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 4 illustrates the timing diagram for both a parallel and a serial load of the MPC9229 synthesizer. M[8:0] and N[1:0] are normally specified once at power–up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine–tune the clock as the ability to control the serial interface becomes available.

### Using the test and diagnosis output TEST

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents $F_{OUT}$, the CMOS output is not able to toggle fast enough for higher output frequencies and should only be used for test and diagnosis. The T2, T1 and T0 control bits are preset to ‘000’ when $\overline{\text{P\_LOAD}}$ is LOW so that the PECL FOUT outputs are as jitter–free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin. Most of the signals available on the TEST output pin are useful only for performance verification of the MPC9229 itself. However the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MPC9229 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the $F_{OUT}$ differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving $F_{OUT}$ directly gives the user more control on the test clocks sent through the clock tree. Figure 6 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 200 MHz. This means the fastest the $F_{OUT}$ pin can be toggled via the S_CLOCK is 100 MHz as the divide ratio of the Post-PLL divider is 2 (if N = 1). Note that the M counter output on the TEST output will not be a 50% duty cycle.

**Table 9. Test and Debug Configuration for TEST**

| T[2:0] | | | TEST output |
|---|---|---|---|
| T2 | T1 | T0 | |
| 0 | 0 | 0 | 14-bit shift register out[a] |
| 0 | 0 | 1 | Logic 1 |
| 0 | 1 | 0 | $f_{XTAL}$ ÷ 16 |
| 0 | 1 | 1 | M-Counter out |
| 1 | 0 | 0 | FOUT |
| 1 | 0 | 1 | Logic 0 |
| 1 | 1 | 0 | M-Counter out in PLL-bypass mode |
| 1 | 1 | 1 | FOUT ÷ 4 |

a. Clocked out at the rate of S_CLOCK

**Table 10. Debug Configuration for PLL bypass[a]**

| Output | Configuration |
|---|---|
| $F_{OUT}$ | S_CLOCK ÷ N |
| TEST | M-Counter out[b] |

a. T[2:0]=110. AC specifications do not apply in PLL bypass mode

b. clocked out at the rate of S_CLOCK÷(4·N)

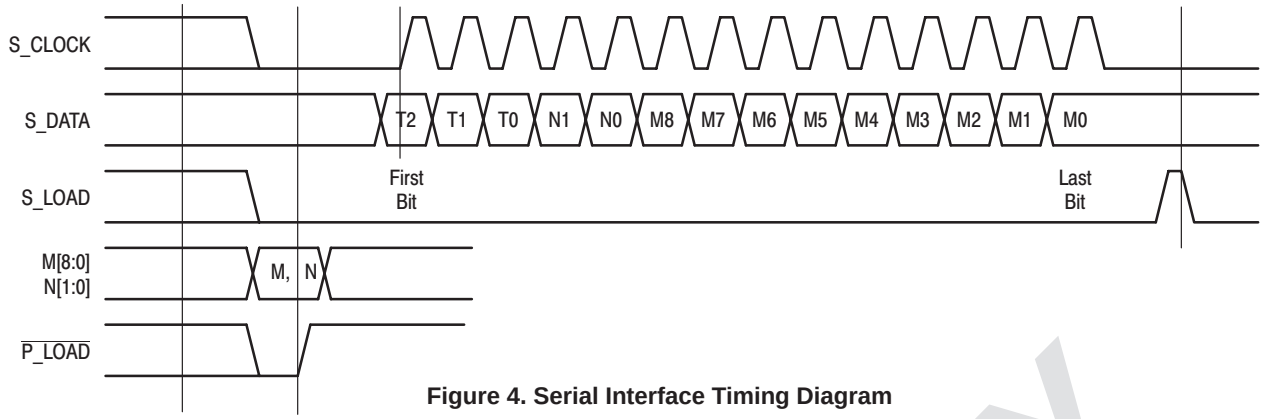



**Figure 4. Serial Interface Timing Diagram**

3

## Power Supply Filtering

The MPC9229 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC9229 provides separate power supplies for the digital circuitry ($V_{CC}$) and the internal PLL (VCC_PLL) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCC_PLL pin for the MPC9229. Figure 5 illustrates a typical power supply filter scheme. The MPC9229 is most susceptible to noise with spectral content in the 1 KHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the MPC9229 pin of the MPC9229. From the data sheet, the VCC_PLL current (the current sourced through the VCC_PLL pin) is typically TBD mA (TBD maximum), assuming that a minimum of 3.135V must be maintained on the VCC_PLL pin, very little DC voltage drop can be tolerated when a 3.3V $V_{CC}$ supply is used. The resistor shown in Figure 5 must have a resistance of TBD Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 KHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Generally, the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering. A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000μH choke will show a significant impedance at 10 KHz frequencies and above. Because of the current draw and the voltage that must be maintained on the VCC_PLL pin, a low DC resistance inductor is required (less than TBD Ω).

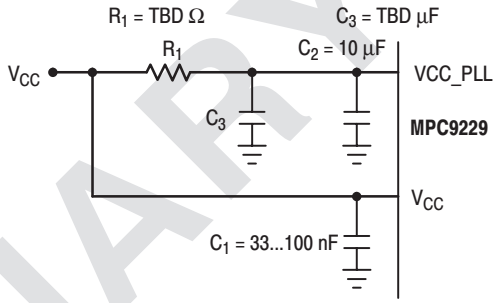



**Figure 5. $V_{CC\_PLL}$ Power Supply Filter**

## Layout Recommendations

The MPC9229 provides sub–nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 6 shows a representative board layout for the MPC9229. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 6 is the low impedance connections between VCC and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the MPC9229 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors. Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on–board oscillator. Although the MPC9229 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall perfor-

mance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

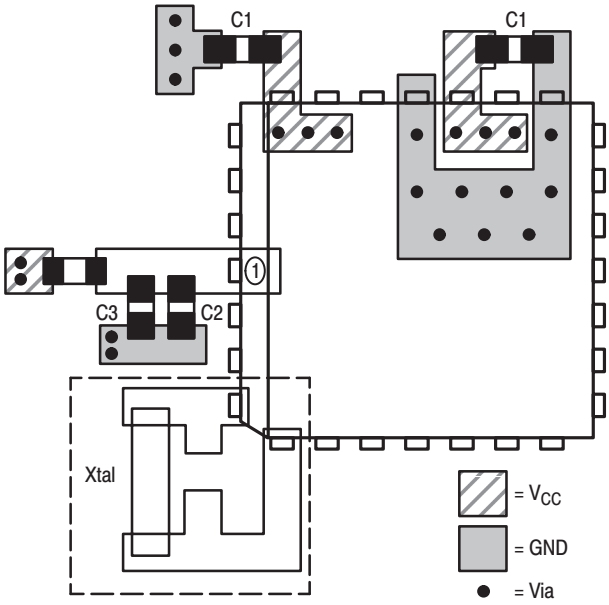



**Figure 6. PCB Board Layout Recommendation for the PLCC28 Package**

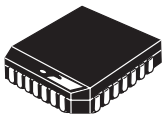
**Order Number: MPC9230/D**
**Rev 0, 11/2001**

*Product Preview*

# 900 MHz Low Voltage PECL Clock Synthesizer

**MPC9230**

**900 MHZ LOW VOLTAGE CLOCK SYNTHESIZER**



**FN SUFFIX**
28 LEAD PLCC PACKAGE
CASE 776

**FA SUFFIX**
32 LEAD LQFP PACKAGE
CASE 873A

3

The MPC9230 is a 3.3V compatible, PLL based clock synthesizer targeted for high performance clock generation in mid-range to high-performance telecom, networking and computing applications. With output frequencies from 50 MHz to 900 MHz and the support of differential PECL output signals the device meets the needs of the most demanding clock applications.

**Features**

- 50 MHz to 900 MHz synthesized clock output signal
- Differential PECL output
- LVCMOS compatible control inputs
- On-chip crystal oscillator for reference frequency generation
- Alternative LVCMOS compatible reference clock input
- 3.3V power supply
- Fully integrated PLL
- Minimal frequency overshoot
- Serial 3-wire programming interface
- Parallel programming interface for power-up
- 32 lead LQFP and 28 PLCC packaging
- SiGe Technology
- Ambient temperature range 0°C to +70°C
- Pin and function compatible to the MC12430

**Functional Description**

The internal crystal oscillator uses the external quartz crystal as the basis of its frequency reference. The frequency of the internal crystal oscillator is divided by 16 and then multiplied by the PLL. The VCO within the PLL operates over a range of 800 to 1800 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The crystal oscillator frequency $f_{XTAL}$, the PLL feedback-divider M and the PLL post-divider N determine the output frequency.

The feedback path of the PLL is internal. The PLL adjusts the VCO output frequency to be 8·M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve phase lock. The PLL will be stable if the VCO frequency is within the specified VCO frequency range (800 to 1800 MHz). The M-value must be programmed by the serial or parallel interface.

The PLL post-divider N is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle. The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated 50Ω to $V_{CC}$ – 2.0V. The positive supply voltage for the internal PLL is separated from the power supply for the core logic and output drivers to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. It is recommended on system reset to hold the $\overline{\text{P\_LOAD}}$ input LOW until power becomes valid. On the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[8:0] and N[1:0] inputs prevent the LVCMOS compatible control inputs from floating.

The serial interface centers on a fourteen bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH–to–LOW edge of the S_LOAD input. See the programming section for more information. The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. In order to minimize the PLL jitter, it is recommended to avoid active signal on the TEST output.



**Rev 0**

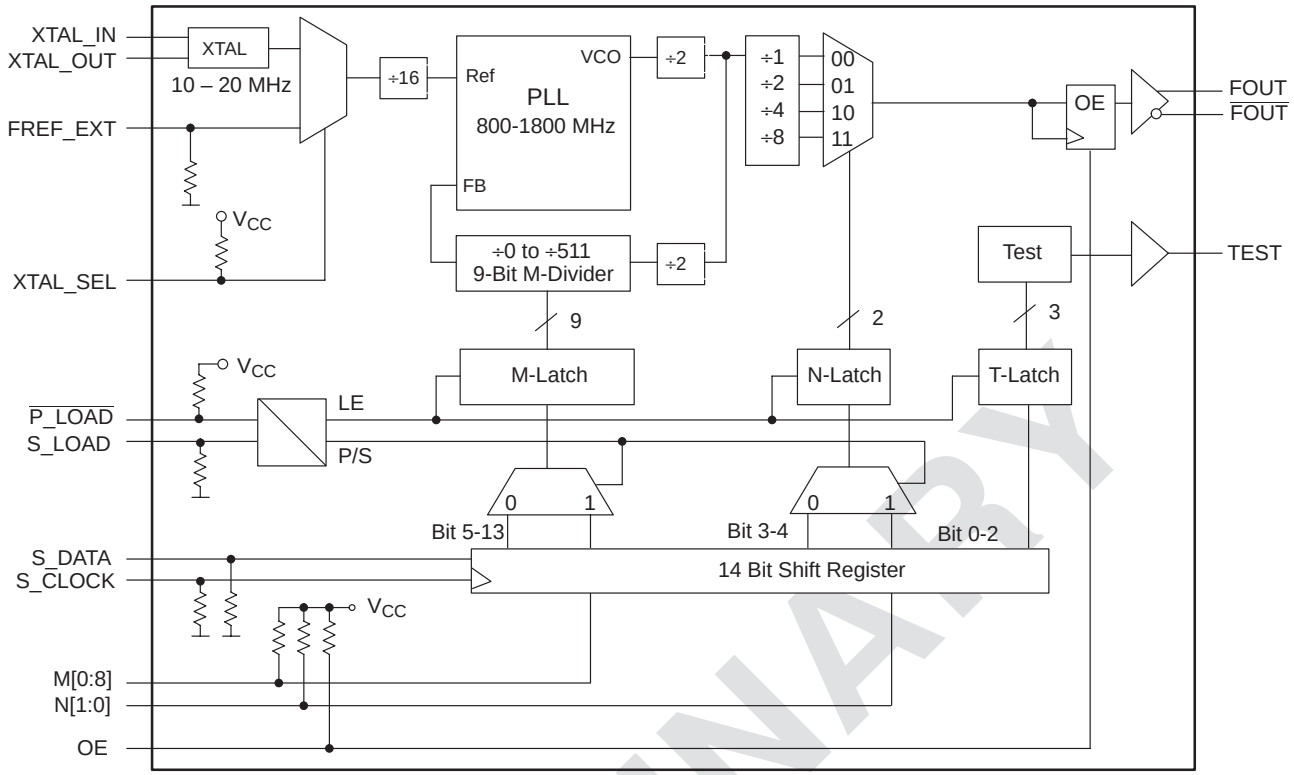



**Figure 1. MPC9230 Logic Diagram**



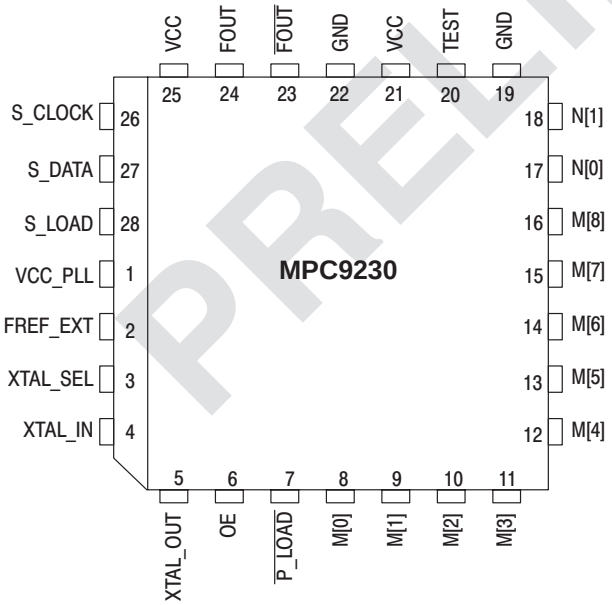



**Figure 2. MPC9230 28–Lead PLCC Pinout**
(Top View)

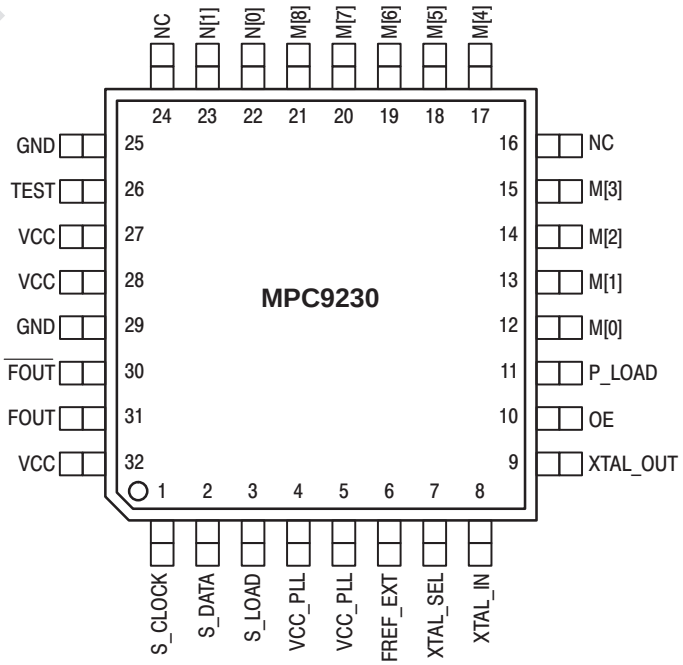



**Figure 3. MPC9230 32–Lead Package Pinout**
(Top View)

**Table 1. Pin Configuration**

| Pin | I/O | Default | Type | Function |
|---|---|---|---|---|
| XTAL_IN, XTAL_OUT | | | Analog | Crystal oscillator interface |
| FREF_EXT | Input | 0 | LVCMOS | Alternative PLL reference input |
| FOUT, $\overline{\text{FOUT}}$ | Output | | LVPECL | Differential clock output |
| TEST | Output | | LVCMOS | Test and device diagnosis output |
| XTAL_SEL | Input | 1 | LVCMOS | PLL reference select input |
| S_LOAD | Input | 0 | LVCMOS | Serial configuration control input.<br>This inputs controls the loading of the configuration latches with the contents of the shift register. The latches will be transparent when this signal is high, thus the data must be stable on the high-to-low transition. |
| $\overline{\text{P\_LOAD}}$ | Input | 1 | LVCMOS | Parallel configuration control input.<br>This input controls the loading of the configuration latches with the content of the parallel inputs (M and N). The latches will be transparent when this signal is low, thus the parallel data must be stable on the low-to-high transition of $\overline{\text{P\_LOAD}}$.<br>$\overline{\text{P\_LOAD}}$ is state sensitive |
| S_DATA | Input | 0 | LVCMOS | Serial configuration data input. |
| S_CLOCK | Input | 0 | LVCMOS | Serial configuration clock input. |
| M[0:8] | Input | 1 | LVCMOS | Parallel configuration for PLL feedback divider (M).<br>M is sampled on the low-to-high transition of $\overline{\text{P\_LOAD}}$. |
| N[1:0] | Input | 1 | LVCMOS | Parallel configuration for Post-PLL divider (N).<br>N is sampled on the low-to-high transition of $\overline{\text{P\_LOAD}}$ |
| OE | Input | 1 | LVCMOS | Output enable (active high)<br>The output enable is synchronous to the output clock to eliminate the possibility of runt pulses on the $F_{OUT}$ output. |
| GND | Supply | Supply | Ground | Negative power supply (GND) |
| $V_{CC}$ | Supply | Supply | $V_{CC}$ | Positive power supply for I/O and core. All $V_{CC}$ pins must be connected to the positive power supply for correct operation |
| VCC_PLL | Supply | Supply | $V_{CC}$ | PLL positive power supply (analog power supply) |

**Table 2. Output frequency range and PLL Post-divider N**

| N | | Output division | Output frequency range |
|---|---|---|---|
| 1 | 0 | | |
| 0 | 0 | 1 | 400 - 900 MHz |
| 0 | 1 | 2 | 200 - 450 MHz |
| 1 | 0 | 4 | 100 - 225 MHz |
| 1 | 1 | 8 | 50 - 112.5 MHz |

**Table 3. Function Table**

| Input | 0 | 1 |
|---|---|---|
| XTAL_SEL | FREF_EXT | XTAL interface |
| OE | Outputs disabled, FOUT is stopped in the logic low state (FOUT = L, $\overline{\text{FOUT}}$ = H) | Outputs enabled |

**Table 4. General Specifications**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output termination voltage | | $V_{CC}$ - 2 | | V | |
| MM | ESD protection (Machine model) | 200 | | | V | |
| HBM | ESD protection (Human body model) | 2000 | | | V | |
| LU | Latch-up immunity | 200 | | | mA | |
| $C_{IN}$ | Input capacitance | | 4.0 | | pF | Inputs |

**Table 5. Absolute Maximum Ratings**[a]

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -65 | 125 | °C | |

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 6. DC Characteristics** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = 0°C to +70°C)[a]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| LVCMOS control inputs (FREF_EXT, XTAL_SEL, $\overline{\text{P\_LOAD}}$, S_LOAD, S_DATA, S_CLOCK, M[0:8], N[0:1], OE) | | | | | | |
| $V_{IH}$ | Input high voltage | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | | | 0.8 | V | LVCMOS |
| $I_{IN}$ | Input Current[b] | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| Differential clock output $F_{OUT}$[c] | | | | | | |
| $V_{OH}$ | Output High Voltage | 2.28 | | 2.56 | V | LVPECL |
| $V_{OL}$ | Output Low Voltage | 1.35 | | 1.70 | V | LVPECL |
| Test and diagnosis output TEST | | | | | | |
| $V_{OH}$ | Output High Voltage | 2.0 | | | V | $I_{OH}$ = -0.8 mA |
| $V_{OL}$ | Output Low Voltage | | | 0.55 | V | $I_{OL}$ = 0.8 mA |
| Supply current | | | | | | |
| $I_{CC\_PLL}$ | Maximum PLL Supply Current | | | 20 | mA | $V_{CC\_PLL}$ Pins |
| $I_{CC}$ | Maximum Supply Current | | | 110 | mA | All $V_{CC}$ Pins |

a All AC characteristics are design targets and subject to change upon device characterization.
b. Inputs have pull-down resistors affecting the input current.
c. Outputs terminated 50Ω to $V_{TT}$ = $V_{CC}$ - 2V.

**Table 7. AC Characteristics** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = 0°C to +70°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{XTAL}$ | Crystal interface frequency range | | 10 | | 20 | MHz | |
| $f_{VCO}$ | VCO frequency range[c] | | 800 | | 1800 | MHz | |
| $f_{MAX}$ | Output Frequency | N = 00 (÷1)<br>N = 01 (÷2)<br>N = 10 (÷4)<br>N = 11 (÷8) | 400<br>200<br>100<br>50 | | 900<br>450<br>225<br>112.5 | MHz<br>MHz<br>MHz<br>MHz | |
| $f_{S\_CLOCK}$ | Serial interface programming clock frequency[d] | | 0 | | 10 | MHz | |
| $t_{P,MIN}$ | Minimum pulse width | (S_LOAD, $\overline{\text{P\_LOAD}}$) | 50 | | | ns | |
| DC | Output duty cycle | | 45 | 50 | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.05 | | TBD | ns | 20% to 80% |
| $t_S$ | Setup Time | S_DATA to S_CLOCK<br>S_CLOCK to $\overline{\text{S\_LOAD}}$<br>M, N to $\overline{\text{P\_LOAD}}$ | 20<br>20<br>20 | | | ns<br>ns<br>ns | |
| $t_S$ | Hold Time | S_DATA to S_CLOCK<br>M, N to $\overline{\text{P\_LOAD}}$ | 20<br>20 | | | ns<br>ns | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ)[e] | | TBD | TBD | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | | ±25 | ps | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | | 10 | ms | |

a All AC characteristics are design targets and subject to change upon device characterization.
b AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
c The input frequency $f_{XTAL}$ and the PLL feedback divider M must match the VCO frequency range: $f_{VCO} = f_{XTAL} \cdot M \div 4$.
d The frequency of S_CLOCK is limited to 10 MHz in serial programming mode. S_CLOCK can be switched at higher frequencies when used as test clock in test mode 6. See application section for more details.
e See application section for a jitter calculation for other confidence factors than 1 σ.

**Programming the MPC9230**

Programming the MPC9230 amounts to properly configuring the internal PLL dividers to produce the desired synthesized frequency at the output. The output frequency can be represented by this formula:

$f_{OUT} = (f_{XTAL} \div 16) \cdot (4 \cdot M) \div (2 \cdot N)$ or (1)
$f_{OUT} = (f_{XTAL} \div 8) \cdot M \div N$ (2)

where $f_{XTAL}$ is the crystal frequency, M is the PLL feedback-divider and N is the PLL post-divider. The input frequency and the selection of the feedback divider M is limited by the VCO-frequency range. $f_{XTAL}$ and M must be configured to match the VCO frequency range of 800 to 1800 MHz in order to achieve stable PLL operation:

$M_{MIN} = 4 \cdot f_{VCO,MIN} \div f_{XTAL}$ and (3)
$M_{MAX} = 4 \cdot f_{VCO,MAX} \div f_{XTAL}$ (4)

For instance, the use of a 16 MHz input frequency requires the configuration of the PLL feedback divider between M=200 and M = 450. Table 8 shows the usable VCO frequency and M divider range for other example input frequencies. Assuming that a 16 MHz input frequency is used, equation (2) reduces to:

$f_{OUT} = 2 \cdot M \div N$ (5)

**Table 8. MPC9230 Frequency Operating Range**

| | | VCO frequency for an crystal interface frequency of | | | | | | Output frequency for $f_{XTAL}$=16 MHz and for N = | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **M** | **M[8:0]** | **10** | **12** | **14** | **16** | **18** | **20** | **1** | **2** | **4** | **8** |
| 160 | 010100000 | | | | | | 800 | | | | |
| 170 | 010101010 | | | | | | 850 | | | | |
| 180 | 010110100 | | | | | 810 | 900 | | | | |
| 190 | 010111110 | | | | | 855 | 950 | | | | |
| 200 | 011001000 | | | | 800 | 900 | 1000 | 400 | 200 | 100 | 50 |
| 210 | 011010010 | | | | 840 | 945 | 1050 | 420 | 210 | 105 | 52.5 |
| 220 | 011011100 | | | | 880 | 990 | 1100 | 440 | 220 | 110 | 55 |
| 230 | 011100110 | | | 805 | 920 | 1035 | 1150 | 460 | 230 | 115 | 57.5 |
| 240 | 011110000 | | | 840 | 960 | 1080 | 1200 | 480 | 240 | 120 | 60 |
| 250 | 011111010 | | | 875 | 100 | 1125 | 1250 | 500 | 250 | 125 | 62.5 |
| 260 | 100000100 | | | 910 | 1040 | 1170 | 1300 | 520 | 260 | 130 | 65 |
| 270 | 100001110 | | 810 | 945 | 1080 | 1215 | 1350 | 540 | 270 | 135 | 67.5 |
| 280 | 100011000 | | 840 | 980 | 1120 | 1260 | 1400 | 560 | 280 | 140 | 70 |
| 290 | 100100010 | | 870 | 1015 | 1160 | 1305 | 1450 | 580 | 290 | 145 | 72.5 |
| 300 | 100101100 | | 900 | 1050 | 1200 | 1350 | 1500 | 600 | 300 | 150 | 75 |
| 310 | 100110110 | | 930 | 1085 | 1240 | 1395 | 1550 | 620 | 310 | 155 | 77.5 |
| 320 | 101000000 | 800 | 960 | 1120 | 1280 | 1440 | 1600 | 640 | 320 | 160 | 80 |
| 330 | 101001010 | 825 | 990 | 1155 | 1320 | 1485 | 1650 | 660 | 330 | 165 | 82.5 |
| 340 | 101010100 | 850 | 1020 | 1190 | 1360 | 1530 | 1700 | 680 | 340 | 170 | 85 |
| 350 | 101011110 | 875 | 1050 | 1225 | 1400 | 1575 | 1750 | 700 | 350 | 175 | 87.5 |
| 360 | 101101000 | 900 | 1080 | 1260 | 1440 | 1620 | 1800 | 720 | 360 | 180 | 90 |
| 370 | 101110010 | 925 | 1110 | 1295 | 1480 | 1665 | | 740 | 370 | 185 | 92.5 |
| 380 | 101111100 | 950 | 1140 | 1330 | 1520 | 1710 | | 760 | 380 | 190 | 95 |
| 390 | 110000110 | 975 | 1170 | 1365 | 1560 | 1755 | | 780 | 390 | 195 | 97.5 |
| 400 | 110010000 | 1000 | 1200 | 1400 | 1600 | 1800 | | 800 | 400 | 200 | 100 |
| 410 | 110011010 | 1025 | 1230 | 1435 | 1640 | | | 820 | 410 | 205 | 102.5 |
| 420 | 110100100 | 1050 | 1260 | 1470 | 1680 | | | 840 | 420 | 210 | 105 |
| 430 | 110101110 | 1075 | 1290 | 1505 | 1720 | | | 860 | 430 | 215 | 107.5 |
| 440 | 110111000 | 1100 | 1320 | 1540 | 1760 | | | 880 | 440 | 220 | 110 |
| 450 | 111000010 | 1125 | 1350 | 1575 | 1800 | | | 900 | 450 | 225 | 112.5 |
| 510 | 111111110 | 1275 | 1530 | | | | | | | | |

Substituting N for the four available values for N (1, 2, 4, 8) yields:

**Table 9. Output Frequency Range for $f_{XTAL}$ = 16 MHz**

| N | | | $F_{OUT}$ | $F_{OUT}$ range | $F_{OUT}$ step |
|---|---|---|---|---|---|
| 1 | 0 | Value | | | |
| 0 | 0 | 1 | 2 · M | 400 - 800 MHz | 2 MHz |
| 0 | 1 | 2 | M | 200 - 400 MHz | 1 MHz |
| 1 | 0 | 4 | M÷2 | 100 - 200 MHz | 500 kHz |
| 1 | 1 | 8 | M÷4 | 50 - 100 MHz | 250 kHz |

3

### Example frequency calculation for an 16 MHz input frequency

If an output frequency of 131 MHz was desired the following steps would be taken to identify the appropriate M and N values. According to Table 9, 131 MHz falls in the frequency set by an value of 4 so N[1:0] = 10. For N = 4 the output frequency is $F_{OUT}$ = M ÷ 2 and M = $F_{OUT}$ x 2. Therefore M = 2 x 131 = 262, so M[8:0] = 010000011. Following this procedure a user can generate any whole frequency between 25 MHz and 900 MHz. Note than for N > 2 fractional values of can be realized. The size of the programmable frequency steps (and thus the indicator of the fractional output frequencies achievable) will be equal to:

$$f_{STEP} = f_{XTAL} \div 8 \div N \quad (6)$$

### Using the parallel and serial interface

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the $\overline{\text{P\_LOAD}}$ signal such that a LOW to HIGH transition will latch the information present on the M[8:0] and N[1:0] inputs into the M and N counters. When the $\overline{\text{P\_LOAD}}$ signal is LOW the input latches will be transparent and any changes on the M[8:0] and N[1:0] inputs will affect the FOUT output pair. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 14 bit shift register. Note that the $\overline{\text{P\_LOAD}}$ signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1 and M8). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 4 illustrates the timing diagram for both a parallel and a serial load of the MPC9230 synthesizer. M[8:0] and N[1:0] are normally specified once at power–up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine–tune the clock as the ability to control the serial interface becomes available.

### Using the test and diagnosis output TEST

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents $F_{OUT}$, the LVCMOS compatible TEST output is not able to toggle fast enough for higher output frequencies and should only be used for test and diagnosis. The T2, T1 and T0 control bits are preset to '000' when $\overline{\text{P\_LOAD}}$ is LOW so that the LVPECL compatible FOUT outputs are as jitter–free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin. Most of the signals available on the TEST output pin are useful only for performance verification of the MPC9230 itself. However the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MPC9230 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the $F_{OUT}$ differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving $F_{OUT}$ directly gives the user more control on the test clocks sent through the clock tree. Table 10 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 200 MHz. This means the fastest the $F_{OUT}$ pin can be toggled via the S_CLOCK is 50 MHz as the divide ratio of the Post-PLL divider is 4 (if N = 1). Note that the M counter output on the TEST output will not be a 50% duty cycle.

**Table 10. Test and Debug Configuration for TEST**

| T[2:0] | | | TEST output |
|---|---|---|---|
| T2 | T1 | T0 | |
| 0 | 0 | 0 | 14-bit shift register out[a] |
| 0 | 0 | 1 | Logic 1 |
| 0 | 1 | 0 | $f_{XTAL}$ ÷ 16 |
| 0 | 1 | 1 | M-Counter out |
| 1 | 0 | 0 | FOUT |
| 1 | 0 | 1 | Logic 0 |
| 1 | 1 | 0 | M-Counter out in PLL-bypass mode |
| 1 | 1 | 1 | FOUT ÷ 4 |

a. Clocked out at the rate of S_CLOCK

**Table 11. Debug Configuration for PLL bypass[a]**

| Output | Configuration |
|---|---|
| $F_{OUT}$ | S_CLOCK ÷ N |
| TEST | M-Counter out[b] |

a. T[2:0]=110. AC specifications do not apply in PLL bypass mode

b. clocked out at the rate of S_CLOCK÷(2·N)

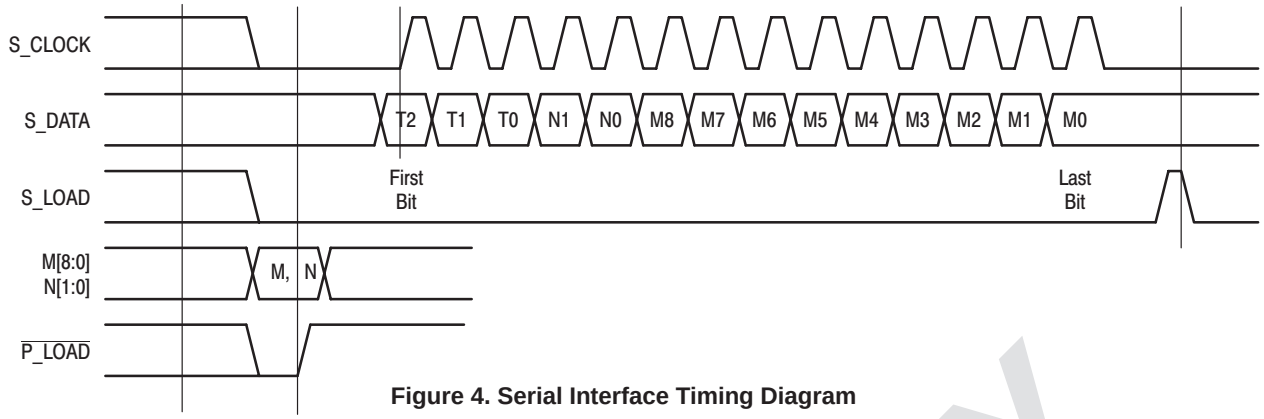



**Figure 4. Serial Interface Timing Diagram**



## Power Supply Filtering

The MPC9230 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC9230 provides separate power supplies for the digital circuitry ($V_{CC}$) and the internal PLL (VCC_PLL) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCC_PLL pin for the MPC9230. Figure 5 illustrates a typical power supply filter scheme. The MPC9230 is most susceptible to noise with spectral content in the 1 KHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the MPC9230 pin of the MPC9230. From the data sheet, the VCC_PLL current (the current sourced through the VCC_PLL pin) is typically TBD mA (TBD maximum), assuming that a minimum of 3.135V must be maintained on the VCC_PLL pin, very little DC voltage drop can be tolerated when a 3.3V $V_{CC}$ supply is used. The resistor shown in Figure 5 must have a resistance of TBD Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 KHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Generally, the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering. A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000μH choke will show a significant impedance at 10 KHz frequencies and above. Because of the current draw and the voltage that must be maintained on the VCC_PLL pin, a low DC resistance inductor is required (less than TBD Ω).

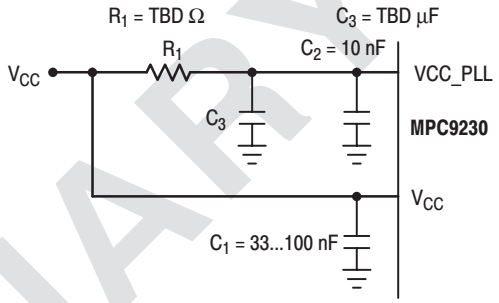



**Figure 5. $V_{CC\_PLL}$ Power Supply Filter**

## Layout Recommendations

The MPC9230 provides sub–nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 6 shows a representative board layout for the MPC9230. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 6 is the low impedance connections between VCC and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the MPC9230 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors. Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on–board oscillator. Although the MPC9230 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall perfor-

mance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

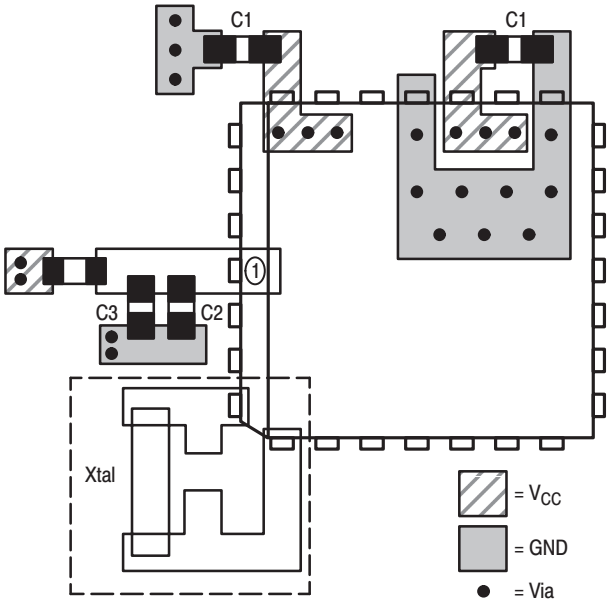



**Figure 6. PCB Board Layout Recommendation for the PLCC28 Package**

**Order Number: MPC9239/D**
**Rev 0, 11/2001**

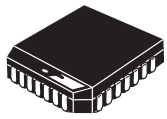
*Preliminary Information*

# 900 MHz Low Voltage PECL Clock Synthesizer

**MPC9239**

**900 MHZ LOW VOLTAGE CLOCK SYNTHESIZER**

3



**FN SUFFIX**
28–LEAD PLCC PACKAGE
CASE 776

The MPC9239 is a 3.3V compatible, PLL based clock synthesizer targeted for high performance clock generation in mid-range to high-performance telecom, networking and computing applications. With output frequencies from 50 MHz to 900 MHz and the support of differential PECL output signals the device meets the needs of the most demanding clock applications.

**Features**

- 50 MHz to 900 MHz synthesized clock output signal
- Differential PECL output
- LVCMOS compatible control inputs
- On-chip crystal oscillator for reference frequency generation
- Alternative LVCMOS compatible reference input
- 3.3V power supply
- Fully integrated PLL
- Minimal frequency overshoot
- Serial 3-wire programming interface
- Parallel programming interface for power-up
- 28 PLCC packaging
- SiGe Technology
- Ambient temperature range 0°C to + 70° C
- Pin and function compatible to the MC12439

**Functional Description**

The internal crystal oscillator uses the external quartz crystal as the basis of its frequency reference. The frequency of the internal crystal oscillator or external reference clock signal is multiplied by the PLL. The VCO within the PLL operates over a range of 800 to 1800 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The crystal oscillator frequency $f_{XTAL}$, the PLL feedback-divider M and the PLL post-divider N determine the output frequency.

The feedback path of the PLL is internal. The PLL adjusts the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve phase lock. The PLL will be stable if the VCO frequency is within the specified VCO frequency range (800 to 1800 MHz). The M-value must be programmed by the serial or parallel interface.

The PLL post-divider N is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle. The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated 50Ω to $V_{CC}$ – 2.0V. The positive supply voltage for the internal PLL is separated from the power supply for the core logic and output drivers to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[6:0] and N[1:0] inputs to configure the internal counters. It is recommended on system reset to hold the $\overline{\text{P\_LOAD}}$ input LOW until power becomes valid. On the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[6:0] and N[1:0] inputs prevent the LVCMOS compatible control inputs from floating. The serial interface centers on a twelve bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH–to–LOW edge of the S_LOAD input. See the programming section for more information. The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. In order to minimize the PLL jitter, it is recommended to avoid active signal on the TEST output. The PWR_DOWN pin, when asserted, will synchronously divide the FOUT by 16. The power down sequence is clocked by the PLL reference clock, thereby causing the frequency reduction to happen relatively slowly. Upon de–assertion of the PWR_DOWN pin, the FOUT input will step back up to its programmed frequency in four discrete increments.



**Rev 0**

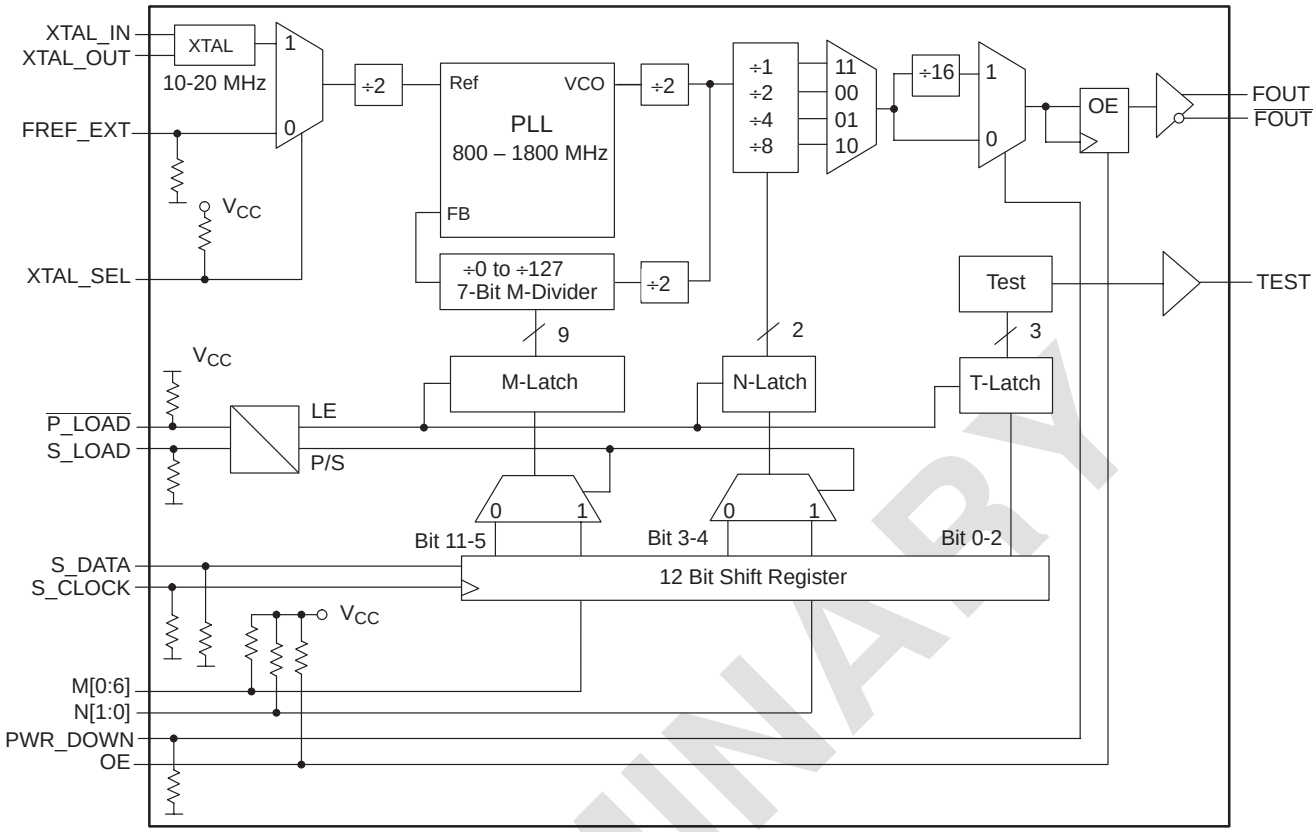



**Figure 1. MPC9239 Logic Diagram**

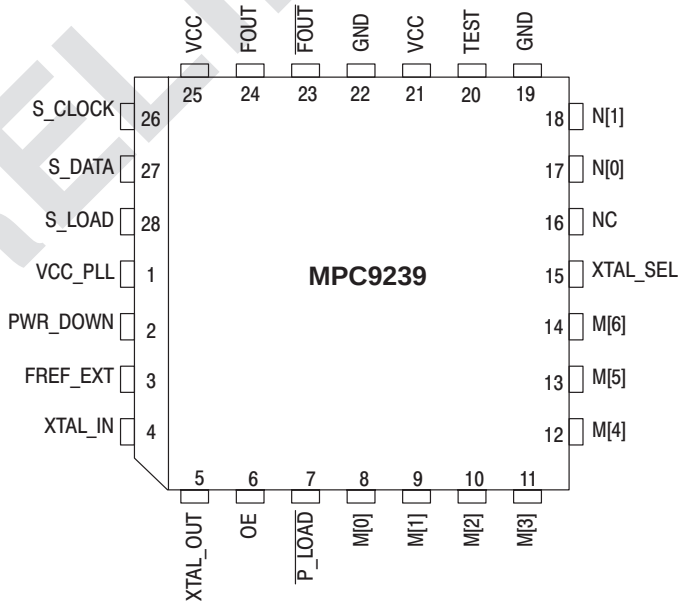



**Figure 2. MPC9239 28–Lead PLCC Pinout**
(Top View)

**Table 1. Pin Configuration**

| Pin | I/O | Default | Type | Function |
|---|---|---|---|---|
| XTAL_IN, XTAL_OUT | | | Analog | Crystal oscillator interface |
| FREF_EXT | Input | 0 | LVCMOS | Alternative PLL reference input |
| FOUT, $\overline{\text{FOUT}}$ | Output | | LVPECL | Differential clock output |
| TEST | Output | | LVCMOS | Test and device diagnosis output |
| XTAL_SEL | Input | 1 | LVCMOS | PLL reference select input |
| PWR_DOWN | Input | 0 | LVCMOS | Configuration input for power down mode. Assertion (deassertion) of power down will decrease (increase) the output frequency by a ratio of 16 in 4 discrete steps. PWR_DOWN assertion (deassertion) is synchronous to the input reference clock. |
| S_LOAD | Input | 0 | LVCMOS | Serial configuration control input. This inputs controls the loading of the configuration latches with the contents of the shift register. The latches will be transparent when this signal is high, thus the data must be stable on the high-to-low transition. |
| $\overline{\text{P\_LOAD}}$ | Input | 1 | LVCMOS | Parallel configuration control input. this input controls the loading of the configuration latches with the content of the parallel inputs (M and N). The latches will be transparent when this signal is low, thus the parallel data must be stable on the low-to-high transition of $\overline{\text{P\_LOAD}}$. $\overline{\text{P\_LOAD}}$ is state sensitive. |
| S_DATA | Input | 0 | LVCMOS | Serial configuration data input. |
| S_CLOCK | Input | 0 | LVCMOS | Serial configuration clock input. |
| M[0:6] | Input | 1 | LVCMOS | Parallel configuration for PLL feedback divider (M). M is sampled on the low-to-high transition of $\overline{\text{P\_LOAD}}$. |
| N[1:0] | Input | 1 | LVCMOS | Parallel configuration for Post-PLL divider (N). N is sampled on the low-to-high transition of $\overline{\text{P\_LOAD}}$ |
| OE | Input | 1 | LVCMOS | Output enable (active high) The output enable is synchronous to the output clock to eliminate the possibility of runt pulses on the FOUT output. OE = L low stops FOUT in the logic low state (FOUT = L, $\overline{\text{FOUT}}$ = H). |
| GND | Supply | | Ground | Negative power supply (GND). |
| $V_{CC}$ | Supply | | $V_{CC}$ | Positive power supply for I/O and core. All $V_{CC}$ pins must be connected to the positive power supply for correct operation. |
| VCC_PLL | Supply | | $V_{CC}$ | PLL positive power supply (analog power supply). |

**Table 2. Output frequency range and PLL Post-divider N**

| PWR_DOWN | N | | VCO Output frequency division | FOUT frequency range |
|---|---|---|---|---|
| | 1 | 0 | | |
| 0 | 0 | 0 | 2 | 200 - 450 MHz |
| 0 | 0 | 1 | 4 | 100 - 225 MHz |
| 0 | 1 | 0 | 8 | 50 - 112.5 MHz |
| 0 | 1 | 1 | 1 | 400 - 900 MHz |
| 1 | 0 | 0 | 32 | 12.5 - 28.125 MHz |
| 1 | 0 | 1 | 64 | 6.25 - 14.0625 MHz |
| 1 | 1 | 0 | 128 | 3.125 - 7.03125 MHz |
| 1 | 1 | 1 | 16 | 25 - 56.25 MHz |

**Table 3. Function Table**

| Input | 0 | 1 |
|---|---|---|
| XTAL_SEL | FREF_EXT | XTAL interface |
| OE | Outputs disabled. FOUT is stopped in the logic low state (FOUT = L, $\overline{FOUT}$ = H) | Outputs enabled |
| PWR_DOWN | Output divider ÷ 1 | Output divider ÷16 |

**Table 4. General Specifications**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output termination voltage | | $V_{CC}$ - 2 | | V | |
| MM | ESD protection (Machine model) | 200 | | | V | |
| HBM | ESD protection (Human body model) | 2000 | | | V | |
| LU | Latch-up immunity | 200 | | | mA | |
| $C_{IN}$ | Input capacitance | | 4.0 | | pF | Inputs |

**Table 5. Absolute Maximum Ratings[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -65 | 125 | °C | |

a Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 6. DC Characteristics** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = 0°C to + 70°C)[a]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| LVCMOS control inputs (FREF_EXT, PWR_DOWN, XTAL_SEL, $\overline{\text{P\_LOAD}}$, S_LOAD, S_DATA, S_CLOCK, M[0:8], N[0:1], OE) | | | | | | |
| $V_{IH}$ | Input high voltage | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | | | 0.8 | V | LVCMOS |
| $I_{IN}$ | Input Current[b] | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| Differential clock output FOUT[c] | | | | | | |
| $V_{OH}$ | Output High Voltage | 2.28 | | 2.56 | V | LVPECL |
| $V_{OL}$ | Output Low Voltage | 1.35 | | 1.70 | V | LVPECL |
| Test and diagnosis output TEST | | | | | | |
| $V_{OH}$ | Output High Voltage | 2.0 | | | V | $I_{OH}$ =-0.8 mA |
| $V_{OL}$ | Output Low Voltage | | | 0.55 | V | $I_{OL}$ = 0.8 mA |
| Supply current | | | | | | |
| $I_{CC\_PLL}$ | Maximum PLL Supply Current | | | 20 | mA | $V_{CC\_PLL}$ Pins |
| $I_{CC}$ | Maximum Supply Current | | | 110 | mA | All $V_{CC}$ Pins |

a. All AC characteristics are design targets and subject to change upon device characterization.
b. Inputs have pull-down resistors affecting the input current.
c. Outputs terminated 50Ω to $V_{TT}$ = $V_{CC}$ - 2V.

**Table 7. AC Characteristics** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = 0°C to + 70°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{XTAL}$ | Crystal interface frequency range | | 10 | | 20 | MHz | |
| $f_{VCO}$ | VCO frequency range[c] | | 800 | | 1800 | MHz | |
| $f_{MAX}$ | Output Frequency | N = 11 (÷1)<br>N = 00 (÷2)<br>N = 01 (÷4)<br>N = 10 (÷8) | 400<br>200<br>100<br>50 | | 900<br>450<br>225<br>112.5 | MHz<br>MHz<br>MHz<br>MHz | PWR_DOWN = 0 |
| $f_{S\_CLOCK}$ | Serial interface programming clock frequency[d] | | 0 | | 10 | MHz | |
| $t_{P,MIN}$ | Minimum pulse width | (S_LOAD, $\overline{\text{P\_LOAD}}$) | 50 | | | ns | |
| DC | Output duty cycle | | 45 | 50 | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.05 | | TBD | ns | 20% to 80% |
| $t_S$ | Setup Time | S_DATA to S_CLOCK<br>S_CLOCK to S_LOAD<br>M, N to $\overline{\text{P\_LOAD}}$ | 20<br>20<br>20 | | | ns<br>ns<br>ns | |
| $t_S$ | Hold Time | S_DATA to S_CLOCK<br>M, N to $\overline{\text{P\_LOAD}}$ | 20<br>20 | | | ns<br>ns | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ)[e] | | TBD | TBD | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | | ±25 | ps | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | | 10 | ms | |

a. All AC characteristics are design targets and subject to change upon device characterization.
b. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
c. The input frequency $f_{XTAL}$ and the PLL feedback divider M must match the VCO frequency range: $f_{VCO} = f_{XTAL} \cdot 2 \cdot M$.
d. The frequency of S_CLOCK is limited to 10 MHz in serial programming mode. S_CLOCK can be switched at higher frequencies when used as test clock in test mode 6. See application section for more details.
e. See application section for a jitter calculation for other confidence factors than 1 σ.

**Table 8. MPC9239 Frequency Operating Range**

| | | VCO frequency for an crystal interface frequency of | | | | | | Output frequency for $f_{XTAL}$=16 MHz and for N = | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **M** | **M[6:0]** | **10** | **12** | **14** | **16** | **18** | **20** | **1** | **2** | **4** | **8** |
| 20 | 0010100 | | | | | | 800 | | | | |
| 21 | 0010101 | | | | | | 840 | | | | |
| 22 | 0010110 | | | | | | 880 | | | | |
| 23 | 0010111 | | | | | 828 | 920 | | | | |
| 24 | 0011000 | | | | | 864 | 960 | | | | |
| 25 | 0011001 | | | | 800 | 900 | 1000 | 400 | 200 | 100 | 50 |
| 26 | 0011010 | | | | 832 | 936 | 1040 | 416 | 208 | 104 | 52 |
| 27 | 0011011 | | | | 864 | 972 | 1080 | 432 | 216 | 108 | 54 |
| 28 | 0011100 | | | 812 | 896 | 1008 | 1120 | 448 | 224 | 112 | 56 |
| 29 | 0011101 | | | 840 | 928 | 1044 | 1160 | 464 | 232 | 116 | 58 |
| 30 | 0011110 | | | 875 | 960 | 1080 | 1200 | 480 | 240 | 120 | 60 |
| 31 | 0011111 | | | 868 | 992 | 1116 | 1240 | 496 | 248 | 124 | 62 |
| 32 | 0100000 | | | 896 | 1024 | 1152 | 1280 | 512 | 256 | 128 | 64 |
| 33 | 0100001 | | | 924 | 1056 | 1188 | 1320 | 528 | 264 | 132 | 66 |
| 34 | 0100010 | | 816 | 952 | 1088 | 1224 | 1360 | 544 | 272 | 136 | 68 |
| 35 | 0100011 | | 840 | 980 | 1120 | 1260 | 1400 | 560 | 280 | 140 | 70 |
| 36 | 0100100 | | 864 | 1008 | 1152 | 1296 | 1440 | 576 | 288 | 144 | 72 |
| 37 | 0100101 | | 888 | 1036 | 1184 | 1332 | 1480 | 592 | 296 | 148 | 74 |
| 38 | 0100110 | | 912 | 1064 | 1216 | 1368 | 1520 | 608 | 304 | 152 | 76 |
| 39 | 0100111 | | 936 | 1092 | 1248 | 1404 | 1560 | 624 | 312 | 156 | 78 |
| 40 | 0101000 | 800 | 960 | 1120 | 1280 | 1440 | 1600 | 640 | 320 | 160 | 80 |
| 41 | 0101001 | 820 | 984 | 1148 | 1312 | 1476 | 1640 | 656 | 328 | 164 | 82 |
| 42 | 0101010 | 840 | 1008 | 1176 | 1344 | 1512 | 1680 | 672 | 336 | 168 | 84 |
| 43 | 0101011 | 860 | 1032 | 1204 | 1376 | 1548 | 1720 | 688 | 344 | 172 | 86 |
| 44 | 0101100 | 880 | 1056 | 1232 | 1408 | 1584 | 1760 | 704 | 352 | 176 | 88 |
| 45 | 0101101 | 900 | 1080 | 1260 | 1440 | 1620 | 1800 | 720 | 360 | 180 | 90 |
| 46 | 0101110 | 920 | 1104 | 1288 | 1472 | 1656 | | 736 | 368 | 184 | 92 |
| 47 | 0101111 | 940 | 1128 | 1316 | 1504 | 1692 | | 752 | 376 | 188 | 94 |
| 48 | 0110000 | 960 | 1152 | 1344 | 1536 | 1728 | | 768 | 384 | 192 | 96 |
| 49 | 0110001 | 980 | 1176 | 1372 | 1568 | 1764 | | 784 | 392 | 196 | 98 |
| 50 | 0110010 | 1000 | 1200 | 1400 | 1600 | 1800 | | 800 | 400 | 200 | 100 |
| 51 | 0110011 | 1020 | 1224 | 1428 | 1632 | | | 816 | 408 | 204 | 102 |
| 52 | 0110100 | 1040 | 1248 | 1456 | 1664 | | | 832 | 416 | 208 | 104 |
| 53 | 0110101 | 1060 | 1272 | 1484 | 1696 | | | 848 | 424 | 212 | 106 |
| 54 | 0110110 | 1080 | 1296 | 1512 | 1728 | | | 864 | 432 | 216 | 108 |
| 55 | 0110111 | 1100 | 1320 | 1540 | 1760 | | | 880 | 440 | 220 | 110 |
| 56 | 0111000 | 1120 | 1344 | 1568 | 1792 | | | 896 | 448 | 224 | 112 |
| 57 | 0111001 | 1140 | 1368 | 1596 | | | | | | | |
| 58 | 0111010 | 1160 | 1392 | 1624 | | | | | | | |
| 59 | 0111011 | 1180 | 1416 | 1652 | | | | | | | |
| 60 | 0111100 | 1200 | 1440 | 1680 | | | | | | | |
| 61 | 0111101 | 1220 | 1488 | 1736 | | | | | | | |
| 62 | 0111110 | 1260 | 1512 | 1764 | | | | | | | |
| 63 | 0111111 | 1260 | 1512 | 1764 | | | | | | | |
| 64 | 1000000 | 1280 | 1536 | 1792 | | | | | | | |
| ... | | ... | ... | ... | | | | | | | |

### Programming the MPC9239

Programming the MPC9239 amounts to properly configuring the internal PLL dividers to produce the desired synthesized frequency at the output. The output frequency can be represented by this formula:

$$f_{OUT} = (f_{XTAL} \div 2) \cdot (M \cdot 4) \div (N \cdot 2) \text{ or} \quad (1)$$
$$f_{OUT} = f_{XTAL} \cdot 2 \cdot M \div N \quad (2)$$

where $f_{XTAL}$ is the crystal frequency, M is the PLL feedback-divider and N is the PLL post-divider. The input frequency and the selection of the feedback divider M is limited by the VCO-frequency range. $f_{XTAL}$ and M must be configured to match the VCO frequency range of 800 to 1800 MHz in order to achieve stable PLL operation:

$$M_{MIN} = f_{VCO,MIN} \div (2 \cdot f_{XTAL}) \text{ and} \quad (3)$$
$$M_{MAX} = f_{VCO,MAX} \div (2 \cdot f_{XTAL}) \quad (4)$$

For instance, the use of a 16 MHz input frequency requires the configuration of the PLL feedback divider between M = 25 and M = 56. Table 8 shows the usable VCO frequency and M divider range for other example input frequencies.
Assuming that a 16 MHz input frequency is used, equation (2) reduces to:

$$f_{OUT} = 16\ M \div N \quad (5)$$

Substituting N for the four available values for N (1, 2, 4, 8) yields:

**Table 9. Output Frequency Range for $f_{XTAL}$ = 16 MHz**

| N | | | $F_{OUT}$ | $F_{OUT}$ range | $F_{OUT}$ step |
|---|---|---|---|---|---|
| 1 | 0 | Value | | | |
| 0 | 0 | 2 | 8·M | 200-450 MHz | 8 MHz |
| 0 | 1 | 4 | 4·M | 100-225 MHz | 4 MHz |
| 1 | 0 | 8 | 2·M | 50-112.5 MHz | 2 MHz |
| 1 | 1 | 1 | 16·M | 400-900 MHz | 16 MHz |

### Example calculation for an 16 MHz input frequency

For example, if an output frequency of 384 MHz was desired, the following steps would be taken to identify the appropriate M and N values. 384 MHz falls within the frequency range set by an N value of 2, so N[1:0]=00. For N = 2, FOUT = 8·M and M = FOUT÷8. Therefore, M = 384 ÷ 8 = 48, so M[6:0] = 0110000. Following this procedure a user can generate any whole frequency between 50 MHz and 900 MHz. The size of the programmable frequency steps will be equal to:

$$f_{STEP} = f_{XTAL} \div N \quad (6)$$

### Using the parallel and serial interface

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the $\overline{\text{P\_LOAD}}$ signal such that a LOW to HIGH transition will latch the information present on the M[6:0] and N[1:0] inputs into the M and N counters. When the $\overline{\text{P\_LOAD}}$ signal is LOW the input latches will be transparent and any changes on the M[6:0] and N[1:0] inputs will affect the FOUT output pair. To use the serial port the S_CLOCK signal samples the information on the $\overline{\text{S\_DATA}}$ line and loads it into a 12 bit shift register. Note that the $\overline{\text{P\_LOAD}}$ signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two, and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1 and M6). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 3 illustrates the timing diagram for both a parallel and a serial load of the MPC9239 synthesizer.

M[6:0] and N[1:0] are normally specified once at power–up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine–tune the clock as the ability to control the serial interface becomes available.

### Using the test and diagnosis output TEST

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents FOUT, the LVCMOS output is not able to toggle fast enough for higher output frequencies and should only be used for test and dignosis.

The T2, T1 and T0 control bits are preset to ‘000’ when $\overline{\text{P\_LOAD}}$ is LOW so that the PECL FOUT outputs are as jitter–free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Most of the signals available on the TEST output pin are useful only for performance verification of the MPC9239 itself. However, the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MPC9239 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the FOUT differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clocktree shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 200 MHz. This means the fastest the FOUT pin can be toggled via the S_CLOCK is 100 MHz as the divide ratio of the Post-PLL divider is 2 (if N = 1). Note that the M counter output on the TEST output will not be a 50% duty cycle.

**Table 10. Test and Debug Configuration for TEST**

| T[2:0] | | | TEST output |
|---|---|---|---|
| T2 | T1 | T0 | |
| 0 | 0 | 0 | 12-bit shift register out[a] |
| 0 | 0 | 1 | Logic 1 |
| 0 | 1 | 0 | $f_{XTAL} \div 2$ |
| 0 | 1 | 1 | M-Counter out |
| 1 | 0 | 0 | FOUT |
| 1 | 0 | 1 | Logic 0 |
| 1 | 1 | 0 | M-Counter out in PLL-bypass mode |
| 1 | 1 | 1 | FOUT ÷ 4 |

a. Clocked out at the rate of S_CLOCK

**Table 11. Debug Configuration for PLL bypass[a]**

| Output | Configuration |
|---|---|
| FOUT | S_CLOCK ÷ N |
| TEST | M-Counter out[b] |

a. T[2:0] = 110. AC specifications do not apply in PLL bypass mode

b. Clocked out at the rate of S_CLOCK ÷ (2·N)

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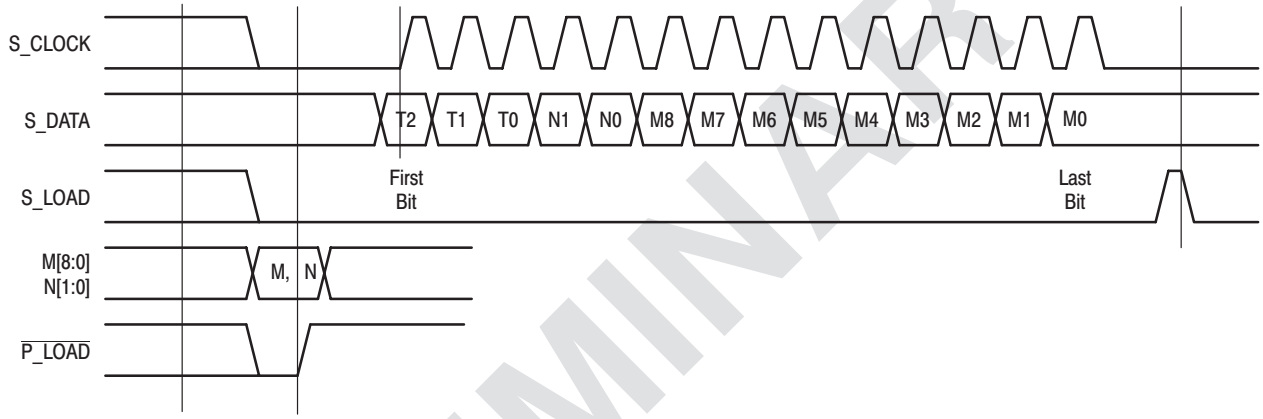


**Figure 3. Serial Interface Timing Diagram**



**Power Supply Filtering**

The MPC9239 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC9239 provides separate power supplies for the digital circuitry (VCC) and the internal PLL (VCC_PLL) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCC_PLL pin for the MPC9239. Figure 4 illustrates a typical power supply filter scheme. The MPC9239 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the MPC9239 pin of the MPC9239. From the data sheet, the VCC_PLL current (the current sourced through the VCC_PLL pin) is typically TBD mA (TBD maximum), assuming that a minimum of 3.135V must be maintained on the VCC_PLL pin, very little DC voltage drop can be tolerated when a 3.3V VCC supply is used. The resistor shown in Figure 4 must have a resistance of TBD Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Generally, the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering. A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000 μH choke will show a significant impedance at 10 kHz frequencies and above. Because of the current draw and the voltage that must be maintained on the VCC_PLL pin, a low DC resistance inductor is required (less than TBD Ω).

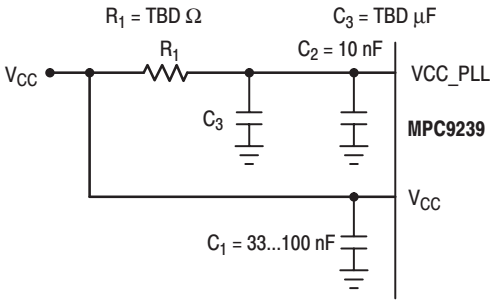


**Figure 4. $V_{CC\_PLL}$ Power Supply Filter**

### Layout Recommendations

The MPC9239 provides sub–nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 5 shows a representative board layout for the MPC9239. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 5 is the low impedance connections between $V_{CC}$ and GND for the bypass capacitors.

Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the MPC9239 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors. Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on–board oscillator. Although the MPC9239 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

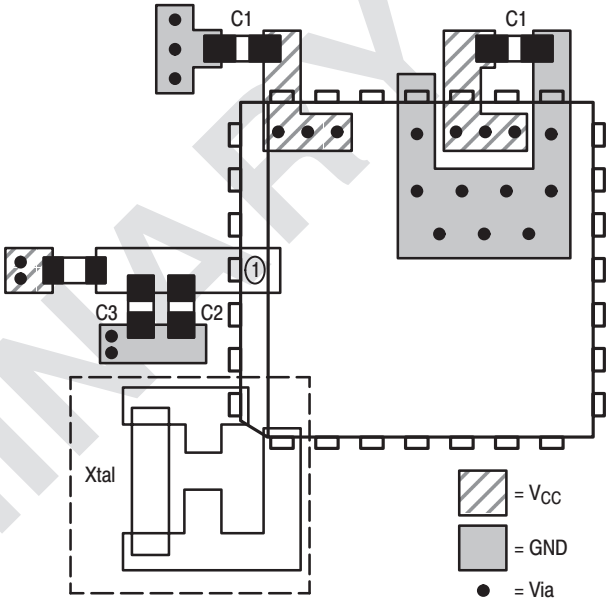


**Figure 5. PCB Board Layout Recommendation for the PLCC28 Package**

*Product Preview*

# HSTL Low Voltage Differential Clock

**MPC998**

**HSTL LOW VOLTAGE DIFFERENTIAL CLOCK SYNTHESIZER FOR 520 – 840 MHZ**

The MPC998 is a low voltage 3.3V, HSTL differential clock synthesizer. The clock is designed to support single and multiple processor systems requiring HSTL differential inputs. The MPC998 supports two differential HSTL output pairs that may be operated from 520 MHz to 840 MHz.

**Features:**

- 2 clock outputs: (PCLK0 and PCLK1), each fully selectable
- Fully integrated PLL
- Output frequencies from 520 MHz to 840 MHz
- HSTL outputs
- HSTL and LVPECL reference clocks
- 32 lead LQFP packaging

The fully integrated Phase Locked Loop multiplies the HSTL_CLK input or the PECL_CLK input frequency to the desired processor clock frequency.

The PLL may be bypassed for test purposes such that the PCLK outputs are fed directly from the HSTL_CLK or PECL_CLK input.

All outputs are HSTL. The PCLK outputs are capable of driving 25Ω to ground with at least 600mV p-p signals. The EXTFB_OUT is capable of driving 50Ω ground with at least a 600 mV p-p signal. For on-chip power reduction, the outputs are powered from 1.8V external supply. For zero delay applications the buffer can operate with either external or internal feedback.

**FA SUFFIX**
LQFP PACKAGE
CASE 873A–02

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.
**Rev 1**

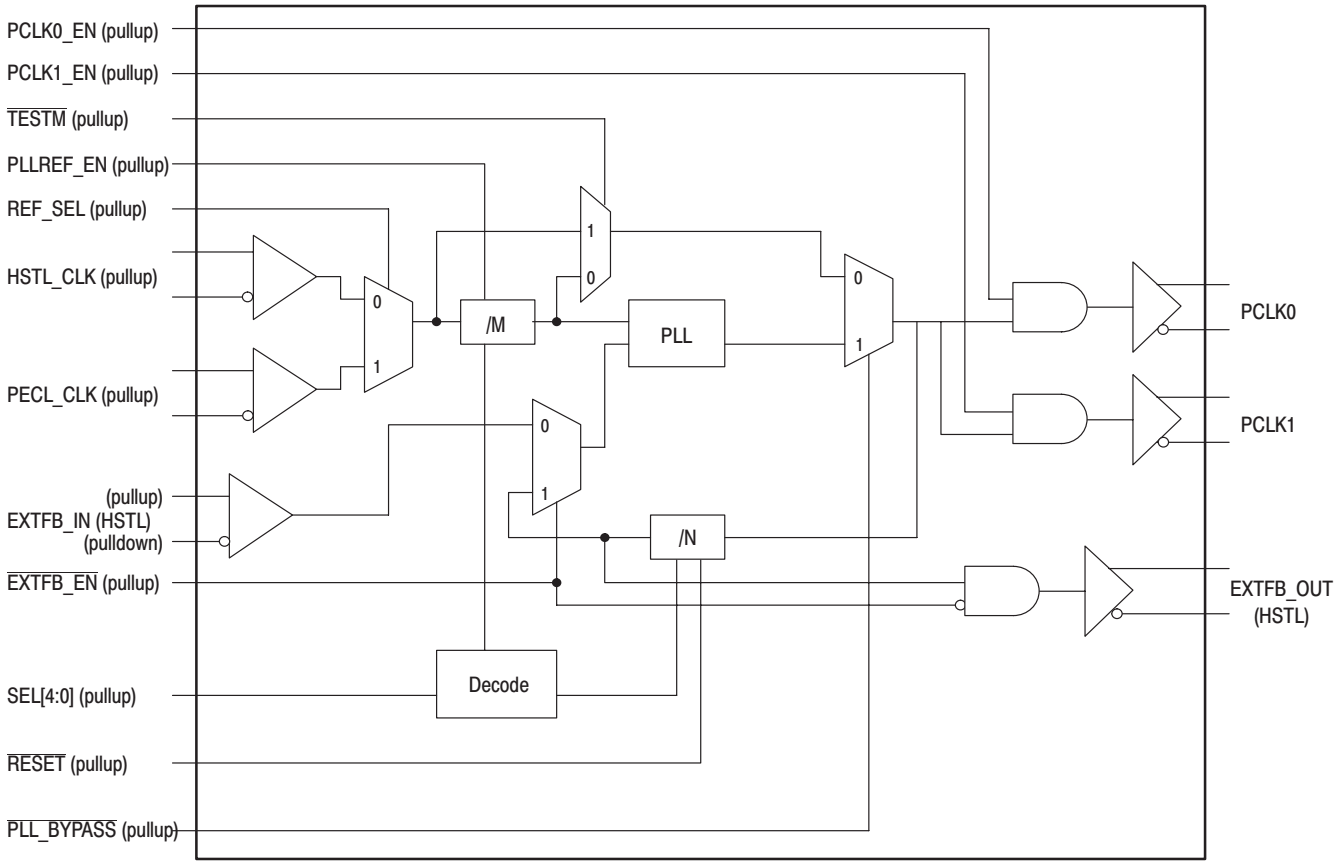


**Figure 1. MPC998 Logic Diagram**

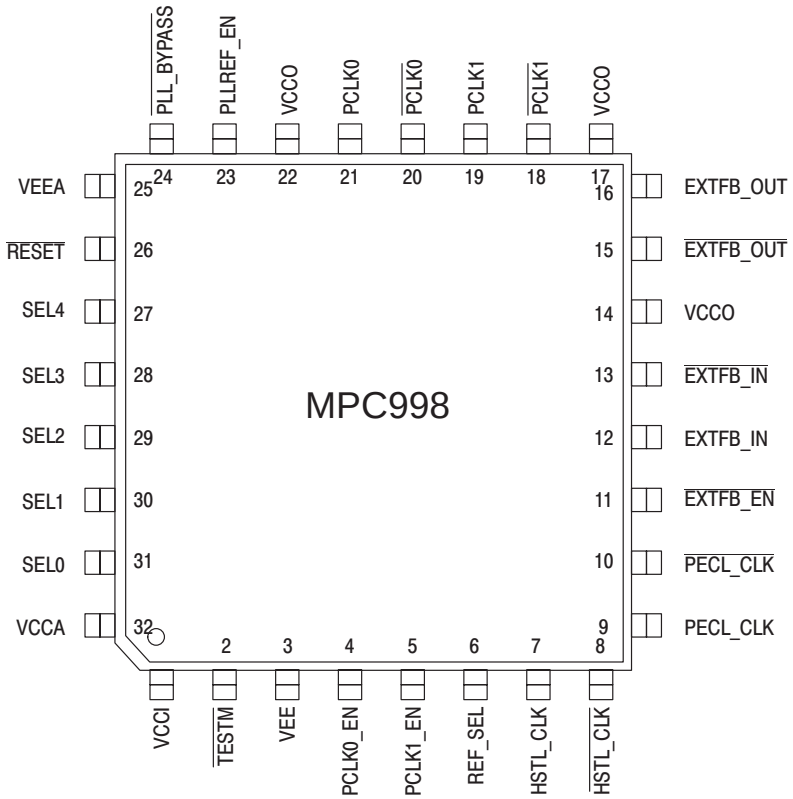


**Figure 2. 32 Lead Package Pinout (Top View)**

**PIN CONFIGURATION**

| Pin # | Pin | I/O Type | Type | Description |
|---|---|---|---|---|
| 1 | VCCI | Power | Power Supply | 3.3 V |
| 2 | $\overline{\text{TESTM}}$ | Input | LVCMOS | M divider test pins |
| 3 | VEE | Power (GND) | Ground | Digital GND |
| 4 | PCLK0_EN | Input | LVCMOS | PCLK0 enable |
| 5 | PCLK1_EN | Input | LVCMOS | PCLK1 enable |
| 6 | REF_SEL | Input | LVCMOS | Selects the PLL input reference clock |
| 7 | HSTL_CLK | Input | Differential HSTL | PLL reference clock input |
| 8 | $\overline{\text{HSTL\_CLK}}$ | Input | Differential HSTL | PLL reference clock input |
| 9 | PECL_CLK | Input | Differential LVPECL | PLL reference clock input |
| 10 | $\overline{\text{PECL\_CLK}}$ | Input | Differential LVPECL | PLL reference clock input |
| 11 | $\overline{\text{EXTFB\_EN}}$ | Input | LVCMOS | External feedback enable |
| 12 | EXTFB_IN | Input | Differential HSTL | External feedback input |
| 13 | $\overline{\text{EXTFB\_IN}}$ | Input | Differential HSTL | External feedback input |
| 14 | VCCO | Power | Power Supply | Output buffers power supply |
| 15 | $\overline{\text{EXTFB\_OUT}}$ | Output | Differential HSTL | External feedback output clock |
| 16 | EXTFB_OUT | Output | Differential HSTL | External feedback output clock |
| 17 | VCCO | Power | Power Supply | Ouput buffers power supply |
| 18 | $\overline{\text{PCLK1}}$ | Output | Differential HSTL | Output clock 1 |
| 19 | PCLK1 | Output | Differential HSTL | Output clock 1 |
| 20 | $\overline{\text{PCLK0}}$ | Output | Differential HSTL | Output clock 0 |
| 21 | PCLK0 | Output | Differential HSTL | Output clock 0 |
| 22 | VCCO | Power | Power Supply | Ouput buffers power supply |
| 23 | PLLREF_EN | Input | LVCMOS | PLL reference enable |
| 24 | $\overline{\text{PLL\_BYPASS}}$ | Input | LVCMOS | Input signal PLL bypass |
| 25 | VEEA | Power (GND) | Ground | Analog GND for PLL |
| 26 | $\overline{\text{RESET}}$ | Input | LVCMOS | PLL bypass reset (for test use) |
| 27 | SEL[4] | Input | LVCMOS | Selection of input and feedback frequency |
| 28 | SEL[3] | Input | LVCMOS | Selection of input and feedback frequency |
| 29 | SEL[2] | Input | LVCMOS | Selection of input and feedback frequency |
| 30 | SEL[1] | Input | LVCMOS | Selection of input and feedback frequency |
| 31 | SEL[0] | Input | LVCMOS | Selection of input and feedback frequency |
| 32 | VCCA | Power | Power Supply | 3.3 V filtered for PLL (PLL power supply) |

**FREQUENCY SELECTION TABLE**

| SEL | | | | | Input Divide | Feedback Divide |
|---|---|---|---|---|---|---|
| **4** | **3** | **2** | **1** | **0** | **M** | **N** |
| 0 | 0 | 0 | 0 | 0 | 5 | 24 |
| 0 | 0 | 0 | 0 | 1 | 5 | 25 |
| 0 | 0 | 0 | 1 | 0 | 5 | 26 |
| 0 | 0 | 0 | 1 | 1 | 5 | 27 |
| 0 | 0 | 1 | 0 | 0 | 5 | 28 |
| 0 | 0 | 1 | 0 | 1 | 5 | 29 |
| 0 | 0 | 1 | 1 | 0 | 5 | 30 |
| 0 | 0 | 1 | 1 | 1 | 5 | 31 |
| 0 | 1 | 0 | 0 | 0 | 5 | 32 |
| 0 | 1 | 0 | 0 | 1 | 5 | 33 |
| 0 | 1 | 0 | 1 | 0 | 5 | 34 |
| 0 | 1 | 0 | 1 | 1 | 5 | 35 |
| 0 | 1 | 1 | 0 | 0 | 5 | 36 |
| 0 | 1 | 1 | 0 | 1 | 5 | 37 |
| 0 | 1 | 1 | 1 | 0 | 5 | 38 |
| 0 | 1 | 1 | 1 | 1 | 5 | 39 |
| 1 | 0 | 0 | 0 | 0 | 5 | 40 |
| 1 | 0 | 0 | 0 | 1 | 5 | 41 |
| 1 | 0 | 0 | 1 | 0 | 5 | 42 |
| 1 | 0 | 0 | 1 | 1 | 5 | 43 |
| 1 | 0 | 1 | 0 | 0 | 5 | 44 |
| 1 | 0 | 1 | 0 | 1 | 5 | 45 |
| 1 | 0 | 1 | 1 | 0 | 5 | 46 |
| 1 | 0 | 1 | 1 | 1 | 5 | 47 |
| 1 | 1 | 0 | 0 | 0 | 5 | 48 |
| 1 | 1 | 0 | 0 | 1 | 5 | 49 |
| 1 | 1 | 0 | 1 | 0 | 5 | 50 |
| 1 | 1 | 0 | 1 | 1 | 5 | 51 |
| 1 | 1 | 1 | 0 | 0 | 5 | 52 |
| 1 | 1 | 1 | 0 | 1 | 5 | 53 |
| 1 | 1 | 1 | 1 | 0 | 5 | 54 |
| 1 | 1 | 1 | 1 | 1 | 5 | 55 |

**FUNCTION TABLE (CONTROLS)**

| Control Pin | 0 | 1 |
|---|---|---|
| REF_SEL | HSTL_CLK | PECL_CLK |
| $\overline{\text{TESTM}}$ | M divider test mode enabled | Reference fed to Bypass mux |
| PLLREF_EN | Disable the input to the PLL and reset the M divider | Enable the input to the PLL |
| $\overline{\text{PLL\_BYPASS}}$ | Outputs fed by input reference or M divider | Outputs fed by VCO |
| $\overline{\text{EXTFB\_EN}}$ | External feedback enabled | Internal feedback enabled |
| PCLK0_EN | PCLK0 = low, $\overline{\text{PCLK0}}$ = high | PCLK0 = high, $\overline{\text{PCLK0}}$ = low |
| PCLK1_EN | PCLK1 = low, $\overline{\text{PCLK1}}$ = high | PCLK1 = high, $\overline{\text{PCLK1}}$ = low |
| $\overline{\text{RESET}}$ | Resets feedback N divider | Feedback enabled |
| SEL[4:0] | See Selection Frequency Table | |

**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| VCC | Supply Voltage | -0.5 | 4.4 | V | |
| VCCO | Output Supply Voltage | -0.5 | 4.4 | V | |
| VIN | Input Voltage | -0.5 | VCC+0.3 | V | |
| IIN | Input Current | -1 | 1 | mA | |
| TS | Storage temperature | -50 | 150 | °C | |

NOTE: Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

**DC CHARACTERISTICS** ($V_{CCA}$=$V_{CCI}$ = 3.3V ± 5%, $V_{CCO}$ = 1.7 to 2.1V, TA = 0 to 70°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| VIH | Input high voltage | 2.0 | | VCCI | V | LVCMOS |
| VIL | Input low voltage | 0.0 | | 0.8 | V | LVCMOS |
| VCMR | Input high voltage[a] | 1 | | VCCI - 0.3 | V | LVPECL |
| VPP | Input low voltage[a] | 0.5 | | 1 | V | LVPECL[b] |
| $V_{IN}$ (dc) | DC input signal voltage | -0.3 | | 1.45 | V | HSTL[c] |
| $V_{DIF}$(dc) | DC differential input voltage | 0.4 | | 1.75 | V | HSTL[d] |
| $V_{CM}$(dc) | DC common mode input voltage | 0.4 | | 1.0 | V | HSTL[e] |
| VOH | Output High Voltage | $V_X$ + 0.3 | $V_X$ + 0.5 | 1.4 | V | HSTL[f,a] |
| VOL | Output Low Voltage | 0.0 | $V_X$ - 0.5 | $V_X$ - 0.3 | V | HSTL[f] |
| ICCI | Core Supply Current | | | 140 | mA | |
| ICCA | PLL Supply Current | | 15 | 20 | mA | |
| ICCO | Output Supply Current | | 150 | | mA | Note [g] |
| $Theta_{JA}$ | Junction to ambient thermal resistance | | 53 | | °C/W | Note [h] |

a) DC levels will vary 1:1 with VCC.
b) VPP minimum and maximum required to maintain AC specifications. Actual device function will tolerate minimum VPP of 200mV.
c) $V_{IN}$ (dc) specifies the maximum allowable dc excursion of each differential input.
d) $V_{DIF}$ (dc) specifies the minimum input differential voltage ($V_{TR}$ - $V_{CP}$) required for switching, where $V_{TR}$ is the "true" input signal and $V_{CP}$ is the "complement" input signal.
e) $V_{CM}$(dc) specifies the maximum allowable range of input signal crosspoint voltage
f) $V_X$ is the differential output crosspoint voltage defined in the "AC CHARACTERISTICS" section
g) 2 PCLK into 25Ω and 1 EXTFB into 50Ω
h) Measured with 1.3M/s (250fpm) airflow

**AC CHARACTERISTICS** ($V_{CCA}$ = $V_{CCI}$ = 3.3V ± 5%, $V_{CCO}$ = 1.7V to 2.1V, $T_A$ = 0 to 70°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| fref | Input Frequency | | 100 - 125 | | MHz | |
| fMAX | Maximum Output Frequency | 520 | | 840 | MHz | Note [b] |
| tsk(o) | Skew Error (PCLK) | | | 35 | ps | Note [c] |
| $t_{jit(0)}$ | Phase jitter (IO jitter) | | | output period / 2 | | Note [c] |
| $t_{jit(cc)}$ | Cycle–to–cycle jitter (full period) | | | 5% | | Note [c, e] |
| $t_{jit(1/2per)}$ | Cycle–to–cycle jitter (half period) | | | 6% | | Note [c, d] |
| $V_{DIFout}$ | Differential Output pk–pk swing | 0.6 | | | V | For all HSTL output pairs |
| Vx | Differential output crosspoint voltage | 0.68 | | 0.9 | V | For all HSTL output pairs |
| $t_{lock}$ | Maximum PLL lock time | | | 10 | ms | |

a) All PCLK outputs are terminated in 25Ω to ground, EXTFB_OUT is terminated in 50Ω to ground (applies to all measurements).
b) With PLL active but in bypass mode, fref Max is limited by input buffer; best performance is expected with PECL input.
c) Measured at differential pair crossover.
d) Reference to half PCLK period.
e) Reference to full PCLK period.

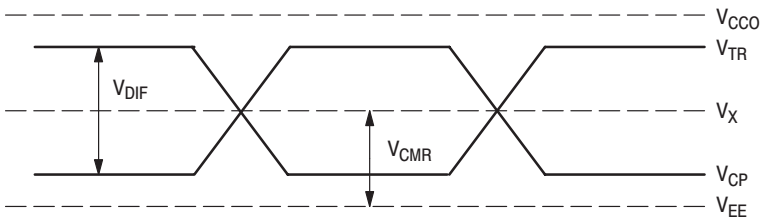


**Figure 3. HSTL Differential Input Levels**

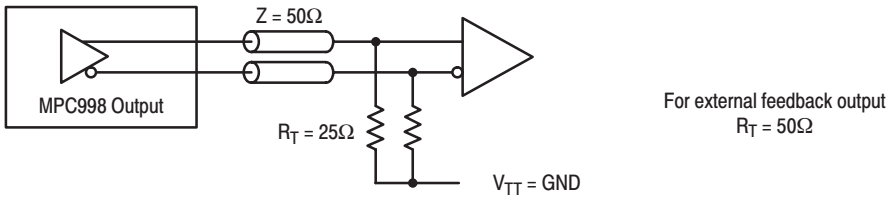


**Figure 4. Output Termination and AC Test Reference**

## APPLICATIONS INFORMATION

### Power Supply Filtering

The MPC998 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC998 provides separate power supplies for the output buffers ($V_{CCO}$) and the phase-locked loop ($V_{CCA}$) of the device.

The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the $V_{CCA}$ pin for the MPC998. Figure 5illustrates a typical power supply filter scheme. The MPC998 is most susceptible to noise with spectral content in the 10kHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the $V_{CCA}$ pin of the MPC998. From the data sheet the $I_{VCCA}$ current (the current sourced through the $V_{CCA}$ pin) is typically 15 mA (20 mA maximum), assuming that a minimum of 3.3V–5% must be maintained on the $V_{CCA}$ pin. Very little DC voltage drop can be tolerated when a 3.3V $V_{CC}$ supply is used. The resistor shown in Figure 5“Power Supply Filter” must have a resistance of 5-15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8-10 Ω resistor to avoid potential $V_{CC}$ drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

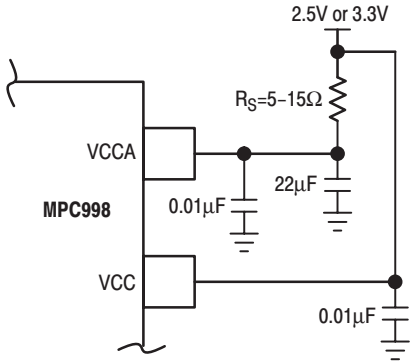


**Figure 5. Power Supply Filter**

Although the MPC998 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

*Product Preview*

# HSTL Low Voltage Differential Clock

The MPC9994 is a low voltage 3.3V, HSTL differential clock synthesizer. The clock is designed to support single and multiple processor systems requiring HSTL differential inputs. The MPC9994 supports two differential HSTL output pairs that may be operated from 340 MHz to 640 MHz.

**Features:**

- 2 clock outputs: (PCLK0 and PCLK1), each fully selectable
- Fully integrated PLL
- Output frequencies from 340 MHz to 640 MHz
- HSTL outputs
- HSTL and LVPECL reference clocks
- 32 lead LQFP packaging

The fully integrated Phase Locked Loop multiplies the HSTL_CLK input or the PECL_CLK input frequency to the desired processor clock frequency.

The PLL may be bypassed for test purposes such that the PCLK outputs are fed directly from the HSTL_CLK or PECL_CLK input.

All outputs are HSTL. The PCLK outputs are capable of driving 25Ω to ground with at least 600mV p-p signals. The EXTFB_OUT is capable of driving 50Ω ground with at least a 600 mV p-p signal. For on-chip power reduction, the outputs are powered from 1.8V external supply. For zero delay applications the buffer can operate with either external or internal feedback.

**MPC9994**

**HSTL LOW VOLTAGE DIFFERENTIAL CLOCK SYNTHESIZER FOR 340 – 640 MHZ**

3

**FA SUFFIX**
LQFP PACKAGE
CASE 873A–02

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**Rev 1**

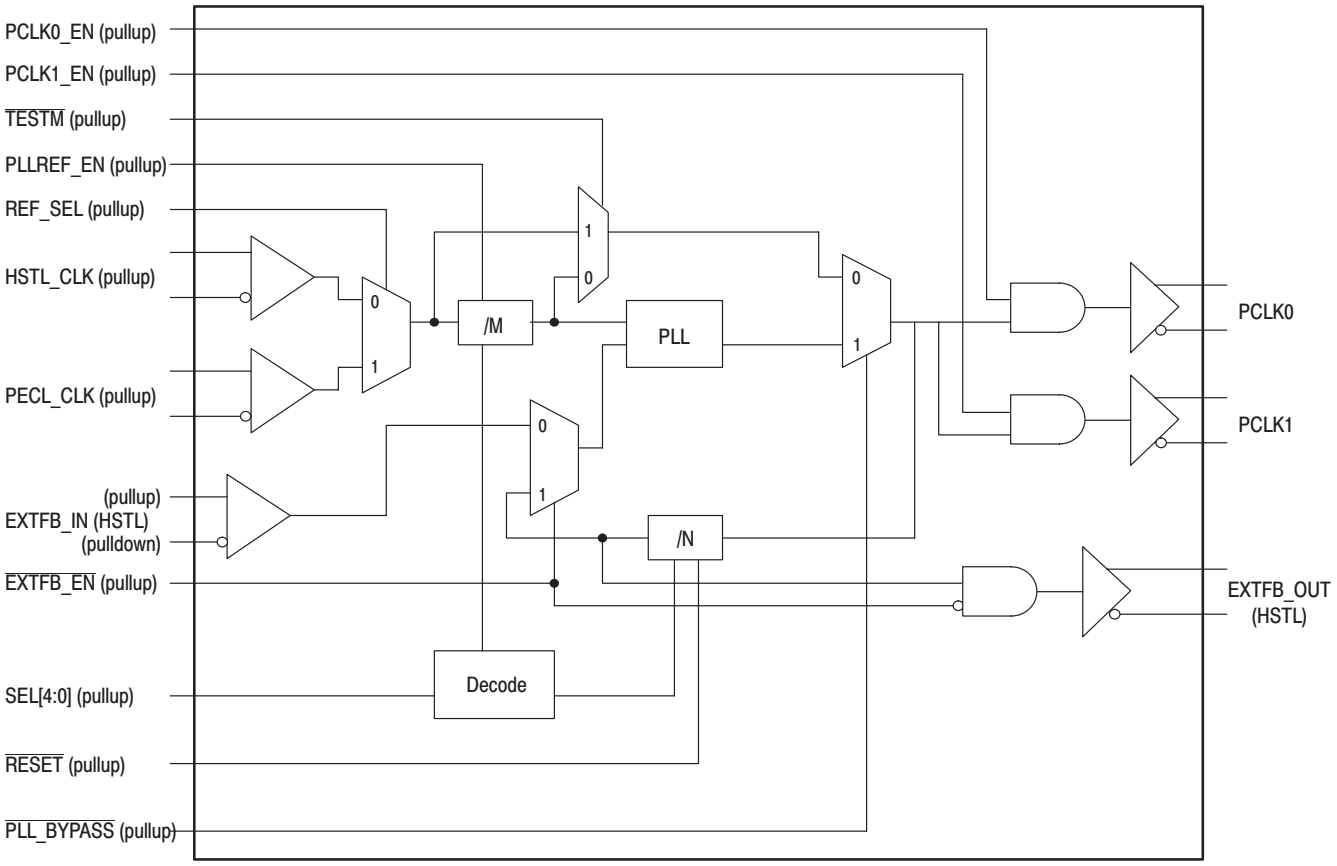



**Figure 1. MPC9994 Logic Diagram**

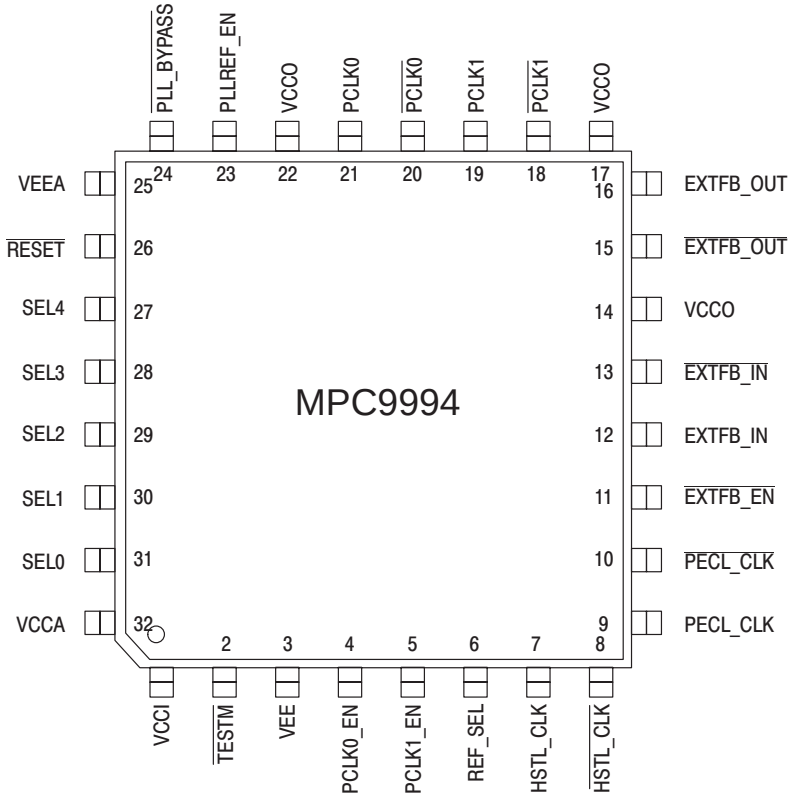



**Figure 2. 32 Lead Package Pinout (Top View)**

**PIN CONFIGURATION**

| Pin # | Pin | I/O Type | Type | Description |
|---|---|---|---|---|
| 1 | VCCI | Power | Power Supply | 3.3 V |
| 2 | $\overline{\text{TESTM}}$ | Input | LVCMOS | M divider test pins |
| 3 | VEE | Power (GND) | Ground | Digital GND |
| 4 | PCLK0_EN | Input | LVCMOS | PCLK0 enable |
| 5 | PCLK1_EN | Input | LVCMOS | PCLK1 enable |
| 6 | REF_SEL | Input | LVCMOS | Selects the PLL input reference clock |
| 7 | HSTL_CLK | Input | Differential HSTL | PLL reference clock input |
| 8 | $\overline{\text{HSTL\_CLK}}$ | Input | Differential HSTL | PLL reference clock input |
| 9 | PECL_CLK | Input | Differential LVPECL | PLL reference clock input |
| 10 | $\overline{\text{PECL\_CLK}}$ | Input | Differential LVPECL | PLL reference clock input |
| 11 | $\overline{\text{EXTFB\_EN}}$ | Input | LVCMOS | External feedback enable |
| 12 | EXTFB_IN | Input | Differential HSTL | External feedback input |
| 13 | $\overline{\text{EXTFB\_IN}}$ | Input | Differential HSTL | External feedback input |
| 14 | VCCO | Power | Power Supply | Output buffers power supply |
| 15 | $\overline{\text{EXTFB\_OUT}}$ | Output | Differential HSTL | External feedback output clock |
| 16 | EXTFB_OUT | Output | Differential HSTL | External feedback output clock |
| 17 | VCCO | Power | Power Supply | Ouput buffers power supply |
| 18 | $\overline{\text{PCLK1}}$ | Output | Differential HSTL | Output clock 1 |
| 19 | PCLK1 | Output | Differential HSTL | Output clock 1 |
| 20 | $\overline{\text{PCLK0}}$ | Output | Differential HSTL | Output clock 0 |
| 21 | PCLK0 | Output | Differential HSTL | Output clock 0 |
| 22 | VCCO | Power | Power Supply | Ouput buffers power supply |
| 23 | PLLREF_EN | Input | LVCMOS | PLL reference enable |
| 24 | $\overline{\text{PLL\_BYPASS}}$ | Input | LVCMOS | Input signal PLL bypass |
| 25 | VEEA | Power (GND) | Ground | Analog GND for PLL |
| 26 | $\overline{\text{RESET}}$ | Input | LVCMOS | PLL bypass reset (for test use) |
| 27 | SEL[4] | Input | LVCMOS | Selection of input and feedback frequency |
| 28 | SEL[3] | Input | LVCMOS | Selection of input and feedback frequency |
| 29 | SEL[2] | Input | LVCMOS | Selection of input and feedback frequency |
| 30 | SEL[1] | Input | LVCMOS | Selection of input and feedback frequency |
| 31 | SEL[0] | Input | LVCMOS | Selection of input and feedback frequency |
| 32 | VCCA | Power | Power Supply | 3.3 V filtered for PLL (PLL power supply) |

**FREQUENCY SELECTION TABLE**

| SEL | | | | | Input Divide | Feedback Divide |
|---|---|---|---|---|---|---|
| **4** | **3** | **2** | **1** | **0** | **M** | **N** |
| 0 | 0 | 0 | 0 | 0 | 5 | 16 |
| 0 | 0 | 0 | 0 | 1 | 5 | 17 |
| 0 | 0 | 0 | 1 | 0 | 5 | 18 |
| 0 | 0 | 0 | 1 | 1 | 5 | 19 |
| 0 | 0 | 1 | 0 | 0 | 5 | 20 |
| 0 | 0 | 1 | 0 | 1 | 5 | 21 |
| 0 | 0 | 1 | 1 | 0 | 5 | 22 |
| 0 | 0 | 1 | 1 | 1 | 5 | 23 |
| 0 | 1 | 0 | 0 | 0 | 5 | 24 |
| 0 | 1 | 0 | 0 | 1 | 5 | 25 |
| 0 | 1 | 0 | 1 | 0 | 5 | 26 |
| 0 | 1 | 0 | 1 | 1 | 5 | 27 |
| 0 | 1 | 1 | 0 | 0 | 5 | 28 |
| 0 | 1 | 1 | 0 | 1 | 5 | 29 |
| 0 | 1 | 1 | 1 | 0 | 5 | 30 |
| 0 | 1 | 1 | 1 | 1 | 5 | 31 |
| 1 | 0 | 0 | 0 | 0 | 5 | 32 |
| 1 | 0 | 0 | 0 | 1 | 5 | 33 |
| 1 | 0 | 0 | 1 | 0 | 5 | 34 |
| 1 | 0 | 0 | 1 | 1 | 5 | 35 |
| 1 | 0 | 1 | 0 | 0 | 5 | 36 |
| 1 | 0 | 1 | 0 | 1 | 5 | 37 |
| 1 | 0 | 1 | 1 | 0 | 5 | 38 |
| 1 | 0 | 1 | 1 | 1 | 5 | 39 |
| 1 | 1 | 0 | 0 | 0 | 5 | 40 |
| 1 | 1 | 0 | 0 | 1 | 5 | 41 |
| 1 | 1 | 0 | 1 | 0 | 5 | 42 |
| 1 | 1 | 0 | 1 | 1 | 5 | 43 |
| 1 | 1 | 1 | 0 | 0 | 5 | 44 |
| 1 | 1 | 1 | 0 | 1 | 5 | 45 |
| 1 | 1 | 1 | 1 | 0 | 5 | 46 |
| 1 | 1 | 1 | 1 | 1 | 5 | 47 |

**FUNCTION TABLE (CONTROLS)**

| Control Pin | 0 | 1 |
|---|---|---|
| REF_SEL | HSTL_CLK | PECL_CLK |
| $\overline{\text{TESTM}}$ | M divider test mode enabled | Reference fed to Bypass mux |
| PLLREF_EN | Disable the input to the PLL and reset the M divider | Enable the input to the PLL |
| $\overline{\text{PLL\_BYPASS}}$ | Outputs fed by input reference or M divider | Outputs fed by VCO |
| $\overline{\text{EXTFB\_EN}}$ | External feedback enabled | Internal feedback enabled |
| PCLK0_EN | PCLK0 = low, $\overline{\text{PCLK0}}$ = high | PCLK0 = high, $\overline{\text{PCLK0}}$ = low |
| PCLK1_EN | PCLK1 = low, $\overline{\text{PCLK1}}$ = high | PCLK1 = high, $\overline{\text{PCLK1}}$ = low |
| $\overline{\text{RESET}}$ | Resets feedback N divider | Feedback enabled |
| SEL[4:0] | See Selection Frequency Table | |

3

**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| VCC | Supply Voltage | -0.5 | 4.4 | V | |
| VCCO | Output Supply Voltage | -0.5 | 4.4 | V | |
| VIN | Input Voltage | -0.5 | VCC+0.3 | V | |
| IIN | Input Current | -1 | 1 | mA | |
| TS | Storage temperature | -50 | 150 | °C | |

NOTE: Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

**DC CHARACTERISTICS** (VCCA=VCCI = 3.3V ± 5%, VCCO = 1.7 to 2.1V, TA = 0 to 70°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| VIH | Input high voltage | 2.0 | | VCCI | V | LVCMOS |
| VIL | Input low voltage | 0.0 | | 0.8 | V | LVCMOS |
| VCMR | Input high voltage[a] | 1 | | VCCI - 0.3 | V | LVPECL |
| VPP | Input low voltage[a] | 0.5 | | 1 | V | LVPECL[b] |
| $V_{IN}$ (dc) | DC input signal voltage | -0.3 | | 1.45 | V | HSTL[c] |
| $V_{DIF}$(dc) | DC differential input voltage | 0.4 | | 1.75 | V | HSTL[d] |
| $V_{CM}$(dc) | DC common mode input voltage | 0.4 | | 1.0 | V | HSTL[e] |
| VOH | Output High Voltage | $V_X$ + 0.3 | $V_X$ + 0.5 | 1.4 | V | HSTL[f,a] |
| VOL | Output Low Voltage | 0.0 | $V_X$ - 0.5 | $V_X$ - 0.3 | V | HSTL[f] |
| ICCI | Core Supply Current | | | 140 | mA | |
| ICCA | PLL Supply Current | | 15 | 20 | mA | |
| ICCO | Output Supply Current | | 150 | | mA | Note [g] |
| $Theta_{JA}$ | Junction to ambient thermal resistance | | 53 | | °C/W | Note [h] |

a) DC levels will vary 1:1 with VCC.
b) VPP minimum and maximum required to maintain AC specifications. Actual device function will tolerate minimum VPP of 200mV.
c) $V_{IN}$ (dc) specifies the maximum allowable dc excursion of each differential input.
d) $V_{DIF}$ (dc) specifies the minimum input differential voltage ($V_{TR}$ - $V_{CP}$) required for switching, where $V_{TR}$ is the "true" input signal and $V_{CP}$ is the "complement" input signal.
e) $V_{CM}$(dc) specifies the maximum allowable range of input signal crosspoint voltage
f) $V_X$ is the differential output crosspoint voltage defined in the "AC CHARACTERISTICS" section
g) 2 PCLK into 25Ω and 1 EXTFB into 50Ω
h) Measured with 1.3M/s (250fpm) airflow

**AC CHARACTERISTICS** ($V_{CCA}$ = $V_{CCI}$ = 3.3V ± 5%, $V_{CCO}$ = 1.7 to 2.1V, $T_A$ = 0 to 70°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| fref | Input Frequency | | 100 - 125 | | MHz | |
| fMAX | Maximum Output Frequency | 340 | | 640 | MHz | Note [b] |
| tsk(o) | Skew Error (PCLK) | | | 35 | ps | Note [c] |
| $t_{jit(0)}$ | Phase jitter (IO jitter) | | | output period / 2 | | Note [c] |
| $t_{jit(cc)}$ | Cycle–to–cycle jitter (full period) | | | 5% | | Note [c, e] |
| $t_{jit(1/2per)}$ | Cycle–to–cycle jitter (half period) | | | 6% | Note[d] | Note [c, d] |
| $V_{DIFout}$ | Differential Output pk–pk swing | 0.6 | | | V | For all HSTL output pairs |
| Vx | Differential output crosspoint voltage | 0.68 | | 0.9 | V | For all HSTL output pairs |
| $t_{lock}$ | Maximum PLL lock time | | | 10 | ms | |

a) All PCLK outputs are terminated in 25Ω to ground, EXTFB_OUT is terminated in 50Ω to ground (applies to all measurements).
b) With PLL active but in bypass mode, fref Max is limited by input buffer; best performance is expected with PECL input.
c) Measured at differential pair crossover.
d) Reference to half PCLK period.
e) Reference to full PCLK period.

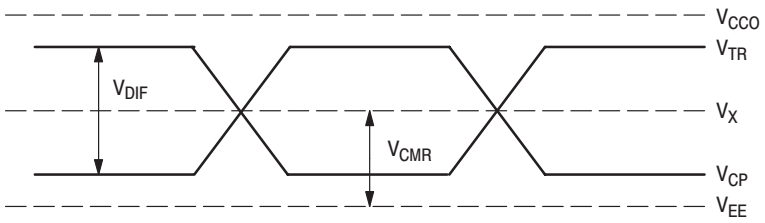



**Figure 3. HSTL Differential Input Levels**

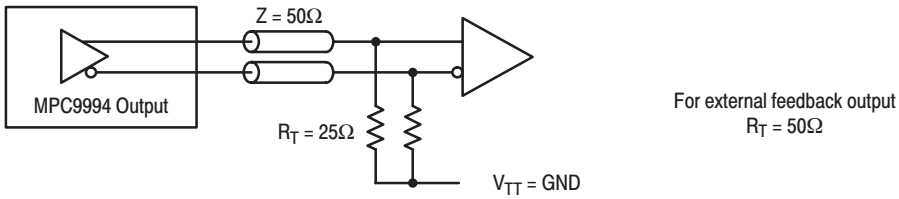



**Figure 4. Output Termination and AC Test Reference**

## APPLICATIONS INFORMATION

### Power Supply Filtering

The MPC9994 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC9994 provides separate power supplies for the output buffers ($V_{CCO}$) and the phase-locked loop ($V_{CCA}$) of the device.

The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the $V_{CCA}$ pin for the MPC9994. Figure 5illustrates a typical power supply filter scheme. The MPC9994 is most susceptible to noise with spectral content in the 10kHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the $V_{CCA}$ pin of the MPC9994. From the data sheet the $I_{VCCA}$ current (the current sourced through the $V_{CCA}$ pin) is typically 15 mA (20 mA maximum), assuming that a minimum of 3.3V–5% must be maintained on the $V_{CCA}$ pin. Very little DC voltage drop can be tolerated when a 3.3V $V_{CC}$ supply is used. The resistor shown in Figure 5“Power Supply Filter” must have a resistance of 5-15Ω to meet the voltage drop criteria.. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8-10 Ω resistor to avoid potential $V_{CC}$ drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

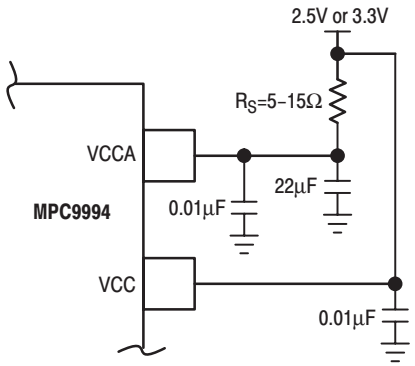



**Figure 5. Power Supply Filter**

Although the MPC9994 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

# Chapter Four
# Zero–Delay Buffer Data Sheets

**Zero–Delay Buffer Device Index**

# Low Voltage PLL Clock Driver

The MPC953 is a 3.3V compatible, PLL based clock driver device targeted for high performance clock tree designs. With output frequencies of up to 110MHz and output skews of 150ps the MPC953 is ideal for the most demanding clock tree designs. The devices employ a fully differential PLL design to minimize cycle–to–cycle and phase jitter.

- Fully Integrated PLL
- Output Frequency up to 110MHz in PLL Mode
- Outputs Disable in High Impedance
- LQFP Packaging
- 100ps Cycle–to–Cycle Jitter

The MPC953 has a differential LVPECL reference input along with an external feedback input. These features make the MPC953 ideal for use as a zero delay, low skew fanout buffer. The device performance has been tuned and optimized for zero delay performance. The MR/$\overline{OE}$ input pin will reset the internal counters and tristate the output buffers when driven “high”.

The MPC953 is fully 3.3V compatible and requires no external loop filter components. All control inputs accept LVCMOS or LVTTL compatible levels while the outputs provide LVCMOS levels with the ability to drive terminated 50Ω transmission lines. For series terminated 50Ω lines, each of the MPC953 outputs can drive two traces giving the device an effective fanout of 1:18. The device is packaged in a 7x7mm 32–lead LQFP package to provide the optimum combination of board density and performance.

**MPC953**

**See Upgrade Product – MPC9653**

**LOW VOLTAGE PLL CLOCK DRIVER**

**FA SUFFIX**
32–LEAD LQFP PACKAGE
CASE 873A–02



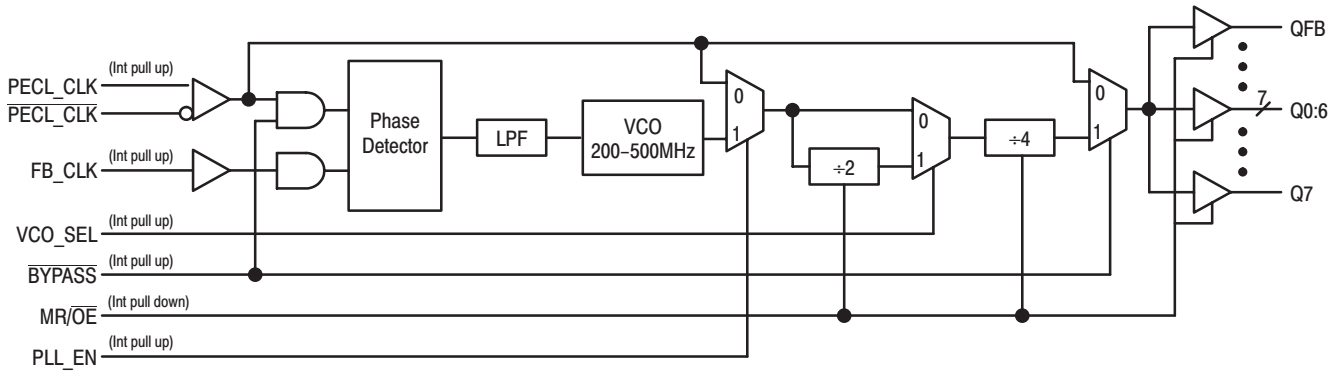



**Figure 1. Logic Diagram**

**Rev 3**

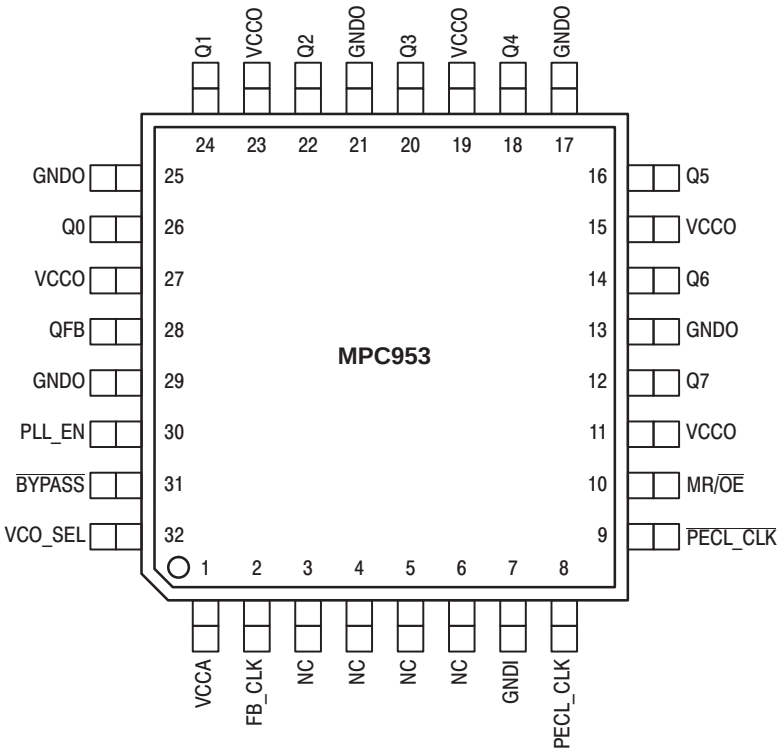



**Figure 2. 32–Lead Pinout** (Top View)

**FUNCTION TABLES**

| $\overline{\text{BYPASS}}$ | Function |
|---|---|
| 1 | PLL Enabled |
| 0 | PLL Bypass |

| MR/$\overline{\text{OE}}$ | Function |
|---|---|
| 1 | Outputs Disabled |
| 0 | Outputs Enabled |

| VCO_SEL | Function |
|---|---|
| 1 | ÷2 |
| 0 | ÷1 |

| PLL_EN | Function |
|---|---|
| 1 | Select VCO |
| 0 | Select PECL_CLK |

4

**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 4.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | Input Current | | ±20 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

**THERMAL CHARACTERISTICS**

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | LVCMOS Inputs | 2.0 | | 3.6 | V | |
| $V_{IL}$ | Input LOW Voltage | LVCMOS Inputs | | | 0.8 | V | |
| $V_{PP}$ | Peak–to–Peak Input Voltage | PECL_CLK | 300 | | 1000 | mV | |
| $V_{CMR}$ | Common Mode Range | PECL_CLK | $V_{CC}$–1.5 | | $V_{CC}$–0.6 | mV | Note 1. |
| $V_{OH}$ | Output HIGH Voltage | | $V_{CC}$–0.6 | | | V | $I_{OH}$ = –20mA, Note 2. |
| $V_{OL}$ | Output LOW Voltage | | | | 0.6 | V | $I_{OL}$ = 20mA, Note 2. |
| $I_{IN}$ | Input Current | | | | ±120 | µA | |
| $C_{IN}$ | Input Capacitance | | | | 4 | pF | |
| $C_{pd}$ | Power Dissipation Capacitance | | | 25 | | pF | Per Output |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | | 75 | mA | All VCC Pins |
| $I_{CCPLL}$ | Maximum PLL Supply Current | | | 15 | 20 | mA | VCCA Pin Only |

1. $V_{CMR}$ is the difference from the most positive side of the differential input signal. Normal operation is obtained when the “HIGH” input is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ specification.
2. The MPC953 outputs can drive series or parallel terminated (50Ω to $V_{CC}$/2) 50Ω transmission lines on the incident edge (see Applications Info section).

4

**PLL INPUT REFERENCE CHARACTERISTICS** ($T_A$ = 0 to 70°C)

| Symbol | Characteristic | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $f_{ref}$ | Reference Input Frequency | 25 | 110 | MHz | Note 3. |
| $f_{refDC}$ | Reference Input Duty Cycle | 25 | 75 | % | |

3. Maximum and minimum input reference is limited by the VCO lock range and the feedback divider.

**AC CHARACTERISTICS** ($T_A$ = 0°C to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.8 to 2.0V, Note 6. |
| $t_{pw}$ | Output Duty Cycle | | 45 | 50 | 55 | % | Note 6. |
| $t_{sk(O)}$ | Output–to–Output Skews | | | | 150 | ps | Note 6. |
| $f_{VCO}$ | PLL VCO Lock Range | | 200 | | 500 | MHz | Note 6. |
| $f_{max}$ | Maximum Output Frequency | PLL Mode<br>PLL Mode<br>Bypass Mode | 25<br>50 | | 62.5<br>110<br>200 | MHz<br>MHz<br>MHz | VCO_SEL = ’1’<br>VCO_SEL = ’0’<br>Note 6. |
| $t_{pd}$(lock) | Input to FB_CLK Delay (with PLL Locked) | | –75 | | 125 | ps | Note 4., 6. |
| $t_{pd}$(bypass) | Input to Q Delay | | 3 | | 7 | ns | PLL Bypassed<br>Note 5., 6. |
| | Part–to–Part Delay | | | | 1.5 | ns | |
| $t_{PLZ,HZ}$ | Output Disable Time | | | | 7 | ns | Note 6. |
| $t_{PZL}$ | Output Enable Time | | | | 6 | ns | Note 6. |
| $t_{jitter}$ | Cycle–to–Cycle Jitter | | | | 100 | ps | Note 6. |
| $t_{lock}$ | Maximum PLL Lock Time | | | | 10 | ms | |

4. $t_{pd}$(lock) is input reference frequency dependent. The $t_{pd}$ is specified at 50MHz ref, feedback ÷ 8. The $t_{pd}$ does not include jitter.
5. For a specified temperature and voltage, includes output skew.
6. Termination of 50Ω to $V_{CC}$/2.

**Power Supply Filtering**

The MPC953 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC953 provides separate power supplies for the output buffers (VCCO) and the phase–locked loop (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC953.

Figure 3 illustrates a typical power supply filter scheme. The MPC953 is most susceptible to noise with spectral content in the 100KHz to 10MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the VCCA pin of the MPC953. From the data sheet the $I_{VCCA}$ current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V $V_{CC}$ supply is used. The resistor shown in Figure 3 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8–10Ω resistor to avoid potential $V_{CC}$ drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

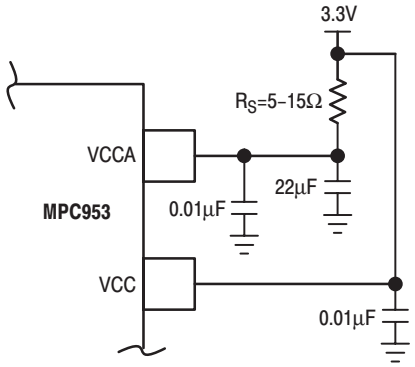



**Figure 3. Power Supply Filter**

Although the MPC953 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Driving Transmission Lines**

The MPC953 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC953 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC953 clock driver is effectively doubled due to its capability to drive multiple lines.

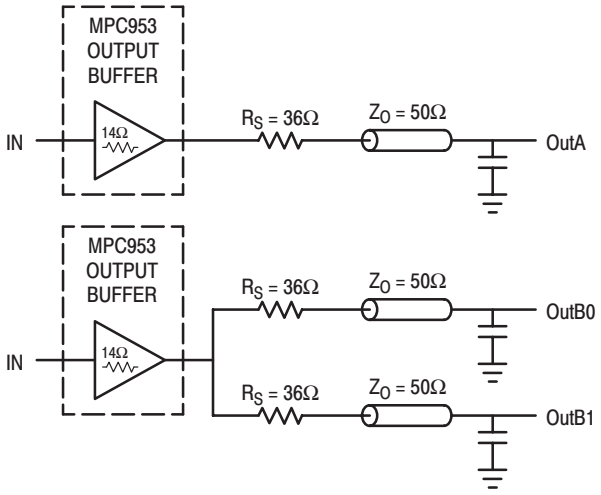



**Figure 4. Single versus Dual Transmission Lines**

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC953 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC953. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

VL = VS ( Zo / (Rs + Ro +Zo))

Zo = 50Ω || 50Ω
Rs = 36Ω || 36Ω
Ro = 14Ω

VL = 3.0 (25 / (18 + 14 + 25) = 3.0 (25 / 57)
= 1.31V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.62V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

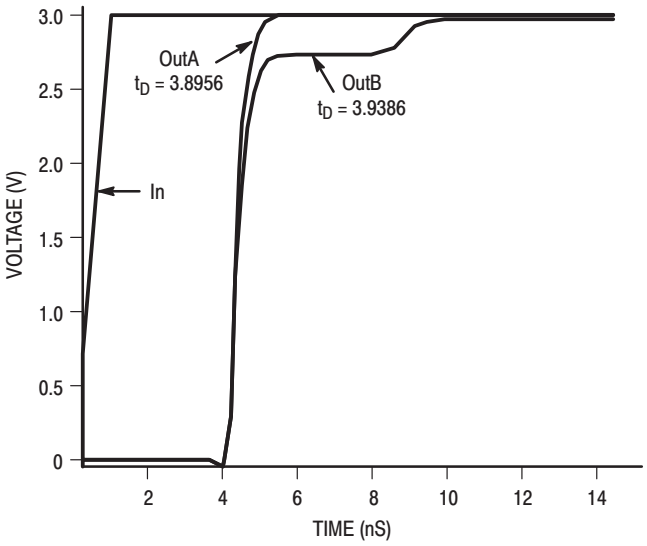
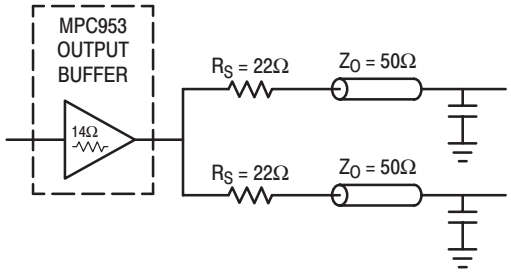



**Figure 5. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




14Ω + 22Ω || 22Ω = 50Ω || 50Ω
25Ω = 25Ω

**Figure 6. Optimized Dual Line Termination**

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

# Low Voltage PLL Clock Driver

The MPC954 is a 3.3V compatible, PLL based zero delay buffer targeted for high performance clock tree designs. With 11 outputs at frequencies of up to 100MHz and output skews of 200ps the MPC954 is ideal for the most demanding clock tree designs. The devices employ a fully differential PLL design to minimize cycle–to–cycle and phase jitter.

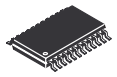
- Fully Integrated PLL
- Output Frequency up to 100MHz
- Outputs Disable in High Impedance
- TSSOP Packaging
- 50ps Cycle–to–Cycle Jitter Typical

The analog $V_{CC}$ pin of the device also serves as a PLL bypass select pin. When driven low the $V_{CCA}$ pin will route the REF_CLK input around the PLL directly to the outputs. The OE input is a logic enable for all of the outputs except QFB. A low on the OE pin forces Q0–Q9 to a logic low state.

The MPC954 is fully 3.3V compatible and requires no external loop filter components. All inputs accept LVCMOS or LVTTL compatible levels while the outputs provide LVCMOS levels with the ability to drive terminated 50Ω transmission lines. The output impedance of the MPC954 is ≈ 10Ω, therefore for series terminated 50Ω lines, each of the MPC954 outputs can drive two traces giving the device an effective fanout of 1:22. The device is packaged in a 24–lead TSSOP package to provide the optimum combination of board density and performance.

**MPC954**

**LOW VOLTAGE PLL ZERO DELAY BUFFER**



**DT SUFFIX**
24–LEAD TSSOP PACKAGE
CASE 948H–01

4



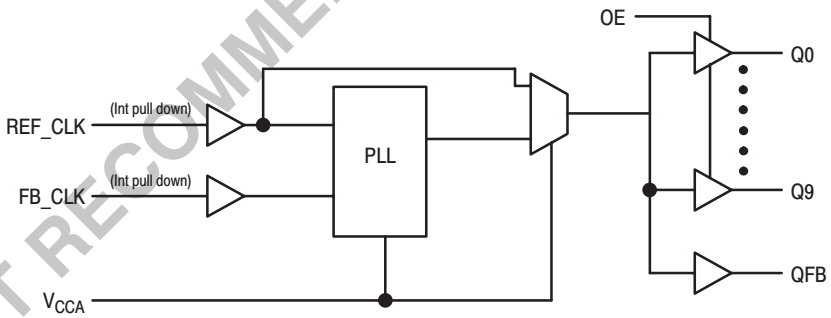



**Figure 1. Block Diagram**

**Rev 1**

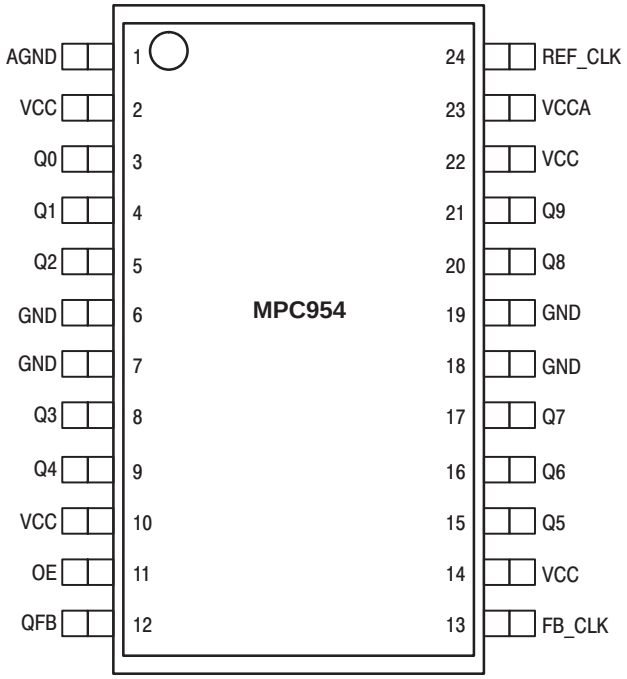



**Figure 2. 24–Lead Pinout** (Top View)

**FUNCTION TABLES**

| $V_{CCA}$ | Function |
|---|---|
| 1 | PLL Enabled |
| 0 | PLL Bypass |

| OE | Function |
|---|---|
| 1 | Q0 – Q9 Enabled |
| 0 | Q0 – Q9 Low |



**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 4.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | Input Current | | ±20 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

**THERMAL CHARACTERISTICS**

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage LVCMOS Inputs | 2.0 | | 3.6 | V | |
| $V_{IL}$ | Input LOW Voltage LVCMOS Inputs | | | 0.8 | V | |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | $I_{OH}$ = –20mA, Note 1. |
| $V_{OL}$ | Output LOW Voltage | | | 0.5 | V | $I_{OL}$ = 20mA, Note 1. |
| $I_{IN}$ | Input Current | | | ±120 | µA | Note 2. |
| $C_{IN}$ | Input Capacitance | | | 4 | pF | |
| $C_{pd}$ | Power Dissipation Capacitance | | 25 | | pF | Per Output |
| $I_{CC}$ | Maximum Quiescent Supply Current | | 40 | | mA | All VCC Pins |
| $I_{CCPLL}$ | Maximum PLL Supply Current | | 15 | | mA | VCCA Pin Only |

1. The MPC954 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}$/2) transmission lines on the incident edge (see Applications Info section).
2. Inputs have pullup resistor which affect input current.

**PLL INPUT REFERENCE CHARACTERISTICS** ($T_A$ = 0 to 70°C)

| Symbol | Characteristic | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $f_{ref}$ | Reference Input Frequency | 50 | 100 | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | 25 | 75 | % | |

**AC CHARACTERISTICS** ($T_A$ = 0°C to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.3 | | 1.5 | ns | 0.8 to 2.0V, (Note 1.) |
| $t_{pw}$ | Output Duty Cycle | 40 | 50 | 60 | % | (Note 1.) |
| $t_{sk(O)}$ | Output–to–Output Skews | | | 300 | ps | (Note 1.) |
| $f_{max}$ | Maximum Output Frequency PLL Mode | 50 | | 100 | MHz | (Note 1.) |
| $t_{pd}$(lock) | REF_CLK to FB_CLK Delay (with PLL Locked) | –300 | | 0 | ps | (Note 1.) |
| $t_{PLZ,HZ}$ | Output Disable Time | | 7 | | ns | (Note 1.) |
| $t_{PZL}$ | Output Enable Time | | 7 | | ns | (Note 1.) |
| $t_{jitter}$ | Cycle–to–Cycle Jitter (Peak–to–Peak) | | 50 | | ps | (Note 1.) |
| $t_{lock}$ | Maximum PLL Lock Time | | | 10 | ms | |

1. Termination of 50Ω to $V_{CC}$/2.

**Power Supply Filtering**

The MPC954 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC954 provides separate power supplies for the output buffers (VCCO) and the phase–locked loop (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC954.

Figure 3 illustrates a typical power supply filter scheme. The MPC954 is most susceptible to noise with spectral content in the 1KHz to 10MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the VCCA pin of the MPC954. From the data sheet the $I_{VCCA}$ current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V $V_{CC}$ supply is used. The resistor shown in Figure 3 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8–10Ω resistor to avoid potential $V_{CC}$ drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

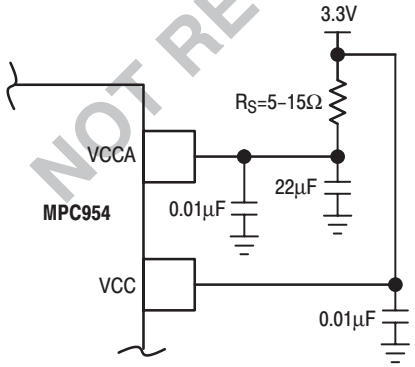



**Figure 3. Power Supply Filter**

Although the MPC954 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Driving Transmission Lines**

The MPC954 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC954 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC954 clock driver is effectively doubled due to its capability to drive multiple lines.

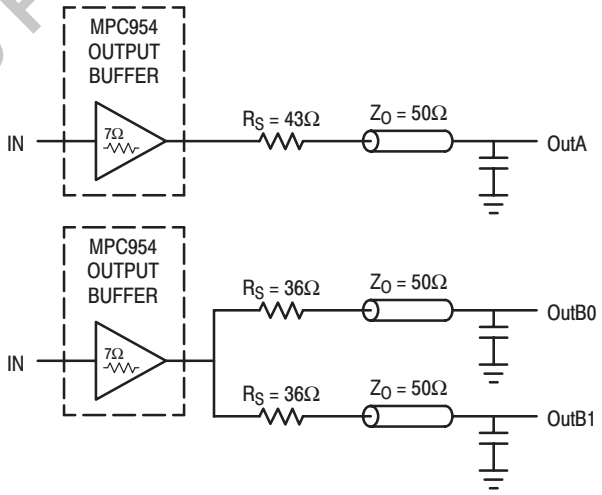



**Figure 4. Single versus Dual Transmission Lines**

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC954 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC954. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

VL = VS ( Zo / (Rs + Ro +Zo))

Zo = 50Ω || 50Ω
Rs = 43Ω || 43Ω
Ro = 7Ω

VL = 3.0 (25 / (21.5 + 7 + 25) = 3.0 (25 / 53.5)
= 1.40V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.80V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

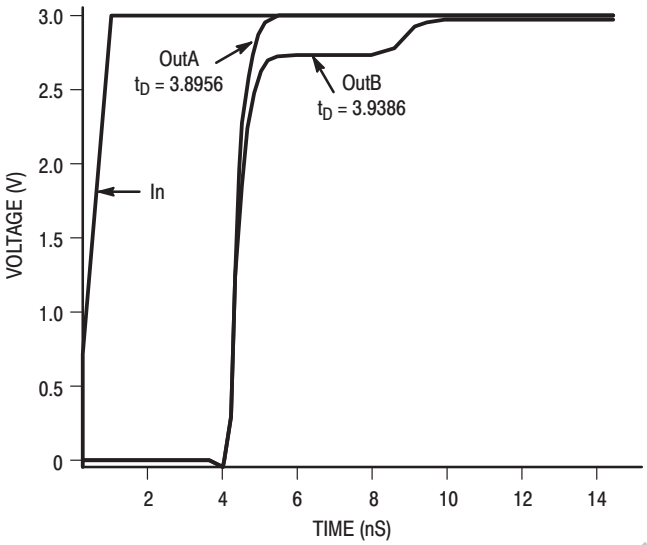
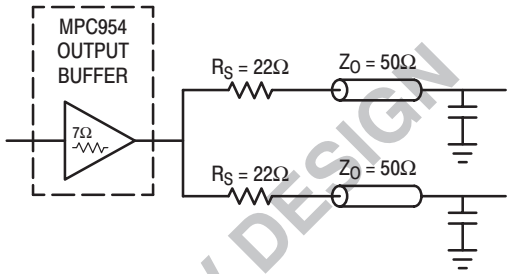



**Figure 5. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




14Ω + 22Ω || 22Ω = 50Ω || 50Ω
25Ω = 25Ω

**Figure 6. Optimized Dual Line Termination**

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.



4

# Low Voltage PLL Clock Driver

**MPC958**

**See Upgrade Product – MPC9658**

**LOW VOLTAGE PLL CLOCK DRIVER**

**FA SUFFIX**
32–LEAD LQFP PACKAGE
CASE 873A–02

The MPC958 is a 3.3V compatible, PLL based clock driver device targeted for high performance clock tree designs. With output frequencies of up to 200MHz and output skews of 200ps the MPC958 is ideal for the most demanding clock tree designs. The devices employ a fully differential PLL design to minimize cycle–to–cycle and phase jitter.

- Fully Integrated PLL
- Output Frequency up to 200MHz
- Outputs Disable in High Impedance
- LQFP Packaging
- 100ps Cycle–to–Cycle Jitter

The MPC958 has a differential LVPECL reference input along with an external feedback input. These features make the MPC958 ideal for use as a zero delay, low skew fanout buffer. The device performance has been tuned and optimized for zero delay performance. The MR/$\overline{OE}$ input pin will tristate the output buffers when driven “high”.

The MPC958 is fully 3.3V compatible and requires no external loop filter components. All control inputs accept LVCMOS or LVTTL compatible levels while the outputs provide LVCMOS levels with the ability to drive terminated 50Ω transmission lines. For series terminated 50Ω lines, each of the MPC958 outputs can drive two traces giving the device an effective fanout of 1:22. The device is packaged in a 7x7mm 32–lead LQFP package to provide the optimum combination of board density and performance.

4

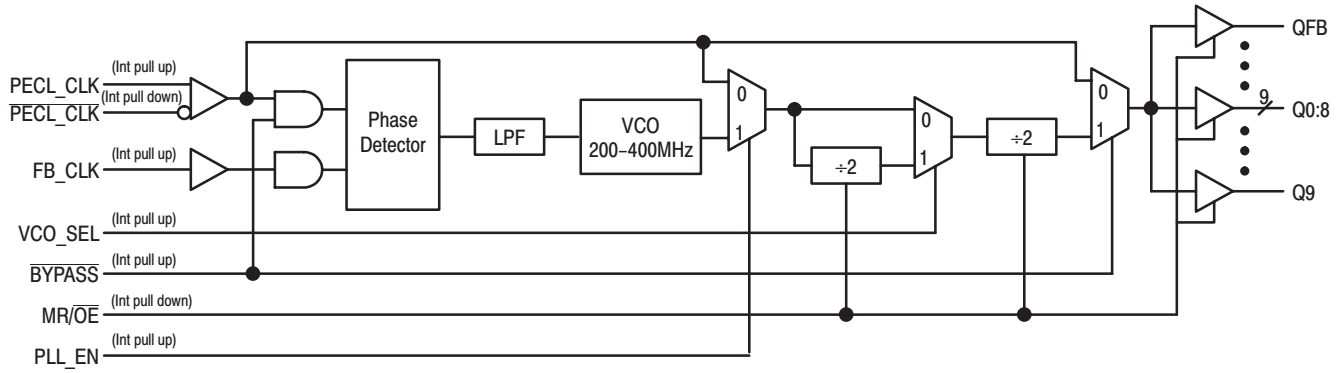



**Figure 1. Logic Diagram**

**Rev 1**

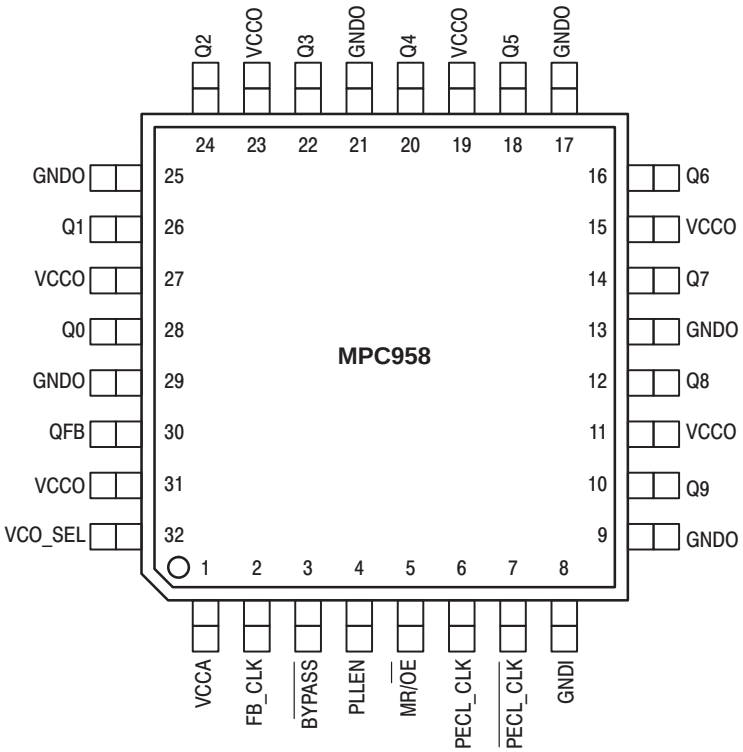



**Figure 2. 32–Lead Pinout** (Top View)

**FUNCTION TABLES**

| $\overline{\text{BYPASS}}$ | Function |
|---|---|
| 1 | PLL Enabled |
| 0 | PLL Bypass |

| MR/$\overline{\text{OE}}$ | Function |
|---|---|
| 1 | Outputs Disabled |
| 0 | Outputs Enabled |

| VCO_SEL | Function |
|---|---|
| 1 | ÷2 |
| 0 | ÷1 |

| PLL_EN | Function |
|---|---|
| 1 | Select VCO |
| 0 | Select PECL_CLK |

4

**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 4.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | Input Current | | ±20 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

**THERMAL CHARACTERISTICS**

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | LVCMOS Inputs | 2.0 | | 3.6 | V | |
| $V_{IL}$ | Input LOW Voltage | LVCMOS Inputs | | | 0.8 | V | |
| $V_{PP}$ | Peak–to–Peak Input Voltage | PECL_CLK | 300 | | 1000 | mV | |
| $V_{CMR}$ | Common Mode Range | PECL_CLK | 1.0 | | 3.0 | V | Note 1. |
| $V_{OH}$ | Output HIGH Voltage | | 2.4 | | | V | $I_{OH}$ = –20mA, Note 2. |
| $V_{OL}$ | Output LOW Voltage | | | | 0.5 | V | $I_{OL}$ = 20mA, Note 2. |
| $I_{IN}$ | Input Current | | | | ±120 | µA | |
| $C_{IN}$ | Input Capacitance | | | | 4 | pF | |
| $C_{pd}$ | Power Dissipation Capacitance | | | 25 | | pF | Per Output |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | | 75 | mA | All VCC Pins |
| $I_{CCPLL}$ | Maximum PLL Supply Current | | | 15 | 20 | mA | VCCA Pin Only |

1. $V_{CMR}$ is the center of the differential input signal. Normal operation is obtained when the input crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ specification.
2. The MPC958 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}$/2) transmission lines on the incident edge (see Applications Info section).

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**PLL INPUT REFERENCE CHARACTERISTICS** ($T_A$ = 0 to 70°C)

| Symbol | Characteristic | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $f_{ref}$ | Reference Input Frequency | Note 1. | Note 1. | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | 25 | 75 | % | |

3. Maximum and minimum input reference is limited by the VCO lock range and the feedback divider.

**AC CHARACTERISTICS** ($T_A$ = 0°C to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.10 | | 1.0 | ns | 0.8 to 2.0V<br>Note 1. |
| $t_{pw}$ | Output Duty Cycle | PLL Mode | tcycle/2 – 400 | | tcycle/2 + 400 | ps | Note 1. |
| $t_{sk(O)}$ | Output–to–Output Skews (Relative to QFB) | | | | 200 | ps | Note 1. |
| $f_{VCO}$ | PLL VCO Lock Range | | 200 | | 400 | MHz | |
| $f_{max}$ | Maximum Output Frequency<br>(Note 1.) | PLL Mode<br>PLL Mode<br>Bypass Mode | 50<br>100 | | 100<br>200<br>200 | MHz | VCO_SEL = ‘1’<br>VCO_SEL = ‘0’ |
| $t_{pd}$(lock) | Input to Ext_FB Delay (with PLL Locked @ 100MHz) | | –70 | | 130 | ps | Note 1. |
| $t_{pd}$(bypass) | Input to Q Delay | | 3.0 | | 7.0 | ns | PLL Bypassed |
| $t_{PLZ,HZ}$ | Output Disable Time | | | | 7 | ns | |
| $t_{PZL}$ | Output Enable Time | | | | 6 | ns | |
| $t_{jitter}$ | Cycle–to–Cycle Jitter (Peak–to–Peak) | | | | 100 | ps | Note 1. |
| $t_{lock}$ | Maximum PLL Lock Time | | | | 10 | ms | |

4. Termination of 50Ω to $V_{CC}$/2.

**Power Supply Filtering**

The MPC958 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC958 provides a separate power supply for the phase–locked loop (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC958.

Figure 3 illustrates a typical power supply filter scheme. The MPC958 is most susceptible to noise with spectral content in the 1kHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the VCCA pin of the MPC958. From the data sheet the $I_{VCCA}$ current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V $V_{CC}$ supply is used. The resistor shown in Figure 3 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20kHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8–10Ω resistor to avoid potential $V_{CC}$ drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

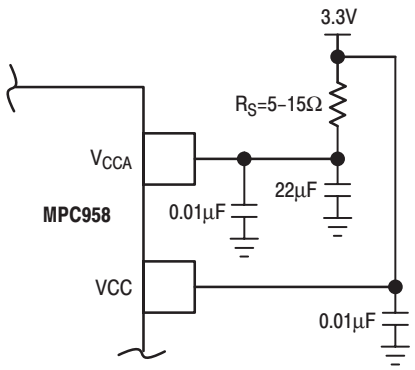



**Figure 3. Power Supply Filter**

Although the MPC958 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Driving Transmission Lines**

The MPC958 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC958 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC958 clock driver is effectively doubled due to its capability to drive multiple lines.

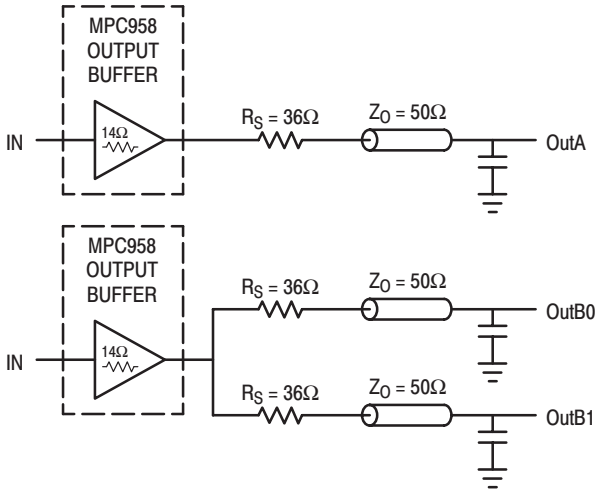



**Figure 4. Single versus Dual Transmission Lines**

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC958 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC958. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

VL = VS ( Zo / (Rs + Ro +Zo))

Zo = 50Ω || 50Ω
Rs = 36Ω || 36Ω
Ro = 14Ω

VL = 3.0 (25 / (18 + 14 + 25) = 3.0 (25 / 57)
= 1.31V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.62V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

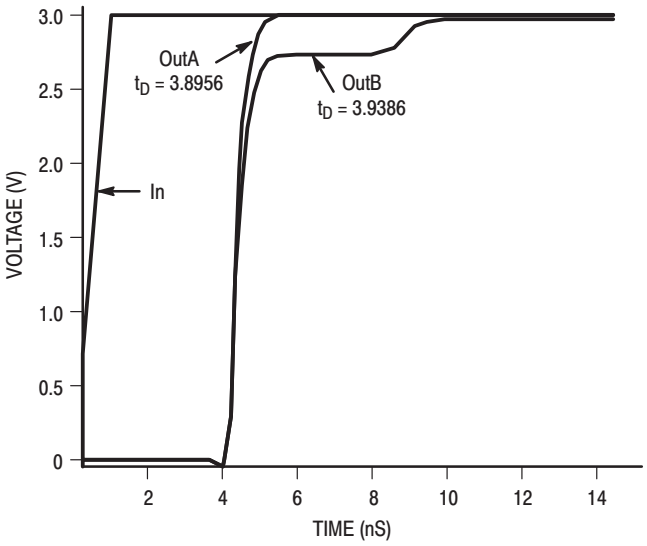
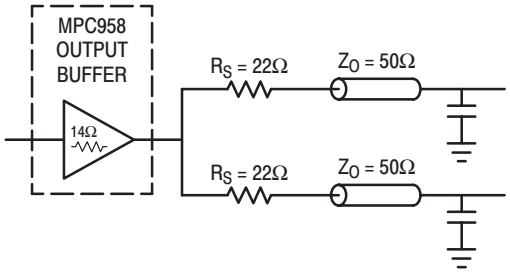



**Figure 5. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




14Ω + 22Ω || 22Ω = 50Ω || 50Ω
25Ω = 25Ω

**Figure 6. Optimized Dual Line Termination**

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

*Product Preview*

# 1:10 LVCMOS Zero Delay Clock Buffer

**MPC9608**

**LOW VOLTAGE 3.3V/2.5V LVCMOS 1:10 ZERO–DELAY CLOCK BUFFER**

**FA SUFFIX**
32–LEAD LQFP PACKAGE
CASE 873A

4

The MPC9608 is a 2.5V and 3.3V compatible, 1:10 PLL based zero-delay buffer. With a very wide frequency range and low output skews the MPC9608 is targeted for high performance and mid-range clock tree designs.

**Features**

- 1:10 outputs LVCMOS zero-delay buffer
- Single 3.3V or 2.5V supply
- 150 ps maximum output skew[1]
- ±100 ps static phase offset (SPO)[1]
- Supports a clock I/O frequency range of 12.5 to 200 MHz
- Selectable divide-by-two for one output bank
- Synchronous output enable control (CLK_STOP)
- Output tristate control (output high impedance)
- PLL bypass mode for low frequency system test purpose
- Supports networking, telecommunications and computer applications
- Supports a variety of microprocessors and controllers
- Compatible to PowerQuicc I and II
- Ambient Temperature Range –40°C to +85°C

**Functional Description**

The MPC9608 uses an internal PLL and an external feedback path to lock its low-skew clock output phase to the reference clock phase, providing virtually zero propagation delay. This enables nested clock designs with near-zero insertion delay. Designs using the MPC9608 as PLL fanout buffer will show significantly lower clock skew than clock distributions developed from traditional fanout buffers. The device offers one reference clock input and two banks of 5 outputs for clock fanout. The input frequency and phase is reproduced by the PLL and provided at the outputs. A selectable frequency divider sets the bank B outputs to generate either an identical copy of the bank A clocks or one half of the bank A clock frequency. Both output banks remain synchronized to the input reference for both bank B configurations.

Outputs are only disabled or enabled when the outputs are already in logic low state (CLK_STOP). For system test and diagnosis, the MPC9608 outputs can also be set to high-impedance state by connecting $\overline{OE}$ to logic high level. Additionally, the device provides a PLL bypass mode for low frequency test purpose. In PLL bypass mode, the minimum frequency and static phase offset specification do not apply.

CLK_STOP and $\overline{OE}$ do not affect the PLL feedback output (QFB) and down stream clocks can be disabled without the internal PLL losing lock.

The MPC9608 is fully 2.5V or 3.3V compatible and requires no external components for the internal PLL. All inputs accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines on the incident edge. For series terminated transmission lines, each of the MPC9608 outputs can drive one or two traces giving the devices an effective fanout of 1:20. The device is packaged in a 7x7 $mm^2$ 32-lead LQFP package.

1. Final AC specifications pending final device characterization.



**Rev 0**

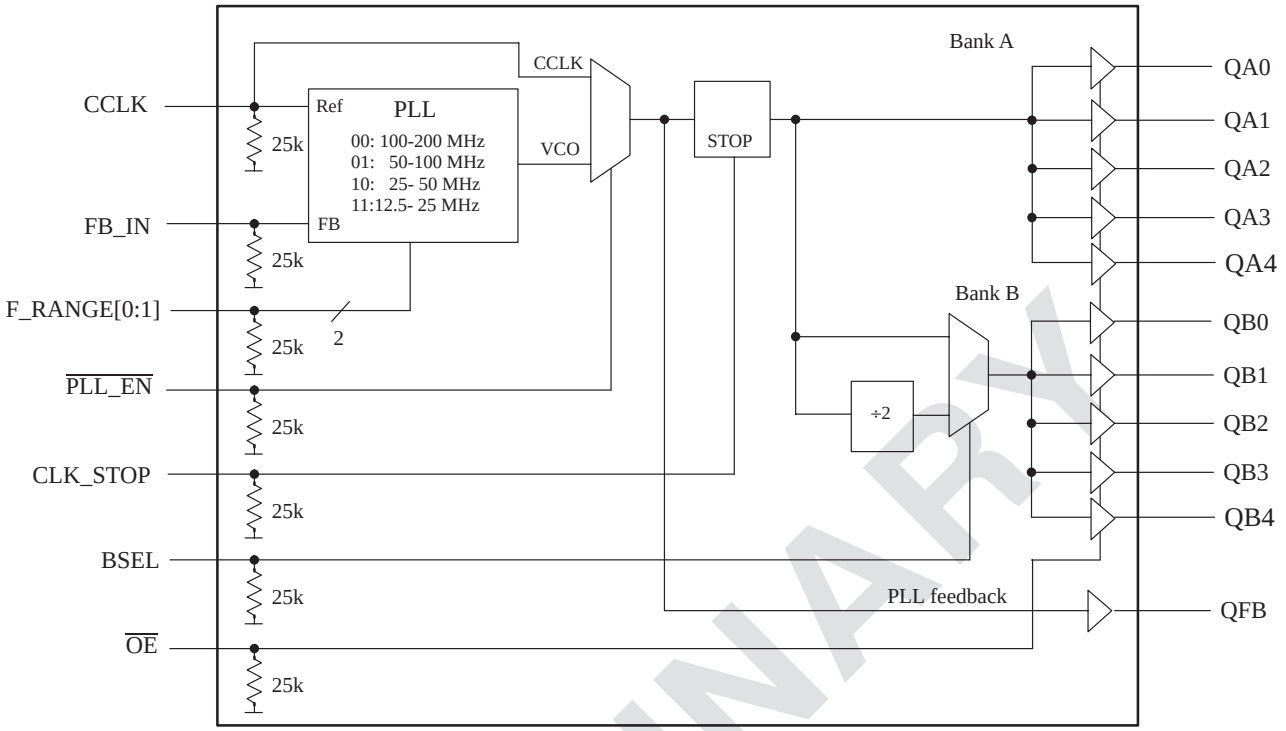



**Figure 1. MPC9608 Logic Diagram**

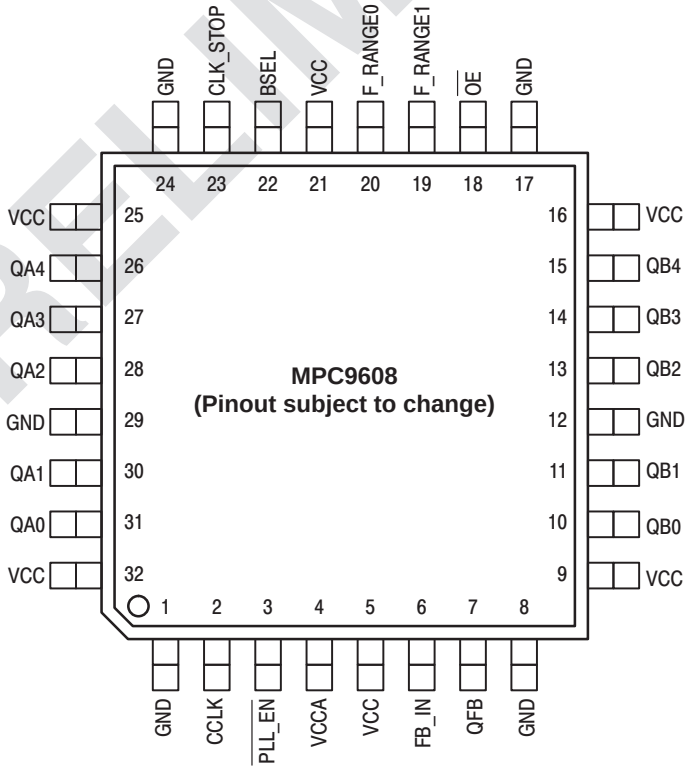



**Figure 2. MPC9608 32–Lead Package Pinout** (Top View)

**TABLE 1: PIN CONFIGURATION**

| Pin | I/O | Type | Function |
|---|---|---|---|
| CCLK | Input | LVCMOS | PLL reference clock signal |
| FB_IN | Input | LVCMOS | PLL feedback signal input, connect to a QFB output |
| F_RANGE[0:1] | Input | LVCMOS | PLL frequency range select |
| BSEL | Input | LVCMOS | Frequency divider select for bank B outputs |
| $\overline{\text{PLL\_EN}}$ | Input | LVCMOS | PLL enable/disable |
| $\overline{\text{OE}}$ | Input | LVCMOS | Output enable/disable (high-impedance tristate) |
| CLK_STOP | Input | LVCMOS | Synchronous clock enable/stop |
| QA0-4, QB0-4 | Output | LVCMOS | Clock outputs |
| QFB | Output | LVCMOS | PLL feedback signal output. Connect to FB_IN |
| GND | Supply | Ground | Negative power supply |
| VCCA | Supply | VCC | PLL positive power supply (analog power supply). The MPC9608 requires an external RC filter for the analog power supply pin $V_{CCA}$. Please see applications section for details. |
| VCC | Supply | VCC | Positive power supply for I/O and core |

**TABLE 2: FUNCTION TABLE**

| Control | Default | 0 | 1 |
|---|---|---|---|
| F_RANGE[0:1] | 00 | PLL frequency range. See Table 3 “Clock frequency configuration for QFB connected to FB_IN” | |
| BSEL | 0 | $f_{QB0-4} = f_{QA0-4}$ | $f_{QB0-4} = f_{QA0-4} \div 2$ |
| CLK_STOP | 0 | Outputs enabled | Outputs synchronously stopped in logic low state |
| $\overline{\text{OE}}$ | 0 | Outputs enabled (active) | Outputs disabled (high-impedance state), independent on CLK_STOP. Applying $\overline{\text{OE}}$=1 and $\overline{\text{PLL\_EN}}$=1 resets the device. The PLL feedback output QFB is not affected by $\overline{\text{OE}}$. |
| $\overline{\text{PLL\_EN}}$ | 0 | Normal operation mode with PLL enabled. | Test mode with PLL disabled. CCLK is substituted for the internal VCO output. MPC9608 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable. Applying $\overline{\text{OE}}$=1 and $\overline{\text{PLL\_EN}}$=1 resets the device. |

**TABLE 3: Clock Frequency Configuration for QFB connected to FB_IN**

| F_RANGE[0] | F_RANGE[1] | BSEL | $f_{REF}$ (CCLK) range [MHz] | QA0-QA4 | | QB0-B4 | | QFB |
|---|---|---|---|---|---|---|---|---|
| | | | | Ratio | $f_{QA0-4}$ [MHz] | Ratio | $f_{QB0-4}$ [MHz] | |
| 0 | 0 | 0 | 100.0—200.0 | $f_{REF}$ | 100.0—200.0 | $f_{REF}$ | 100.0—200.0 | $f_{REF}$ |
| 0 | 0 | 1 | | | | $f_{REF} \div 2$ | 50.0—25.0 | $f_{REF}$ |
| 0 | 1 | 0 | 50.0—100.0 | $f_{REF}$ | 50.0—100.0 | $f_{REF}$ | 50.0—100.0 | $f_{REF}$ |
| 0 | 1 | 1 | | | | $f_{REF} \div 2$ | 25.0—50.0 | $f_{REF}$ |
| 1 | 0 | 0 | 25.0—50.0 | $f_{REF}$ | 25.0—50.0 | $f_{REF}$ | 25.0—50.0 | $f_{REF}$ |
| 1 | 0 | 1 | | | | $f_{REF} \div 2$ | 12.5—25.0 | $f_{REF}$ |
| 1 | 1 | 0 | 12.5—25.0 | $f_{REF}$ | 12.5—25 | $f_{REF}$ | 12.5—25.0 | $f_{REF}$ |
| 1 | 1 | 1 | | | | $f_{REF} \div 2$ | 50.0—100 | $f_{REF}$ |



4

**TABLE 4: GENERAL SPECIFICATIONS**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output termination voltage | | $V_{CC} \div 2$ | | V | |
| MM | ESD protection (Machine model) | 200 | | | V | |
| HBM | ESD protection (Human body model) | 2000 | | | V | |
| LU | Latch-up immunity | 200 | | | mA | |
| $C_{PD}$ | Power dissipation capacitance | | 10 | | pF | Per output |
| $C_{IN}$ | Input capacitance | | 4.0 | | pF | Inputs |

**TABLE 5: ABSOLUTE MAXIMUM RATINGS[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -65 | 125 | °C | |

a. Absolute maximum continuos ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

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**TABLE 6: DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40° to 85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | | | 0.8 | V | LVCMOS |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$=-24 mA[a] |
| $V_{OL}$ | Output Low Voltage | | | 0.55<br>0.30 | V<br>V | $I_{OL}$= 24 mA<br>$I_{OL}$= 12 mA |
| $Z_{OUT}$ | Output Impedance | | 14 - 17 | | Ω | |
| $I_{IN}$ | Input Current[b] | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CCA}$ | Maximum PLL Supply Current | | 3.0 | 5.0 | mA | $V_{CCA}$ Pin |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a. The MPC9608 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.
b. Inputs have pull–down resistors affecting the input current.

**TABLE 7: AC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40° to 85°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input reference frequency in PLL mode[c] | F_RANGE = 00 | 100 | | 200 | MHz | |
| | | F_RANGE = 01 | 50 | | 100 | MHz | |
| | | F_RANGE = 10 | 25 | | 50 | MHz | |
| | | F_RANGE = 11 | 12.5 | | 25 | MHz | |
| | Input reference frequency in PLL bypass mode[d] | | 0 | | TBD | MHz | |
| $f_{MAX}$ | Output Frequency[e] | F_RANGE = 00 | 100 | | 200 | MHz | BSEL = 0 |
| | | F_RANGE = 01 | 50 | | 100 | MHz | BSEL = 0 |
| | | F_RANGE = 10 | 25 | | 50 | MHz | BSEL = 0 |
| | | F_RANGE = 11 | 12.5 | | 25 | MHz | BSEL = 0 |
| $f_{refDC}$ | Reference Input Duty Cycle | | 25 | | 75 | % | |
| tr, tf | CCLK Input Rise/Fall Time | | | | 1.0 | ns | 0.8 to 2.0V |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) CCLK to FB_IN<br>F_RANGE = 00<br>F_RANGE = 01<br>F_RANGE = 10<br>F_RANGE = 11 | | | ±100 | | ps | PLL locked |
| $t_{sk(o)}$ | Output-to-Output Skew[f] | | | | 150 | ps | |
| DC | Output Duty Cycle | | 45 | 50 | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.55 to 2.4V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 10 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 10 | ns | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ)[g] | | 15 | | ps | BSEL = 0 |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | 10 | | ps | BSEL = 0 |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1 σ) | | TBD | | ps | BSEL = 0 |
| $t_S$ | Setup time, CLK_STOP to CCLK | | 100 | | | ps | |
| $t_H$ | Hold time, CCLK to CLK_STOP | | 100 | | | ps | |
| BW | PLL closed loop bandwidth[h] | F_RANGE = 00 | | | TBD | kHz | |
| | | F_RANGE = 01 | | | TBD | kHz | |
| | | F_RANGE = 10 | | | TBD | kHz | |
| | | F_RANGE = 11 | | | TBD | kHz | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 10 | | ms | |

a. All AC characteristics are design targets and subject to change upon device characterization.
b. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
c. PLL mode requires $\overline{PLL\_EN}$ = 0 to enable the PLL and zero–delay operation.
d. In bypass mode, the MPC9608 divides the input reference clock.
e. Applies for bank A and for bank B if BSEL = 0. If BSEL = 1, the min. and max. output frequency of bank B must be divided by two.
f. See application section for part–to–part skew calculation.
g. See application section for a jitter calculation for other confidence factors than 1 σ.
h. –3 dB point of PLL transfer characteristics.

**TABLE 8: DC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40° to 85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | –0.3 | | 0.7 | V | LVCMOS |
| $V_{OH}$ | Output High Voltage | 1.8 | | | V | $I_{OH}$=-15 mA[a] |
| $V_{OL}$ | Output Low Voltage | | | 0.6 | V | $I_{OL}$= 15 mA |
| $Z_{OUT}$ | Output Impedance | | 17 - 20 | | Ω | |
| $I_{IN}$ | Input Current | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CCA}$ | Maximum PLL Supply Current | | 2.0 | 5.0 | mA | $V_{CCA}$ Pin |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a. The MPC9608 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.

**TABLE 9: AC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40° to 85°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input reference frequency in PLL mode[c] | F_RANGE = 00 | 100 | | 200 | MHz | |
| | | F_RANGE = 01 | 50 | | 100 | MHz | |
| | | F_RANGE = 10 | 25 | | 50 | MHz | |
| | | F_RANGE = 11 | 12.5 | | 25 | MHz | |
| | Input reference frequency in PLL bypass mode[d] | | 0 | | TBD | MHz | |
| $f_{MAX}$ | Output Frequency[e] | F_RANGE = 00 | 100 | | 200 | MHz | BSEL = 0 |
| | | F_RANGE = 01 | 50 | | 100 | MHz | BSEL = 0 |
| | | F_RANGE = 10 | 25 | | 50 | MHz | BSEL = 0 |
| | | F_RANGE = 11 | 12.5 | | 25 | MHz | BSEL = 0 |
| $f_{refDC}$ | Reference Input Duty Cycle | | 25 | | 75 | % | |
| tr, tf | CCLK Input Rise/Fall Time | | | | 1.0 | ns | 0.7 to 1.7V |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) CCLK to FB_IN | | | | | | |
| | | F_RANGE = 00 | | ±100 | | ps | PLL locked |
| | | F_RANGE = 01 | | | | | |
| | | F_RANGE = 10 | | | | | |
| | | F_RANGE = 11 | | | | | |
| $t_{sk(o)}$ | Output-to-Output Skew[f] | | | | 150 | ps | |
| DC | Output Duty Cycle | | 45 | 50 | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.6 to 1.8V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 10 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 10 | ns | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ)[g] | | 15 | | ps | BSEL = 0 |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | 10 | | ps | BSEL = 0 |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1 σ) | | TBD | | ps | BSEL = 0 |
| $t_S$ | Setup time, CLK_STOP to CCLK | | 100 | | | ps | |
| $t_H$ | Hold time, CCLK to CLK_STOP | | 100 | | | ps | |
| BW | PLL closed loop bandwidth[h] | F_RANGE = 00 | | | TBD | kHz | |
| | | F_RANGE = 01 | | | TBD | kHz | |
| | | F_RANGE = 10 | | | TBD | kHz | |
| | | F_RANGE = 11 | | | TBD | kHz | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | 10 | | ms | |

a. All AC characteristics are design targets and subject to change upon device characterization.
b. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
c. PLL mode requires $\overline{PLL\_EN}$ = 0 to enable the PLL and zero–delay operation.
d. In bypass mode, the MPC9608 divides the input reference clock.
e. Applies for bank A and for bank B if BSEL = 0. If BSEL = 1, the min. and max. output frequency of bank B must be divided by two.
f. See application section for part–to–part skew calculation.
g. See application section for a jitter calculation for other confidence factors than 1 σ.
h. –3 dB point of PLL transfer characteristics.

## APPLICATIONS INFORMATION

### Power Supply Filtering

The MPC9608 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the $V_{CCA}$ (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC9608 provides separate power supplies for the output buffers ($V_{CC}$) and the phase-locked loop ($V_{CCA}$) of the device.The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the $V_{CCA}$ pin for the MPC9608. Figure 3 illustrates a typical power supply filter scheme. The MPC9608 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor $R_F$. From the data sheet the $I_{CCA}$ current (the current sourced through the $V_{CCA}$ pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V ($V_{CC}$=3.3V or $V_{CC}$=2.5V) must be maintained on the $V_{CCA}$ pin. The resistor $R_F$ shown in Figure 3 "$V_{CCA}$ Power Supply Filter" must have a resistance of 270Ω ($V_{CC}$=3.3V) or 9-10Ω ($V_{CC}$=2.5V) to meet the voltage drop criteria.

$R_F$ = 270Ω for $V_{CC}$ = 3.3V
$R_F$ = 9–10Ω for $V_{CC}$ = 2.5V

$C_F$ = 1 μF for $V_{CC}$ = 3.3V
$C_F$ = 22 μF for $V_{CC}$ = 2.5V

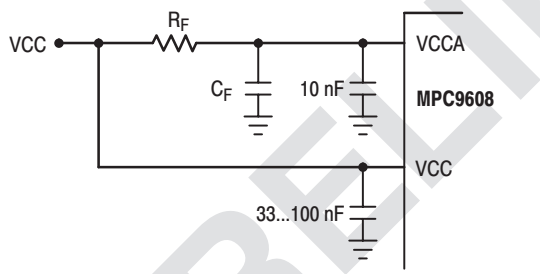



**Figure 3. $V_{CCA}$ Power Supply Filter**

The minimum values for $R_F$ and the filter capacitor $C_F$ are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3 "$V_{CCA}$ Power Supply Filter", the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9608 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

### Using the MPC9608 in zero–delay applications

Nested clock trees are typical applications for the MPC9608. Designs using the MPC9608 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC9608 clock driver allows for its use as a zero delay buffer. By using the QFB output as a feedback to the PLL the propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

### Calculation of part-to-part skew

The MPC9608 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9608 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\,LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consists of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

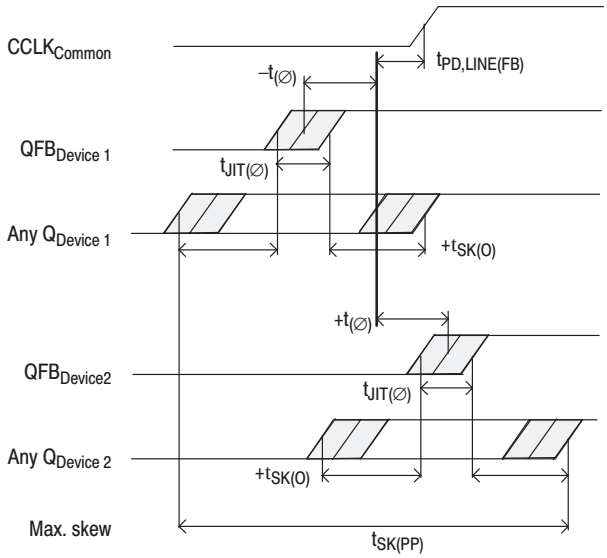



**Figure 4. MPC9608 max. device-to-device skew**

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 10.

**Table 10: Confidence Facter CF**

| CF | Probability of clock edge within the distribution |
|---|---|
| ± 1σ | 0.68268948 |
| ± 2σ | 0.95449988 |
| ± 3σ | 0.99730007 |
| ± 4σ | 0.99993663 |
| ± 5σ | 0.99999943 |
| ± 6σ | 0.99999999 |

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of -295 ps to 295 ps[1] relative to CCLK:

$t_{SK(PP)}$ = *[–100ps...100ps] + [–150ps...150ps] + [(15ps · –3)...(15ps · 3)] +* $t_{PD,\ LINE(FB)}$

$t_{SK(PP)}$ = *[–295ps...295ps] +* $t_{PD,\ LINE(FB)}$

Due to the frequency dependence of I/O jitter, Figure 5 ”Max. I/O Jitter versus frequency” can be used for a more precise timing performance analysis.

TBD

**Figure 5. Max. I/O Jitter versus frequency**

### Driving Transmission Lines

The MPC9608 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}$÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9608 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 6 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9608 clock driver is effectively doubled due to its capability to drive multiple lines.

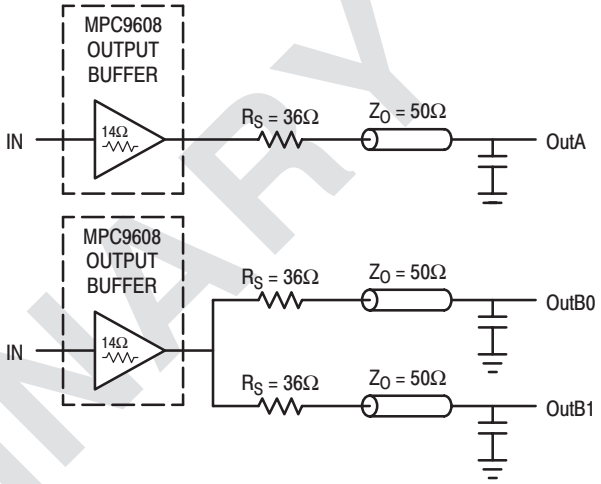



**Figure 6. Single versus Dual Transmission Lines**

The waveform plots in Figure 7 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9608 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9608. The output waveform in Figure 7 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$V_L = V_S ( Z_0 \div (R_S + R_0 + Z_0))$
$Z_0 = 50\Omega \parallel 50\Omega$
$R_S = 36\Omega \parallel 36\Omega$
$R_0 = 14\Omega$
$V_L = 3.0 ( 25 \div (18+17+25)$
$= 1.31V$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

1. Skew data are design targets and pending device specifications.

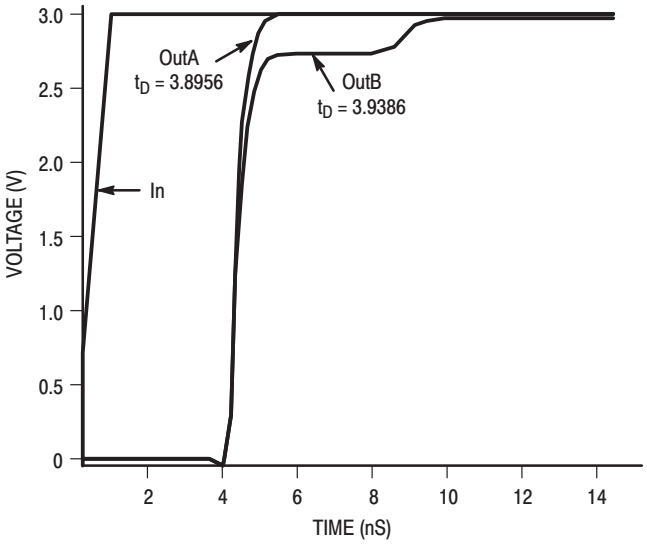
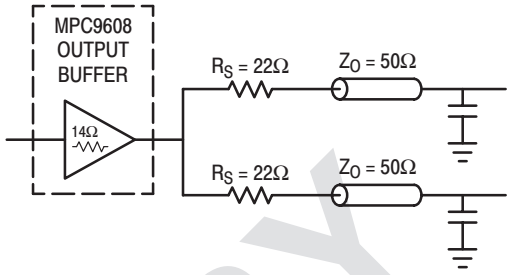



**Figure 7. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 8 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




14Ω + 22Ω || 22Ω = 50Ω || 50Ω
25Ω = 25Ω

**Figure 8. Optimized Dual Line Termination**

4

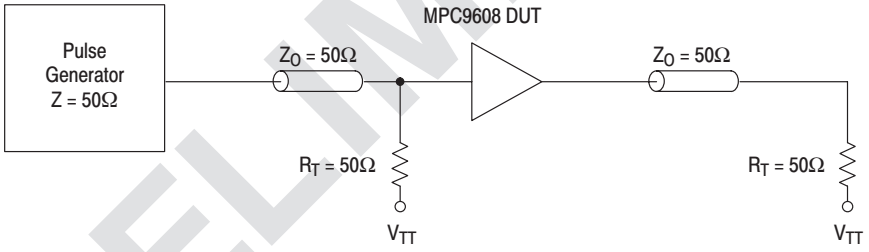
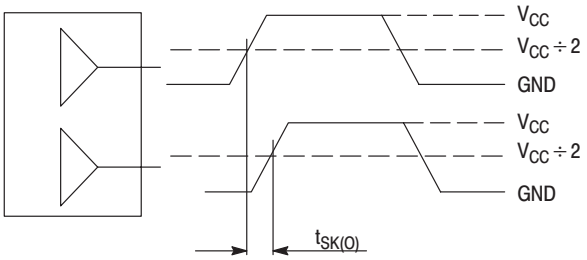



**Figure 9. CCLK MPC9608 AC test reference for $V_{cc}$ = 3.3V and $V_{cc}$ = 2.5V**




The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 10. Output–to–output Skew $t_{SK(O)}$**

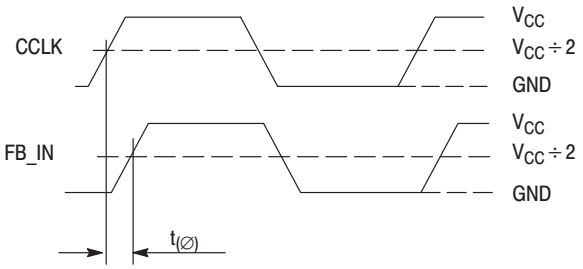
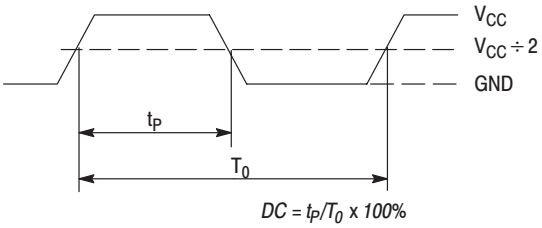
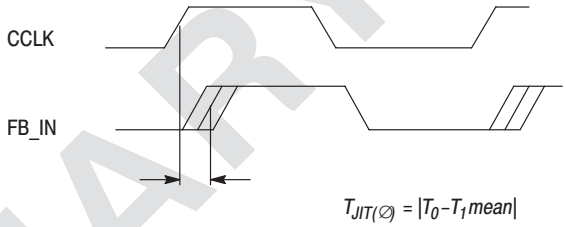



**Figure 11. Propagation delay ($t_{PD}$, static phase offset) test reference**



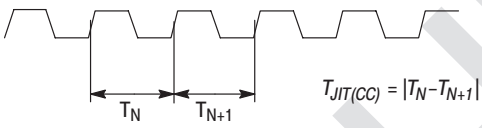

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 12. Output Duty Cycle (DC)**



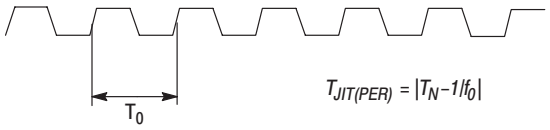

The deviation in $t_0$ for a controlled edge with respect to a $t_0$ mean in a random sample of cycles

**Figure 13. I/O Jitter**




The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

**Figure 14. Cycle–to–cycle Jitter**




The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

**Figure 15. Period Jitter**

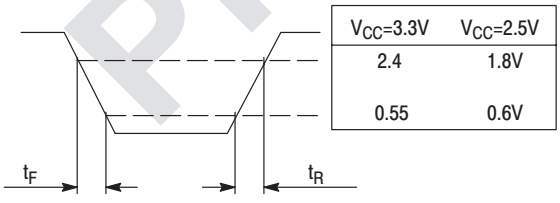



**Figure 16. Output Transition Time Test Reference**

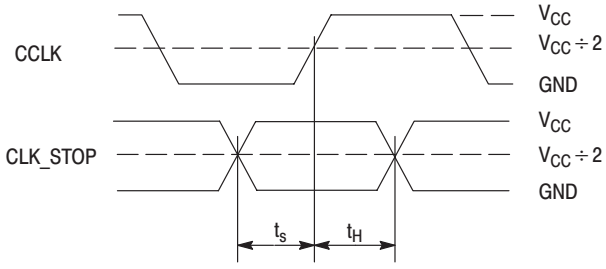



**Figure 17. Setup and Hold Time ($t_S$, $t_H$) Test Reference**

# Low Voltage Zero Delay Buffer

**MPC961C**

**LOW VOLTAGE ZERO DELAY BUFFER**

**FA SUFFIX**
32–LEAD LQFP PACKAGE
CASE 873A–02

4

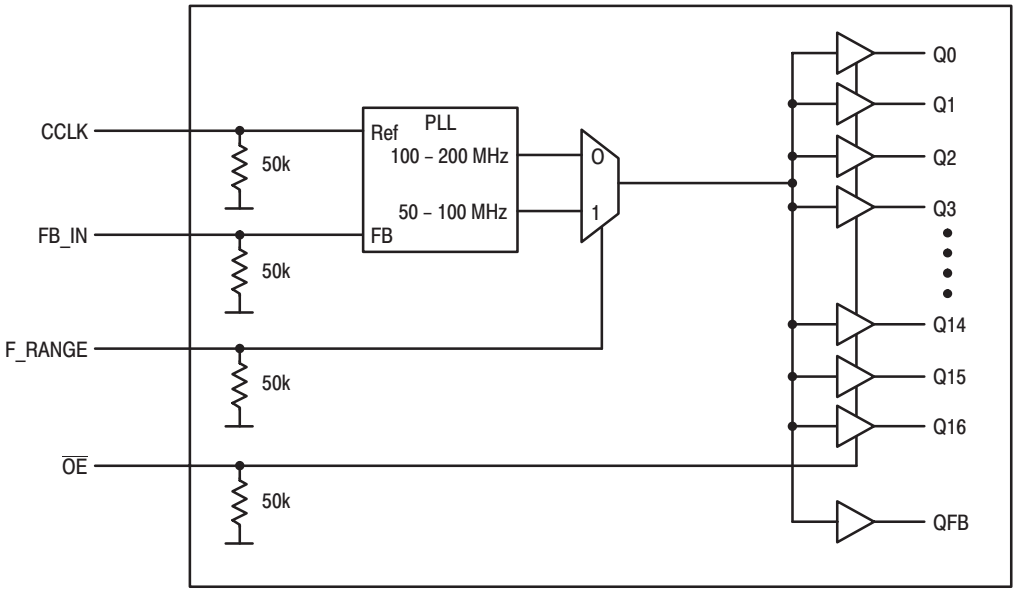
The MPC961 is a 2.5V or 3.3V compatible, 1:18 PLL based zero delay buffer. With output frequencies of up to 200MHz, output skews of 150ps the device meets the needs of the most demanding clock tree applications.

- Fully Integrated PLL
- Up to 200MHz I/O Frequency
- LVCMOS Outputs
- Outputs Disable in High Impedance
- LVCMOS Reference Clock Options
- LQFP Packaging
- ±50ps Cycle–Cycle Jitter
- 150ps Output Skews

The MPC961 is offered with two different input configurations. The MPC961C offers an LVCMOS reference clock while the MPC961P offers an LVPECL reference clock.

When pulled high the $\overline{OE}$ pin will force all of the outputs (except QFB) into a high impedance state. Because the $\overline{OE}$ pin does not affect the QFB output, down stream clocks can be disabled without the internal PLL losing lock.

The MPC961 is fully 2.5V or 3.3V compatible and requires no external loop filter components. All control inputs accept LVCMOS compatible levels and the outputs provide low impedance LVCMOS outputs capable of driving terminated 50Ω transmission lines. For series terminated lines the MPC961 can drive two lines per output giving the device an effective fanout of 1:36. The device is packaged in a 32 lead LQFP.




The MPC961C requires an external RC filter for the analog power supply pin $V_{CCA}$. Please see applications section for details.

**Figure 1. MPC961C Logic Diagram**

**Rev 1**

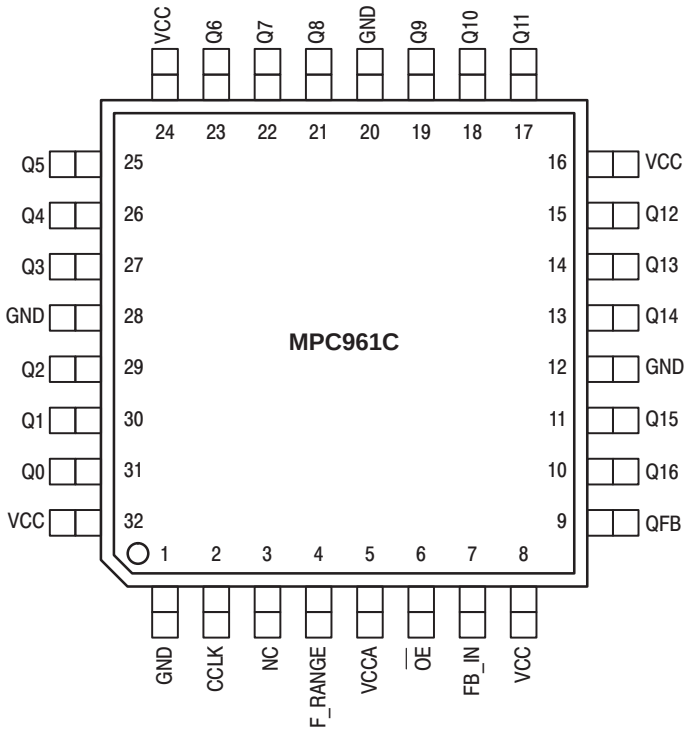



**Figure 2. 32–Lead Pinout** (Top View)

**Table 1: PIN CONFIGURATIONS**

| Pin | I/O | Type | Function |
|---|---|---|---|
| CCLK | Input | LVCMOS | PLL reference clock signal |
| FB_IN | Input | LVCMOS | PLL feedback signal input, connect to a QFB output |
| F_RANGE | Input | LVCMOS | PLL frequency range select |
| $\overline{OE}$ | Input | LVCMOS | Output enable/disable |
| Q0 - Q16 | Output | LVCMOS | Clock outputs |
| QFB | Output | LVCMOS | PLL feedback signal output, connect to a FB_IN |
| GND | Supply | Ground | Negative power supply |
| VCCA | Supply | VCC | PLL positive power supply (analog power supply). The MPC961C requires an external RC filter for the analog power supply pin $V_{CCA}$. Please see applications section for details. |
| VCC | Supply | VCC | Positive power supply for I/O and core |
| NC | | | Not connected |

**Table 2: FUNCTION TABLE**

| Control | Default | 0 | 1 |
|---|---|---|---|
| F_RANGE | 0 | PLL high frequency range. MPC961C input reference and output clock frequency range is 100 – 200 MHz | PLL low frequency range. MPC961C input reference and output clock frequency range is 50 – 100 MHz |
| $\overline{OE}$ | 0 | Outputs enabled | Outputs disabled (high–impedance state) |

**Table 3: ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 3.6 | V |
| $V_{IN}$ | DC Input Voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $V_{OUT}$ | DC Output Voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | DC Input Current | | ±20 | mA |
| $I_{OUT}$ | DC Output Current | | ±50 | mA |
| $T_S$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

**Table 4: DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40° to 85°C)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input LOW Voltage | –0.3 | | 0.8 | V | LVCMOS |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | $I_{OH}$ = –20mA[a] |
| $V_{OL}$ | Output LOW Voltage | | | 0.55 | V | $I_{OL}$ = 20mA[a] |
| $Z_{OUT}$ | Output Impedance | | 14 | 20 | Ω | |
| $I_{IN}$ | Input Current | | | ±120 | µA | |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | |
| $C_{PD}$ | Power Dissipation Capacitance | | 8.0 | 10 | pF | Per Output |
| $I_{CCA}$ | Maximum PLL Supply Current | | 2.0 | 5.0 | mA | $V_{CCA}$ Pin |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | | mA | All VCC Pins |
| $V_{TT}$ | Output Termination Voltage | | $V_{CC}$ ÷ 2 | | V | |

a. The MPC961C is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up two 50Ω series terminated transmission lines.

**Table 5: AC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40° to 85°C)[a]

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency | F_RANGE = 0<br>F_RANGE = 1 | 100<br>50 | | 200<br>100 | MHz | |
| $f_{max}$ | Maximum Output Frequency | F_RANGE = 0<br>F_RANGE = 1 | 100<br>50 | | 200<br>100 | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 25 | | 75 | % | |
| $t_r$, $t_f$ | TCLK Input Rise/Fall Time | | | | 3.0 | ns | 0.8 to 2.0V |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) | CCLK to FB_IN | –80 | | 120 | ps | PLL locked |
| $t_{sk(O)}$ | Output–to–Output Skew[b] | | | 90 | 150 | ps | |
| $DC_O$ | Output Duty Cycle | F_RANGE = 0<br>F_RANGE = 1 | 42<br>45 | 50<br>50 | 55<br>55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.55 to 2.4V |
| $t_{PLZ,HZ}$ | Output Disable Time | | | | 10 | ns | |
| $t_{PZL,LZ}$ | Output Enable Time | | | | 10 | ns | |
| $t_{JIT(CC)}$ | Cycle–to–Cycle Jitter | RMS (1 σ)[c] | | | 15 | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | 7.0 | 10 | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1 σ) | | | 15 | ns | |
| $t_{lock}$ | Maximum PLL Lock Time | | | | 10 | ms | |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$
b. See applications section for part–to–part skew calculation
c. See applications section for calculation for other confidence factors than 1 σ

**Table 6: DC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40° to 85°C)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input LOW Voltage | –0.3 | | 0.7 | V | LVCMOS |
| $V_{OH}$ | Output HIGH Voltage | 1.8 | | | V | $I_{OH}$ = –15mA[a] |
| $V_{OL}$ | Output LOW Voltage | | | 0.6 | V | $I_{OL}$ = 15mA[a] |
| $Z_{OUT}$ | Output Impedance | | 18 | 26 | Ω | |
| $I_{IN}$ | Input Current | | | ±120 | µA | |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | |
| $C_{PD}$ | Power Dissipation Capacitance | | 8.0 | 10 | pF | Per Output |
| $I_{CCA}$ | Maximum PLL Supply Current | | 2.0 | 5.0 | mA | $V_{CCA}$ Pin |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | | mA | All VCC Pins |
| $V_{TT}$ | Output Termination Voltage | | $V_{CC}$ ÷ 2 | | V | |

a. The MPC961C is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up two 50Ω series terminated transmission lines.

**Table 7: AC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40° to 85°C)[a]

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency | F_RANGE = 0<br>F_RANGE = 1 | 100<br>50 | | 200<br>100 | MHz | |
| $f_{max}$ | Maximum Output Frequency | F_RANGE = 0<br>F_RANGE = 1 | 100<br>50 | | 200<br>100 | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 25 | | 75 | % | |
| $t_r$, $t_f$ | TCLK Input Rise/Fall Time | | | | 3.0 | ns | 0.7 to 1.7V |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) | CCLK to FB_IN | –80 | | 120 | ps | PLL locked |
| $t_{sk(O)}$ | Output–to–Output Skew[b] | | | 90 | 150 | ps | |
| $DC_O$ | Output Duty Cycle | F_RANGE = 0<br>F_RANGE = 1 | 40<br>45 | 50<br>50 | 60<br>55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.6 to 1.8V |
| $t_{PLZ,HZ}$ | Output Disable Time | | | | 10 | ns | |
| $t_{PZL,LZ}$ | Output Enable Time | | | | 10 | ns | |
| $t_{JIT(CC)}$ | Cycle–to–Cycle Jitter | RMS (1 σ)[c] | | | 15 | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | 7.0 | 10 | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1 σ) | | | 15 | ns | |
| $t_{lock}$ | Maximum PLL Lock Time | | | | 10 | ms | |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$
b. See applications section for part–to–part skew calculation
c. See applications section for calculation for other confidence factors than 1 σ

**Power Supply Filtering**

The MPC961C is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC961C provides separate power supplies for the output buffers ($V_{CC}$) and the phase–locked loop ($V_{CCA}$) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the $V_{CCA}$ pin for the MPC961C.

Figure 3 illustrates a typical power supply filter scheme. The MPC961C is most susceptible to noise with spectral content in the 10kHz to 10MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the $V_{CCA}$ pin of the MPC961C. From the data sheet the $I_{CCA}$ current (the current sourced through the $V_{CCA}$ pin) is typically 2mA (5mA maximum), assuming that a minimum of 2.375V ($V_{CC}$ = 3.3V or $V_{CC}$ = 2.5V) must be maintained on the $V_{CCA}$ pin. The resistor $R_F$ shown in Figure 3 must have a resistance of 270Ω ($V_{CC}$ = 3.3V) or 5 to 15Ω ($V_{CC}$ = 2.5V) to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20kHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

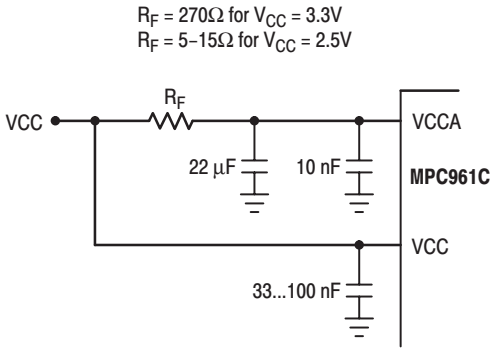



**Figure 3. Power Supply Filter**

Although the MPC961C has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Driving Transmission Lines**

The MPC961C clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 15Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091.

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC961C clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC961C clock driver is effectively doubled due to its capability to drive multiple lines.



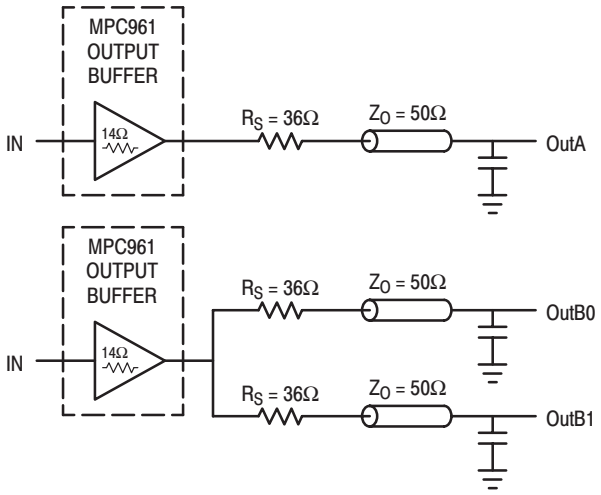



**Figure 4. Single versus Dual Transmission Lines**

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC961C output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC961C. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

VL = VS ( Zo / (Rs + Ro +Zo))
Zo = 50Ω || 50Ω
Rs = 36Ω || 36Ω
Ro = 14Ω
VL = 3.0 (25 / (18 + 14 + 25) = 3.0 (25 / 57)
= 1.31V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.62V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

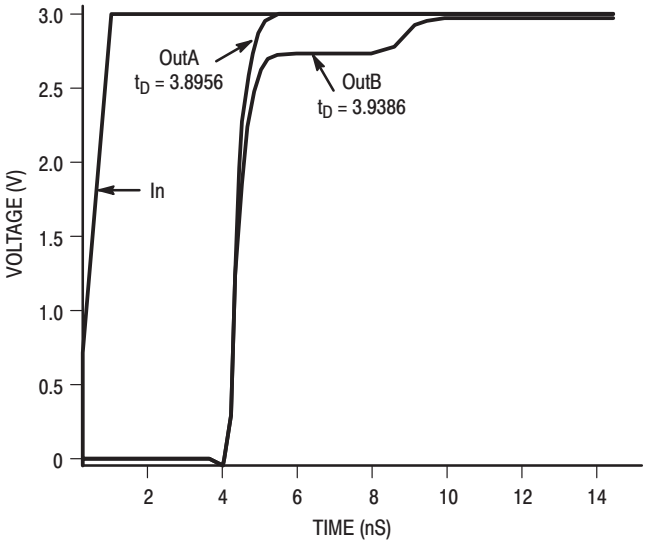
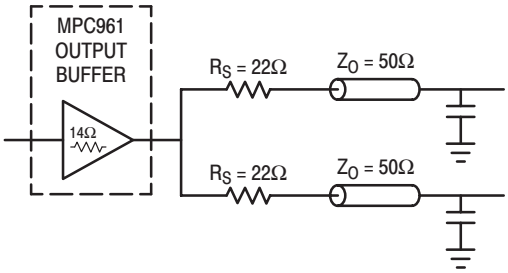



**Figure 5. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




14Ω + 22Ω || 22Ω = 50Ω || 50Ω
25Ω = 25Ω

**Figure 6. Optimized Dual Line Termination**

SPICE level and IBIS output buffer models are available for engineers who want to simulate their specific interconnect schemes.

**Using the MPC961C in zero-delay applications**

Nested clock trees are typical applications for the MPC961C. Designs using the MPC961C as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC961C clock driver allows for its use as a zero delay buffer. By using the QFB output as a feedback to the PLL the propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

**Calculation of part-to-part skew**

The MPC961C zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC961C are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

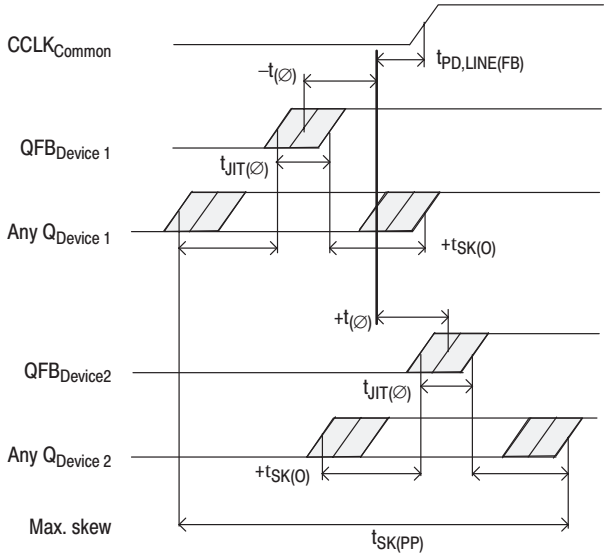



**Figure 7. MPC961C max. device-to-device skew**

Due to the statistical nature of I/O jitter a rms value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

**Table 8: Confidence Facter CF**

| CF | Probability of clock edge within the distribution |
|---|---|
| ± 1σ | 0.68268948 |
| ± 2σ | 0.95449988 |
| ± 3σ | 0.99730007 |
| ± 4σ | 0.99993663 |
| ± 5σ | 0.99999943 |
| ± 6σ | 0.99999999 |

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of -275 ps to 315 ps relative to CCLK:

$t_{SK(PP)}$ = *[–80ps...120ps] + [–150ps...150ps] + [(15ps · –3)...(15ps · 3)] +* $t_{PD,\ LINE(FB)}$

$t_{SK(PP)}$ = *[–275ps...315ps] +* $t_{PD,\ LINE(FB)}$

Due to the frequency dependence of the I/O jitter, Figure 8 “Max. I/O Jitter versus frequency” can be used for a more precise timing performance analysis.

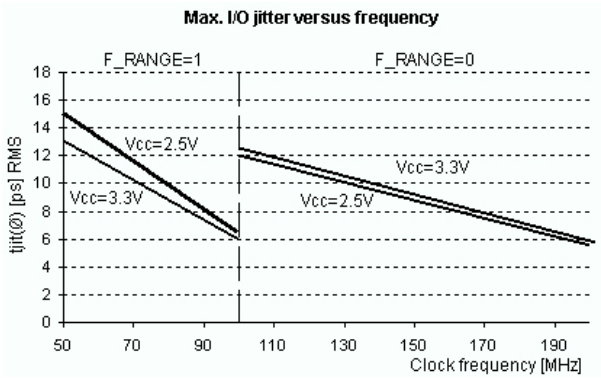



**Figure 8. Max. I/O Jitter versus frequency**

### Power Consumption of the MPC961C and Thermal Management

The MPC961C AC specification is guaranteed for the entire operating frequency range up to 200 MHz. The MPC961C power consumption and the associated long-term reliability may decrease the maximum frequency limit, depending on operating conditions such as clock frequency, supply voltage, output loading, ambient temperature, vertical convection and thermal conductivity of package and board. This section describes the impact of these parameters on the junction temperature and gives a guideline to estimate the MPC961C die junction temperature and the associated device reliability. For a complete analysis of power consumption as a function of operating conditions and associated long term device reliability please refer to the application note AN1545. According the AN1545, the long-term device reliability is a function of the die junction temperature:

**Table 9: Die junction temperature and MTBF**

| Junction temperature (°C) | MTBF (Years) |
|---|---|
| 100 | 20.4 |
| 110 | 9.1 |
| 120 | 4.2 |
| 130 | 2.0 |

Increased power consumption will increase the die junction temperature and impact the device reliability (MTBF). According to the system-defined tolerable MTBF, the die junction temperature of the MPC961C needs to be controlled and the thermal impedance of the board/package should be optimized. The power dissipated in the MPC961C is represented in equation 1.

Where $I_{CCQ}$ is the static current consumption of the MPC961C, $C_{PD}$ is the power dissipation capacitance per output, $(M)\Sigma C_L$ represents the external capacitive output load, N is the number of active outputs (N is always 27 in case of the MPC961C). The MPC961C supports driving transmission lines to maintain high signal integrity and tight timing parameters. Any transmission line will hide the lumped capacitive load at the end of the board trace, therefore, $\Sigma C_L$ is zero for controlled transmission line systems and can be eliminated from equation 1. Using parallel termination output termination results in equation 2 for power dissipation.

In equation 2, P stands for the number of outputs with a parallel or thevenin termination, $V_{OL}$, $I_{OL}$, $V_{OH}$ and $I_{OH}$ are a function of the output termination technique and $DC_Q$ is the clock signal duty cyle. If transmission lines are used $\Sigma C_L$ is zero in equation 2 and can be eliminated. In general, the use of controlled transmission line techniques eliminates the impact of the lumped capacitive loads at the end lines and greatly reduces the power dissipation of the device. Equation 3 describes the die junction temperature $T_J$ as a function of the power consumption.

$$P_{TOT} = \left[ I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left( N \cdot C_{PD} + \sum_{M} C_L \right) \right] \cdot V_{CC} \qquad \text{Equation 1}$$

$$P_{TOT} = V_{CC} \cdot \left[ I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left( N \cdot C_{PD} + \sum_{M} C_L \right) \right] + \sum_{P} \left[ DC_Q \cdot I_{OH} \cdot (V_{CC} - V_{OH}) + (1 - DC_Q) \cdot I_{OL} \cdot V_{OL} \right] \qquad \text{Equation 2}$$

$$T_J = T_A + P_{TOT} \cdot R_{thja} \qquad \text{Equation 3}$$

$$f_{CLOCK,MAX} = \frac{1}{C_{PD} \cdot N \cdot V_{CC}^2} \cdot \left[ \frac{T_{J,MAX} - T_A}{R_{thja}} - (I_{CCQ} \cdot V_{CC}) \right] \qquad \text{Equation 4}$$

Where $R_{thja}$ is the thermal impedance of the package (junction to ambient) and $T_A$ is the ambient temperature. According to Table 9, the junction temperature can be used to estimate the long-term device reliability. Further, combining equation 1 and equation 2 results in a maximum operating frequency for the MPC961C in a series terminated transmission line system.

**Table 10: Thermal package impedance of the 32ld LQFP**

| Convection, LFPM | $R_{thja}$ (1P2S board), K/W |
|---|---|
| Still air | 80 |
| 100 lfpm | 70 |
| 200 lfpm | 61 |
| 300 lfpm | 57 |
| 400 lfpm | 56 |
| 500 lfpm | 55 |

$T_{J,MAX}$ should be selected according to the MTBF system requirements and Table 9. $R_{thja}$ can be derived from Table 10. The $R_{thja}$ represent data based on 1S2P boards, using 2S2P boards will result in a lower thermal impedance than indicated below.

If the calculated maximum frequency is below 200 MHz, it becomes the upper clock speed limit for the given application conditions. The following two derating charts describe the safe frequency operation range for the MPC961C. The charts were calculated for a maximum tolerable die junction temperature of 110°C, corresponding to an estimated MTBF of 9.1 years, a supply voltage of 3.3V and series terminated transmission line or capacitive loading. Depending on a given set of these operating conditions and the available device convection a decision on the maximum operating frequency can be made. There are no operating frequency limitations if a 2.5V power supply or the system specifications allow for a MTBF of 4 years (corresponding to a max. junction temperature of 120°C.



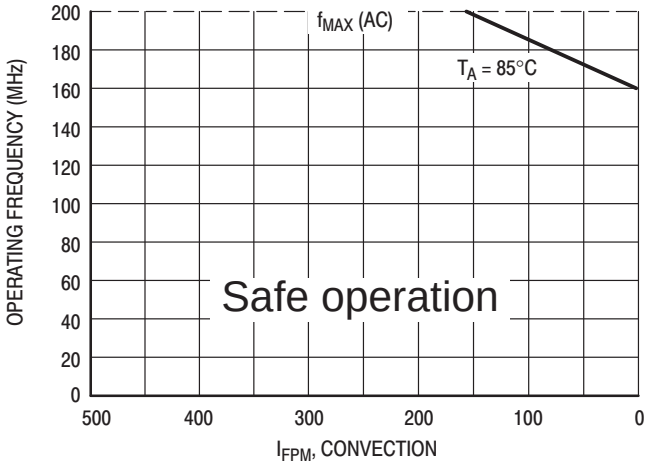



**Figure 9. Maximum MPC961C frequency, $V_{CC}$ = 3.3V, MTBF 9.1 years, driving series terminated transmission lines**

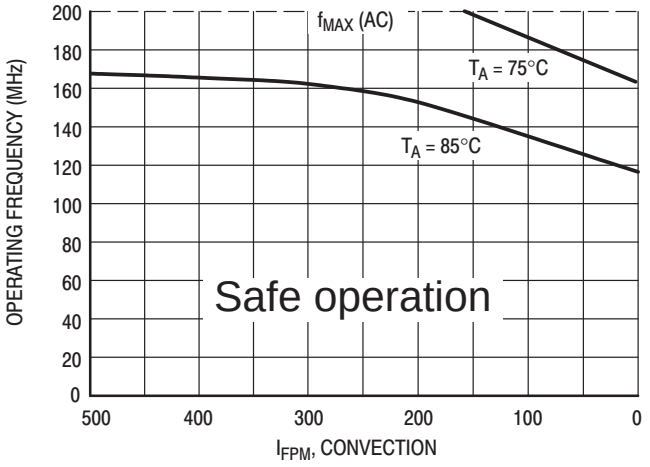



**Figure 10. Maximum MPC961C frequency, $V_{CC}$ = 3.3V, MTBF 9.1 years, 4 pF load per line**

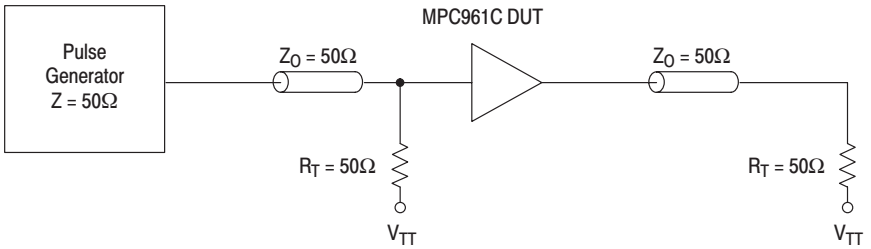
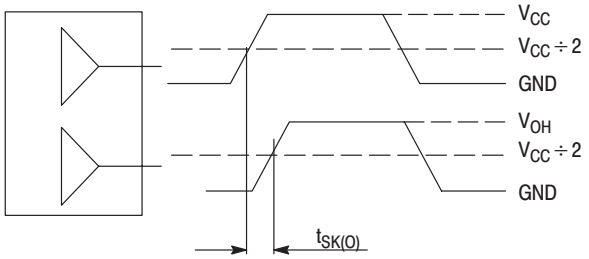



**Figure 11. TCLK MPC961C AC test reference for $V_{cc}$ = 3.3V and $V_{cc}$ = 2.5V**




The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 12. Output–to–output Skew $t_{SK(O)}$**

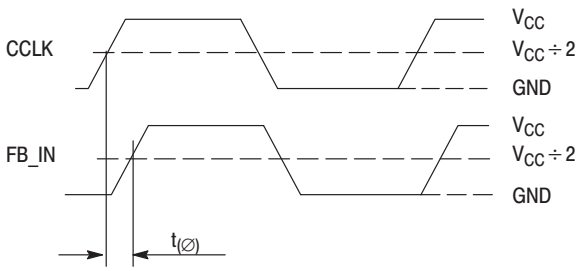
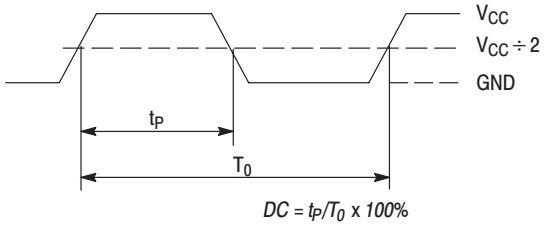
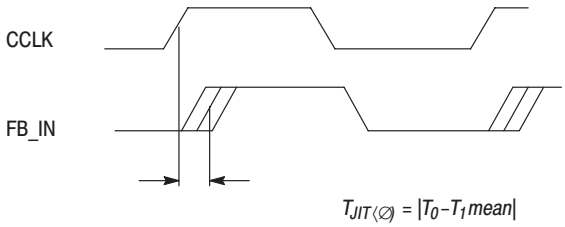



**Figure 13. Propagation delay ($t_{PD}$, static phase offset) test reference**



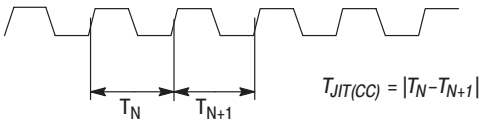

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 14. Output Duty Cycle (DC)**



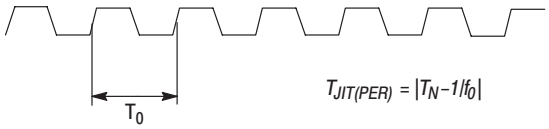

The deviation in $t_0$ for a controlled edge with respect to a $t_0$ mean in a random sample of cycles

**Figure 15. I/O Jitter**




The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

**Figure 16. Cycle–to–cycle Jitter**




The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

**Figure 17. Period Jitter**

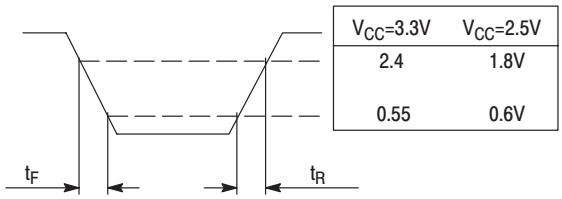



**Figure 18. Output Transition Time Test Reference**

go

# Low Voltage Zero Delay Buffer

**MPC961P**

**LOW VOLTAGE ZERO DELAY BUFFER**

**FA SUFFIX**
32–LEAD LQFP PACKAGE
CASE 873A–02

The MPC961 is a 2.5V or 3.3V compatible, 1:18 PLL based zero delay buffer. With output frequencies of up to 200MHz, output skews of 150ps the device meets the needs of the most demanding clock tree applications.

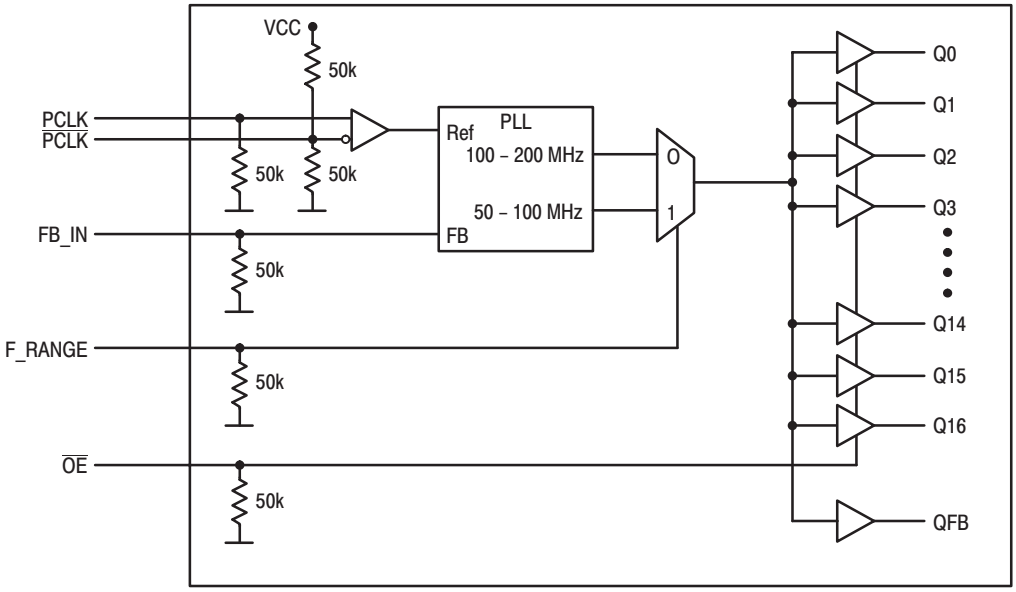
- Fully Integrated PLL
- Up to 200MHz I/O Frequency
- LVCMOS Outputs
- Outputs Disable in High Impedance
- LVPECL Reference Clock Options
- LQFP Packaging
- ±50ps Cycle–Cycle Jitter
- 150ps Output Skews

4

The MPC961 is offered with two different input configurations. The MPC961C offers an LVCMOS reference clock while the MPC961P offers an LVPECL reference clock.

When pulled high the $\overline{OE}$ pin will force all of the outputs (except QFB) into a high impedance state. Because the $\overline{OE}$ pin does not affect the QFB output, down stream clocks can be disabled without the internal PLL losing lock.

The MPC961 is fully 2.5V or 3.3V compatible and requires no external loop filter components. All control inputs accept LVCMOS compatible levels and the outputs provide low impedance LVCMOS outputs capable of driving terminated 50Ω transmission lines. For series terminated lines the MPC961 can drive two lines per output giving the device an effective fanout of 1:36. The device is packaged in a 32 lead LQFP package to provide the optimum combination of board density and performance.




The MPC961P requires an external RC filter for the analog power supply pin $V_{CCA}$. Please see applications section for details.

**Figure 1. MPC961P Logic Diagram**

**Rev 2**

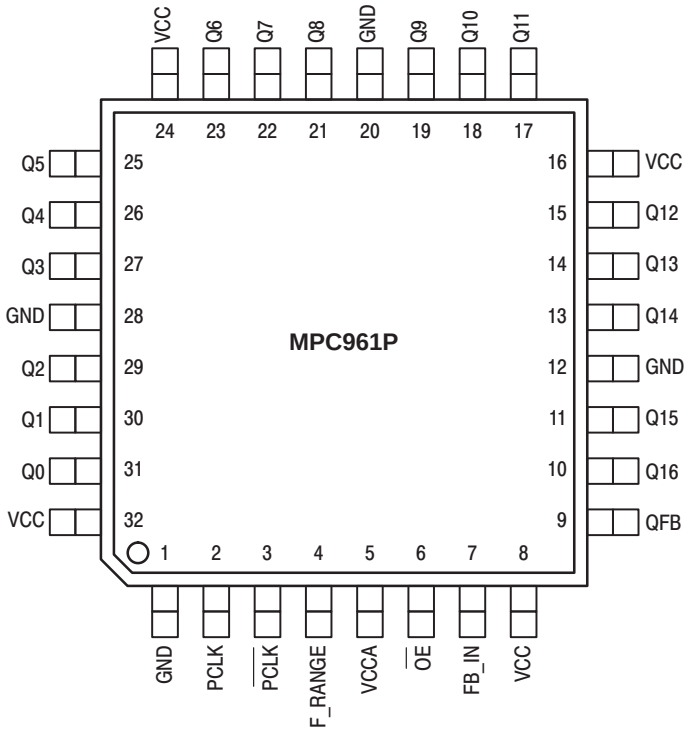



**Figure 2. 32–Lead Pinout** (Top View)

**Table 1: PIN CONFIGURATIONS**

| Pin | I/O | Type | Function |
|---|---|---|---|
| PCLK, $\overline{\text{PCLK}}$ | Input | LVCMOS | PLL reference clock signal |
| FB_IN | Input | LVCMOS | PLL feedback signal input, connect to a QFB output |
| F_RANGE | Input | LVCMOS | PLL frequency range select |
| $\overline{\text{OE}}$ | Input | LVCMOS | Output enable/disable |
| Q0 - Q16 | Output | LVCMOS | Clock outputs |
| QFB | Output | LVCMOS | PLL feedback signal output, connect to a FB_IN |
| GND | Supply | Ground | Negative power supply |
| VCCA | Supply | VCC | PLL positive power supply (analog power supply). The MPC961P requires an external RC filter for the analog power supply pin $V_{CCA}$. Please see applications section for details. |
| VCC | Supply | VCC | Positive power supply for I/O and core |

**Table 2: FUNCTION TABLE**

| Control | Default | 0 | 1 |
|---|---|---|---|
| F_RANGE | 0 | PLL high frequency range. MPC961P input reference and output clock frequency range is 100 – 200 MHz | PLL low frequency range. MPC961P input reference and output clock frequency range is 50 – 100 MHz |
| $\overline{\text{OE}}$ | 0 | Outputs enabled | Outputs disabled (high–impedance state) |

**Table 3: ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 3.6 | V |
| $V_{IN}$ | DC Input Voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $V_{OUT}$ | DC Output Voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | DC Input Current | | ±20 | mA |
| $I_{OUT}$ | DC Output Current | | ±50 | mA |
| $T_S$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

**Table 4: DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40° to 85°C)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input LOW Voltage | –0.3 | | 0.8 | V | LVCMOS |
| $V_{PP}$ | Peak–to–peak input voltage[a] PECL_CLK, $\overline{\text{PECL\_CLK}}$ | 500 | | 1000 | mV | LVPECL |
| $V_{CMR}$ | Common Mode Range[a] PECL_CLK, $\overline{\text{PECL\_CLK}}$ | 1.2 | | $V_{CC}$ – 0.8 | V | LVPECL |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | $I_{OH}$ = –20mA[b] |
| $V_{OL}$ | Output LOW Voltage | | | 0.55 | V | $I_{OL}$ = 20mA[b] |
| $Z_{OUT}$ | Output Impedance | | 14 | 20 | Ω | |
| $I_{IN}$ | Input Current | | | ±120 | µA | |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | |
| $C_{PD}$ | Power Dissipation Capacitance | | 8.0 | 10 | pF | Per Output |
| $I_{CCA}$ | Maximum PLL Supply Current | | 2.0 | 5.0 | mA | $V_{CCA}$ Pin |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | | mA | All VCC Pins |
| $V_{TT}$ | Output Termination Voltage | | $V_{CC}$ ÷ 2 | | V | |

a. Exceeding the specified $V_{CMR}/V_{PP}$ window results in a $t_{PD}$ changes of approx. 250 ps.
b. The MPC961P is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up two 50Ω series terminated transmission lines.

**Table 5: AC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40° to 85°C)[a]

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency | F_RANGE = 0<br>F_RANGE = 1 | 100<br>50 | | 200<br>100 | MHz | |
| $f_{max}$ | Maximum Output Frequency | F_RANGE = 0<br>F_RANGE = 1 | 100<br>50 | | 200<br>100 | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 25 | | 75 | % | |
| $t_{(\varnothing)}$ | Propagation Delay[b] (static phase offset) | PECL_CLK to FB_IN | –50 | | 225 | ps | PLL locked |
| $t_{sk(O)}$ | Output–to–Output Skew[c] | | | 90 | 150 | ps | |
| $DC_O$ | Output Duty Cycle | F_RANGE = 0<br>F_RANGE = 1 | 42<br>45 | 50<br>50 | 55<br>55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.55 to 2.4V |
| $t_{PLZ,HZ}$ | Output Disable Time | | | | 10 | ns | |
| $t_{PZL,LZ}$ | Output Enable Time | | | | 10 | ns | |
| $t_{JIT(CC)}$ | Cycle–to–Cycle Jitter | RMS (1 σ)[d] | | | 15 | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | 7.0 | 10 | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1 σ) F_RANGE = 0<br>F_RANGE = 1 | | | 0.0015 · T<br>0.0010 · T | ns | T = Clock Signal Period |
| $t_{lock}$ | Maximum PLL Lock Time | | | | 10 | ms | |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$
b. $t_{PD}$ applies for $V_{CMR} = V_{CC}$–1.3V and $V_{PP}$ = 800mV
c. See applications section for part–to–part skew calculation
d. See applications section for calculation for other confidence factors than 1 σ

**Table 6: DC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40° to 85°C)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input LOW Voltage | –0.3 | | 0.7 | V | LVCMOS |
| $V_{PP}$ | Peak–to–peak input voltage[a] PECL_CLK, $\overline{\text{PECL\_CLK}}$ | 500 | | 1000 | mV | LVPECL |
| $V_{CMR}$ | Common Mode Range[a] PECL_CLK, $\overline{\text{PECL\_CLK}}$ | 1.2 | | $V_{CC}$ – 0.7 | V | LVPECL |
| $V_{OH}$ | Output HIGH Voltage | 1.8 | | | V | $I_{OH}$ = –15mA[b] |
| $V_{OL}$ | Output LOW Voltage | | | 0.6 | V | $I_{OL}$ = 15mA[b] |
| $Z_{OUT}$ | Output Impedance | | 18 | 26 | Ω | |
| $I_{IN}$ | Input Current | | | ±120 | µA | |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | |
| $C_{PD}$ | Power Dissipation Capacitance | | 8.0 | 10 | pF | Per Output |
| $I_{CCA}$ | Maximum PLL Supply Current | | 2.0 | 5.0 | mA | $V_{CCA}$ Pin |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | | mA | All VCC Pins |
| $V_{TT}$ | Output Termination Voltage | | $V_{CC}$ ÷ 2 | | V | |

a. Exceeding the specified $V_{CMR}/V_{PP}$ window results in a $t_{PD}$ changes < 250 ps.
b. The MPC961P is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up two 50Ω series terminated transmission lines.

**Table 7: AC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40° to 85°C)[a]

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency | F_RANGE = 0<br>F_RANGE = 1 | 100<br>50 | | 200<br>100 | MHz | |
| $f_{max}$ | Maximum Output Frequency | F_RANGE = 0<br>F_RANGE = 1 | 100<br>50 | | 200<br>100 | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 25 | | 75 | % | |
| $t_{(\varnothing)}$ | Propagation Delay[b] (static phase offset) | PCLK to FB_IN | –50 | | 175 | ps | PLL locked |
| $t_{sk(O)}$ | Output–to–Output Skew[c] | | | 90 | 150 | ps | |
| $DC_O$ | Output Duty Cycle | F_RANGE = 0<br>F_RANGE = 1 | 40<br>45 | 50<br>50 | 60<br>55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.6 to 1.8V |
| $t_{PLZ,HZ}$ | Output Disable Time | | | | 10 | ns | |
| $t_{PZL,LZ}$ | Output Enable Time | | | | 10 | ns | |
| $t_{JIT(CC)}$ | Cycle–to–Cycle Jitter | RMS (1 σ)[d] | | | 15 | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | 7.0 | 10 | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1 σ) F_RANGE = 0<br>F_RANGE = 1 | | | 0.0015 · T<br>0.0010 · T | ns | T = Clock Signal Period |
| $t_{lock}$ | Maximum PLL Lock Time | | | | 10 | ms | |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$
b. $t_{PD}$ applies for $V_{CMR} = V_{CC}–1.3V$ and $V_{PP}$ = 800mV
c. See applications section for part–to–part skew calculation
d. See applications section for calculation for other confidence factors than 1 σ

**Power Supply Filtering**

The MPC961P is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC961P provides separate power supplies for the output buffers ($V_{CC}$) and the phase–locked loop ($V_{CCA}$) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the $V_{CCA}$ pin for the MPC961P.

Figure 3 illustrates a typical power supply filter scheme. The MPC961P is most susceptible to noise with spectral content in the 10kHz to 5MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the $V_{CCA}$ pin of the MPC961P. From the data sheet the $I_{CCA}$ current (the current sourced through the $V_{CCA}$ pin) is typically 2mA (5mA maximum), assuming that a minimum of 2.375V ($V_{CC}$ = 3.3V or $V_{CC}$ = 2.5V) must be maintained on the $V_{CCA}$ pin. The resistor $R_F$ shown in Figure 3 must have a resistance of 270Ω ($V_{CC}$ = 3.3V) or 5 to 15Ω ($V_{CC}$ = 2.5V) to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20kHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

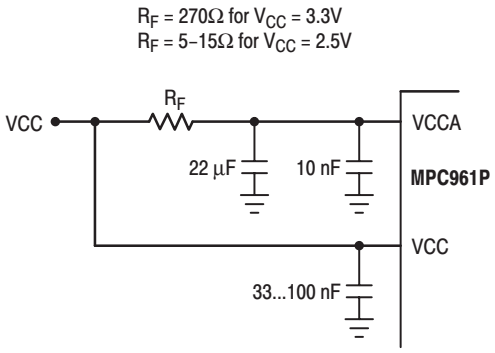



**Figure 3. Power Supply Filter**

Although the MPC961P has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Driving Transmission Lines**

The MPC961P clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 15Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091.

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC961P clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC961P clock driver is effectively doubled due to its capability to drive multiple lines.



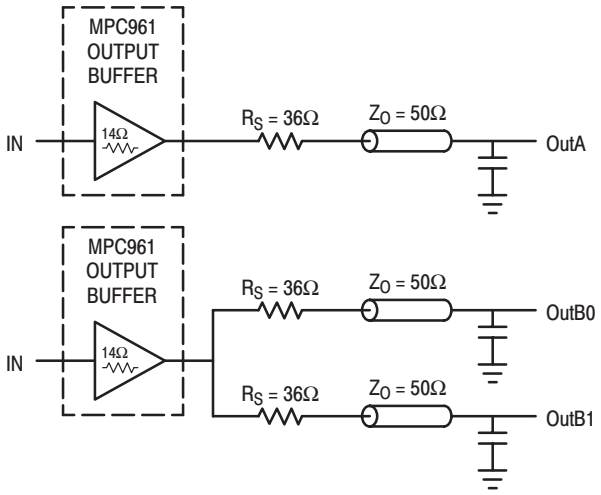



**Figure 4. Single versus Dual Transmission Lines**

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC961P output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC961P. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

VL = VS ( Zo / (Rs + Ro +Zo))
Zo = 50Ω || 50Ω
Rs = 36Ω || 36Ω
Ro = 14Ω
VL = 3.0 (25 / (18 + 14 + 25) = 3.0 (25 / 57)
= 1.31V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.62V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

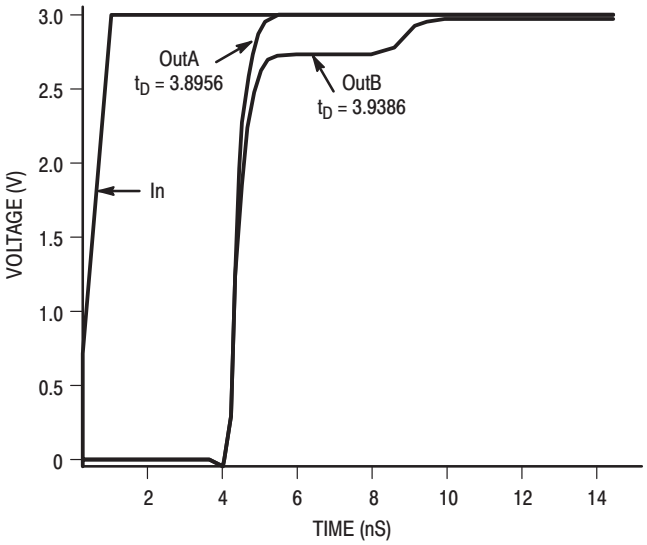
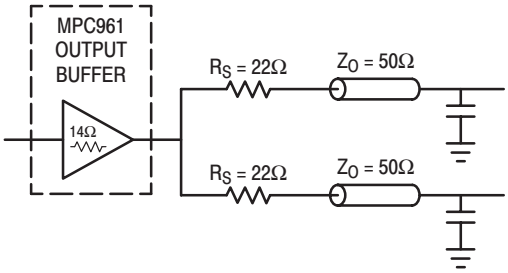



**Figure 5. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




14Ω + 22Ω || 22Ω = 50Ω || 50Ω
25Ω = 25Ω

**Figure 6. Optimized Dual Line Termination**

SPICE level and IBIS output buffer models are available for engineers who want to simulate their specific interconnect schemes.

**Using the MPC961P in zero-delay applications**

Nested clock trees are typical applications for the MPC961P. Designs using the MPC961P as LVCMOS PLL fan-out buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fan-out buffers. The external feedback option of the MPC961P clock driver allows for its use as a zero delay buffer. By using the QFB output as a feedback to the PLL the propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

**Calculation of part-to-part skew**

The MPC961P zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC961P are connected together, the maximum overall timing uncertainty from the common PCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

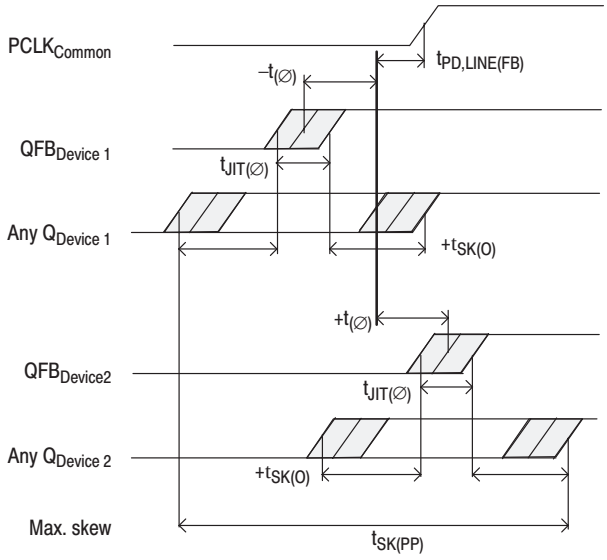



**Figure 7. MPC961P max. device-to-device skew**

Due to the statistical nature of I/O jitter a rms value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

**Table 8: Confidence Facter CF**

| CF | Probability of clock edge within the distribution |
|---|---|
| ± 1σ | 0.68268948 |
| ± 2σ | 0.95449988 |
| ± 3σ | 0.99730007 |
| ± 4σ | 0.99993663 |
| ± 5σ | 0.99999943 |
| ± 6σ | 0.99999999 |

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of -236 ps to 361 ps relative to PCLK (f=125 MHz, $V_{CC}$=2.5V):

$t_{SK(PP)}$ = [–50ps...175ps] + [–150ps...150ps] + [(12ps · –3)...(12ps · 3)] + $t_{PD, LINE(FB)}$

$t_{SK(PP)}$ = [–236ps...361ps] + $t_{PD, LINE(FB)}$

Due to the frequency dependence of the I/O jitter, Figure 8 “Max. I/O Jitter versus frequency” can be used for a more precise timing performance analysis.

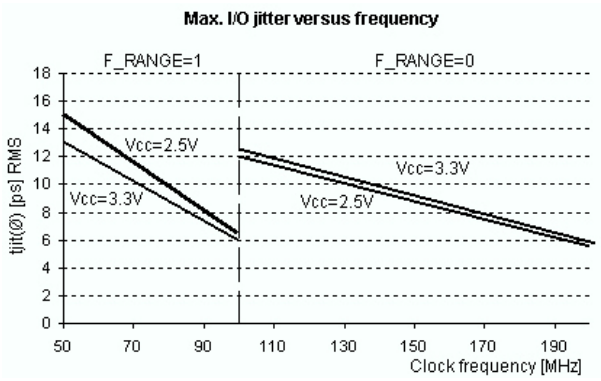



**Figure 8. Max. I/O Jitter versus frequency**

**Power Consumption of the MPC961P and Thermal Management**

The MPC961P AC specification is guaranteed for the entire operating frequency range up to 200 MHz. The MPC961P power consumption and the associated long-term reliability may decrease the maximum frequency limit, depending on operating conditions such as clock frequency, supply voltage, output loading, ambient temperature, vertical convection and thermal conductivity of package and board. This section describes the impact of these parameters on the junction temperature and gives a guideline to estimate the MPC961P die junction temperature and the associated device reliability. For a complete analysis of power consumption as a function of operating conditions and associated long term device reliability please refer to the application note AN1545. According the AN1545, the long-term device reliability is a function of the die junction temperature:

**Table 9: Die junction temperature and MTBF**

| Junction temperature (°C) | MTBF (Years) |
|---|---|
| 100 | 20.4 |
| 110 | 9.1 |
| 120 | 4.2 |
| 130 | 2.0 |

Increased power consumption will increase the die junction temperature and impact the device reliability (MTBF). According to the system-defined tolerable MTBF, the die junction temperature of the MPC961P needs to be controlled and the thermal impedance of the board/package should be optimized. The power dissipated in the MPC961P is represented in equation 1.

Where $I_{CCQ}$ is the static current consumption of the MPC961P, $C_{PD}$ is the power dissipation capacitance per output, $(M)\Sigma C_L$ represents the external capacitive output load, N is the number of active outputs (N is always 27 in case of the MPC961P). The MPC961P supports driving transmission lines to maintain high signal integrity and tight timing parameters. Any transmission line will hide the lumped capacitive load at the end of the board trace, therefore, $\Sigma C_L$ is zero for controlled transmission line systems and can be eliminated from equation 1. Using parallel termination output termination results in equation 2 for power dissipation.

In equation 2, P stands for the number of outputs with a parallel or thevenin termination, $V_{OL}$, $I_{OL}$, $V_{OH}$ and $I_{OH}$ are a function of the output termination technique and $DC_Q$ is the clock signal duty cyle. If transmission lines are used $\Sigma C_L$ is zero in equation 2 and can be eliminated. In general, the use of controlled transmission line techniques eliminates the impact of the lumped capacitive loads at the end lines and greatly reduces the power dissipation of the device. Equation 3 describes the die junction temperature $T_J$ as a function of the power consumption.

$$P_{TOT} = \left[ I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left( N \cdot C_{PD} + \sum_{M} C_L \right) \right] \cdot V_{CC} \quad \text{Equation 1}$$

$$P_{TOT} = V_{CC} \cdot \left[ I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left( N \cdot C_{PD} + \sum_{M} C_L \right) \right] + \sum_{P} \left[ DC_Q \cdot I_{OH} \cdot (V_{CC} - V_{OH}) + (1 - DC_Q) \cdot I_{OL} \cdot V_{OL} \right] \quad \text{Equation 2}$$

$$T_J = T_A + P_{TOT} \cdot R_{thja} \quad \text{Equation 3}$$

$$f_{CLOCK,MAX} = \frac{1}{C_{PD} \cdot N \cdot V_{CC}^2} \cdot \left[ \frac{T_{J,MAX} - T_A}{R_{thja}} - (I_{CCQ} \cdot V_{CC}) \right] \quad \text{Equation 4}$$

Where $R_{thja}$ is the thermal impedance of the package (junction to ambient) and $T_A$ is the ambient temperature. According to Table 9, the junction temperature can be used to estimate the long-term device reliability. Further, combining equation 1 and equation 2 results in a maximum operating frequency for the MPC961P in a series terminated transmission line system.

**Table 10: Thermal package impedance of the 32ld LQFP**

| Convection, LFPM | $R_{thja}$ (1P2S board), K/W |
|---|---|
| Still air | 80 |
| 100 lfpm | 70 |
| 200 lfpm | 61 |
| 300 lfpm | 57 |
| 400 lfpm | 56 |
| 500 lfpm | 55 |

$T_{J,MAX}$ should be selected according to the MTBF system requirements and Table 9. $R_{thja}$ can be derived from Table 10. The $R_{thja}$ represent data based on 1S2P boards, using 2S2P boards will result in a lower thermal impedance than indicated below.

If the calculated maximum frequency is below 200 MHz, it becomes the upper clock speed limit for the given application conditions. The following two derating charts describe the safe frequency operation range for the MPC961P. The charts were calculated for a maximum tolerable die junction temperature of 110°C, corresponding to an estimated MTBF of 9.1 years, a supply voltage of 3.3V and series terminated transmission line or capacitive loading. Depending on a given set of these operating conditions and the available device convection a decision on the maximum operating frequency can be made. There are no operating frequency limitations if a 2.5V power supply or the system specifications allow for a MTBF of 4 years (corresponding to a max. junction temperature of 120°C.

4

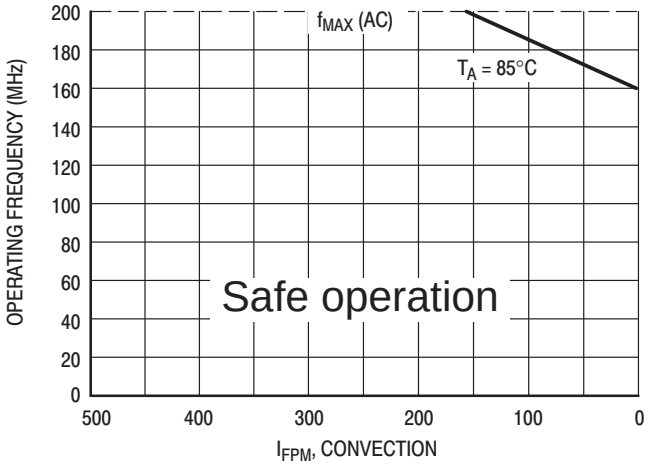



**Figure 9. Maximum MPC961P frequency, $V_{CC}$ = 3.3V, MTBF 9.1 years, driving series terminated transmission lines**

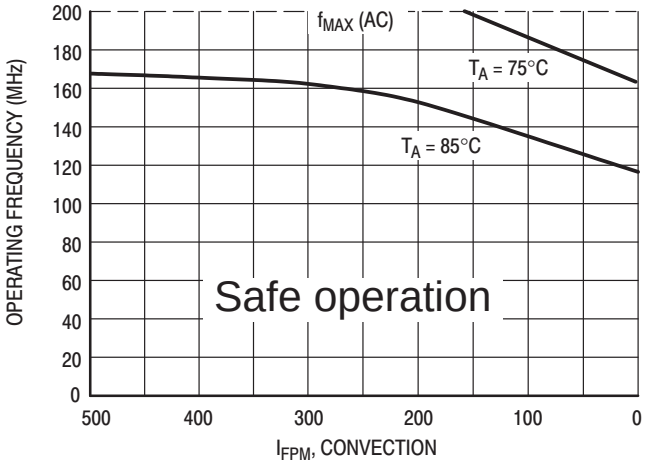



**Figure 10. Maximum MPC961P frequency, $V_{CC}$ = 3.3V, MTBF 9.1 years, 4 pF load per line**

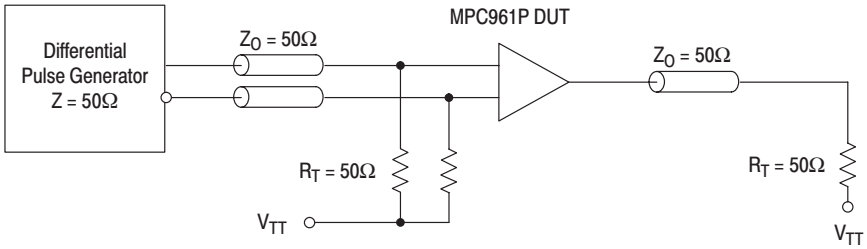



**Figure 11. TCLK MPC961P AC test reference for $V_{cc}$ = 3.3V and $V_{cc}$ = 2.5V**

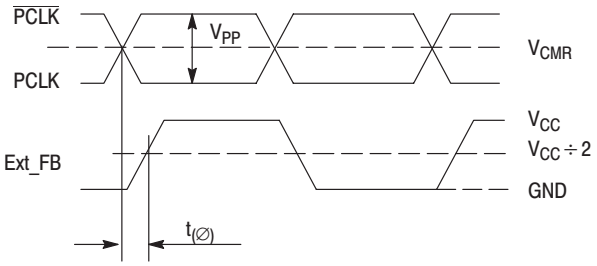



**Figure 12. Propagation delay ($t_{(\varnothing)}$, static phase offset) test reference**

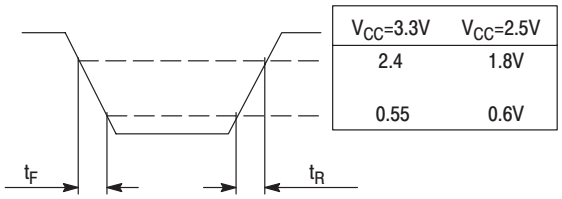
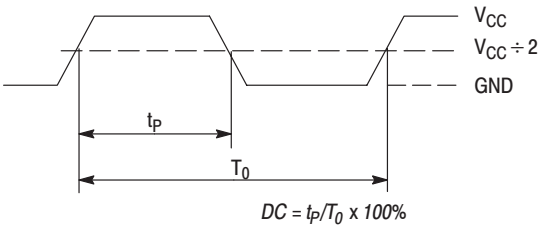
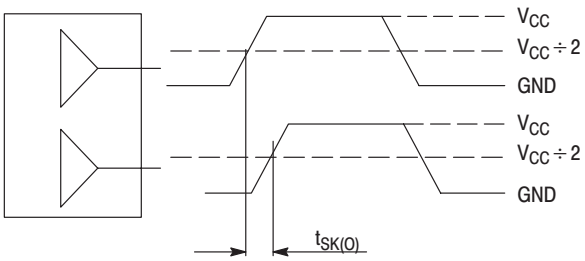



**Figure 13. Output Transition Time Test Reference**



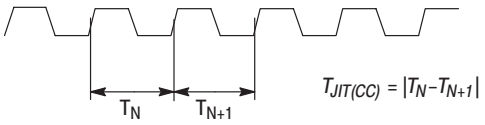

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 14. Output Duty Cycle (DC)**



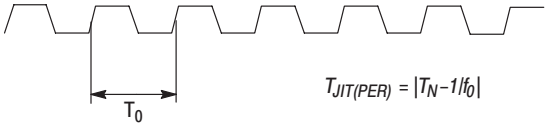

The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 15. Output–to–output Skew $t_{SK(O)}$**



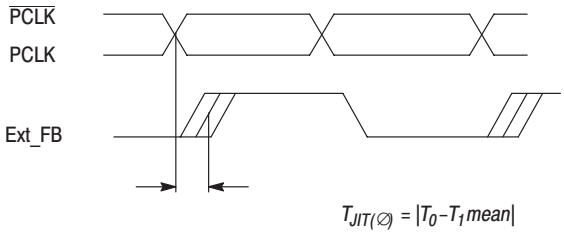

The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

**Figure 16. Cycle–to–cycle Jitter**




The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

**Figure 17. Period Jitter**




The deviation in $t_0$ for a controlled edge with respect to a $t_0$ mean in a random sample of cycles

**Figure 18. I/O Jitter**

**Order Number: MPC9653/D**
**Rev 0, 11/2001**

*Product Preview*

# 3.3V/2.5V 1:8 LVCMOS PLL Clock Generator

**MPC9653**

**LOW VOLTAGE**
**3.3V/2.5V LVCMOS 1:8**
**PLL CLOCK GENERATOR**

**FA SUFFIX**
32 LEAD LQFP PACKAGE
CASE 873A

4

The MPC9653 is a 3.3V or 2.5V compatible, 1:8 PLL based clock generator and zero-delay buffer targeted for high performance low-skew clock distribution in mid-range to high-performance telecom, networking and computing applications. With output frequencies up to 112.5 MHz and output skews less than 150 ps[1] the device meets the needs of the most demanding clock applications.

**Features**

- 1:8 PLL based low-voltage clock generator
- Supports zero-delay operation
- 2.5V or 3.3V power supply
- Generates clock signals up to 112.5 MHz
- Maximum output skew of 150 ps[1]
- Differential LVPECL reference clock input
- External PLL feedback
- Drives up to 16 clock lines
- 32 lead LQFP packaging
- Ambient temperature range 0°C to +70°C
- Pin and function compatible to the MPC953

**Functional Description**

The MPC9653 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9653 requires the connection of the QFB output to the feedback input to close the PLL feedback path (external feedback). With the PLL locked, the output frequency is equal to the reference frequency of the device and VCO_SEL selects the operating frequency range of 25 to 56.25 MHz or 50 to 112.5 MHz. The two available post-PLL dividers selected by VCO_SEL (divide-by-4 or divide-by-8) and the reference clock frequency determine the VCO frequency. Both must be selected to match the VCO frequency range. The internal VCO of the MPC9653 is running at either 4x or 8x of the reference clock frequency.

The MPC9653 has a differential LVPECL reference input along with an external feedback input. The device is ideal for use as a zero delay, low skew fanout buffer. The device performance has been tuned and optimized for zero delay performance.

The PLL_EN and $\overline{\text{BYPASS}}$ controls select the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is bypassing the PLL and routed either to the output dividers or directly to the outputs. The PLL bypass configurations are fully static and the minimum clock frequency specification and all other PLL characteristics do not apply. The outputs can be disabled (high-impedance) and the device reset by asserting the MR/$\overline{\text{OE}}$ pin. Asserting MR/$\overline{\text{OE}}$ also causes the PLL to loose lock due to missing feedback signal presence at FB_IN. Deasserting MR/$\overline{\text{OE}}$ will enable the outputs and close the phase locked loop, enabling the PLL to recover to normal operation.

The MPC9653 is fully 2.5V and 3.3V compatible and requires no external loop filter components. The inputs (except PCLK) accept LVCMOS except signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9653 outputs can drive one or two traces giving the devices an effective fanout of 1:16. The device is packaged in a 7x7 mm$^2$ 32-lead LQFP package.

1. Final specification of this parameter is pending characterization.



**Rev 0**

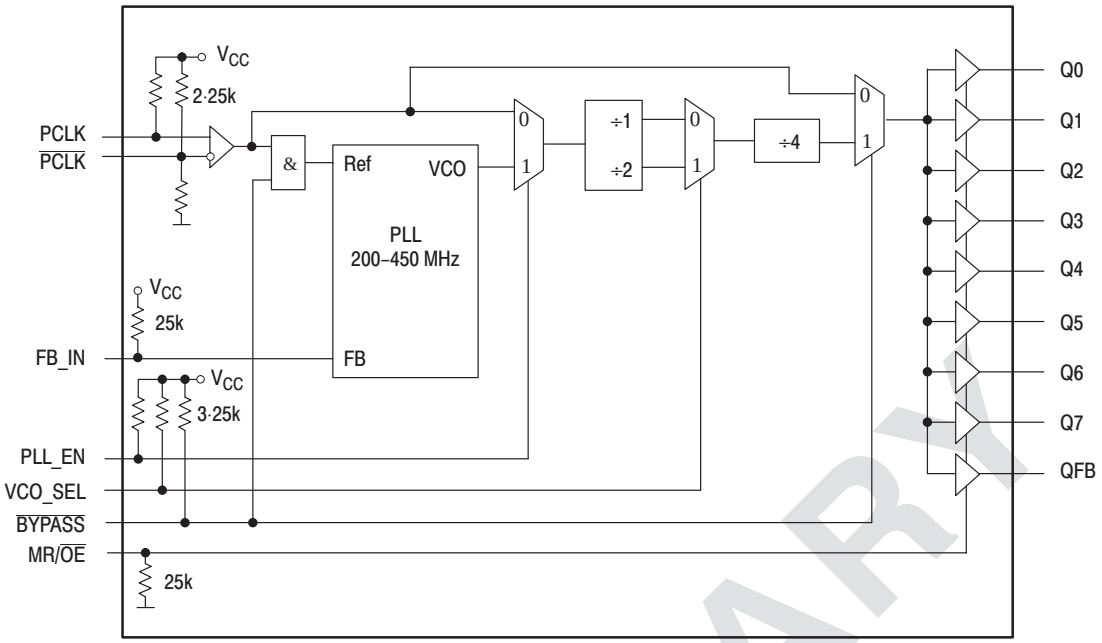



**Figure 1. MPC9653 Logic Diagram**

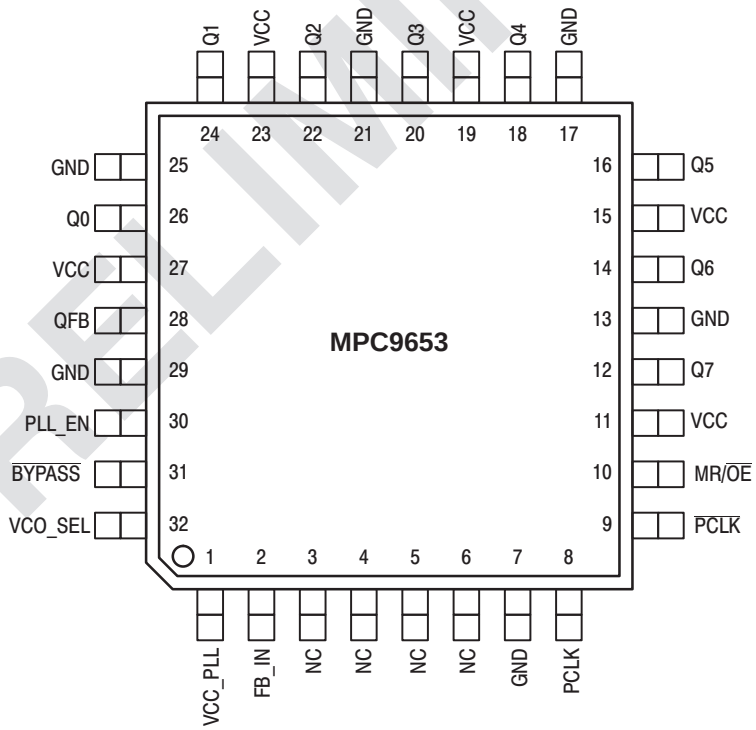



**Figure 2. MPC9653 32–Lead Package Pinout** (Top View)

**Table 1: PIN CONFIGURATION**

| Pin | I/O | Type | Function |
|---|---|---|---|
| PCLK, $\overline{\text{PCLK}}$ | Input | LVPECL | PECL reference clock signal |
| FB_IN | Input | LVCMOS | PLL feedback signal input, connect to QFB |
| VCO_SEL | Input | LVCMOS | Operating frequency range select |
| $\overline{\text{BYPASS}}$ | Input | LVCMOS | PLL and output divider bypass select |
| PLL_EN | Input | LVCMOS | PLL enable/disable |
| MR/$\overline{\text{OE}}$ | Input | LVCMOS | Output enable/disable (high-impedance tristate) and device reset |
| Q0-7 | Output | LVCMOS | Clock outputs |
| QFB | Output | LVCMOS | Clock output for PLL feedback, connect to FB_IN |
| GND | Supply | Ground | Negative power supply (GND) |
| VCC_PLL | Supply | VCC | PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin $V_{CC\_PLL}$. Please see applications section for details. |
| VCC | Supply | VCC | Positive power supply for I/O and core. All VCC pins must be connected to the positive power supply for correct operation |

4

**Table 2: FUNCTION TABLE**

| Control | Default | 0 | 1 |
|---|---|---|---|
| PLL_EN | 1 | Test mode with PLL bypassed. The reference clock (PCLK) is substituted for the internal VCO output. MPC9653 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable. | Selects the VCO output[a] |
| $\overline{\text{BYPASS}}$ | 1 | Test mode with PLL and output dividers bypassed. The reference clock (PCLK) is directly routed to the outputs. MPC9653 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable. | Selects the output dividers. |
| VCO_SEL | 1 | VCO ÷ 1 (High frequency range). $f_{REF} = f_{Q0\text{-}7} = 4 \cdot f_{VCO}$ | VCO ÷ 2 (Low output range). $f_{REF} = f_{Q0\text{-}7} = 8 \cdot f_{VCO}$ |
| MR/$\overline{\text{OE}}$ | 0 | Outputs enabled (active) | Outputs disabled (high-impedance state) and reset of the device. During reset the PLL feedback loop is open. The VCO is tied to its lowest frequency. The MPC9653 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (PCLK). |

a. PLL operation requires BYPASS=1 and PLL_EN=1.

**Table 3: GENERAL SPECIFICATIONS**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output Termination Voltage | | $V_{CC} \div 2$ | | V | |
| MM | ESD Protection (Machine Model) | 200 | | | V | |
| HBM | ESD Protection (Human Body Model) | 2000 | | | V | |
| LU | Latch–Up Immunity | 200 | | | mA | |
| $C_{PD}$ | Power Dissipation Capacitance | | 10 | | pF | Per output |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | Inputs |

**Table 4: ABSOLUTE MAXIMUM RATINGS[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage Temperature | -65 | 125 | °C | |

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 5: DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = 0°C to 70°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | | | 0.8 | V | LVCMOS |
| $V_{PP}$ | Peak-to-peak input voltage (PCLK) | 250 | | | mV | LVPECL |
| $V_{CMR}$[a] | Common Mode Range (PCLK) | 1.0 | | $V_{CC}$-0.6 | V | LVPECL |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$=-24 mA[b] |
| $V_{OL}$ | Output Low Voltage | | | 0.55<br>0.30 | V<br>V | $I_{OL}$= 24 mA<br>$I_{OL}$= 12 mA |
| $Z_{OUT}$ | Output impedance | | 14 - 17 | | Ω | |
| $I_{IN}$ | Input Current[c] | | | ±200 | µA | $V_{IN}$=$V_{CC}$ or GND |
| $I_{CC\_PLL}$ | Maximum PLL Supply Current | | 3.0 | 5.0 | mA | $V_{CC\_PLL}$ Pin |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (DC) specification.

b The MPC9653 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

c Inputs have pull-down resistors affecting the input current.

4

**Table 6: AC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = 0°C to 70°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input reference frequency<br>PLL mode, external feedback<br><br>Input reference frequency in PLL bypass mode[e] | ÷4 feedback[c]<br>÷8 feedback[d] | 50<br>25<br><br>0 | | 112.5<br>61.25<br><br>200 | MHz<br>MHz<br><br>MHz | PLL locked<br>PLL locked |
| $f_{VCO}$ | VCO lock frequency range[f] | | 200 | | 450 | MHz | |
| $f_{MAX}$ | Output Frequency | ÷4 feedback[c]<br>÷8 feedback[d] | 50<br>25 | | 112.5<br>61.25 | MHz<br>MHz | PLL locked<br>PLL locked |
| $V_{PP}$ | Peak-to-peak input voltage (PCLK) | | 500 | | 1000 | mV | LVPECL |
| $V_{CMR}$[g] | Common Mode Range (PCLK) | | 1.2 | | $V_{CC}$-0.9 | V | LVPECL |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | | 60 | % | |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) | PCLK to FB_IN | | ±100 | | ps | PLL locked |
| $t_{PD}$ | Propagation Delay (PLL and divider bypass)<br>(PLL bypass) | PCLK to Q0-7<br>PCLK to Q0-7 | TBD<br>TBD | | TBD<br>TBD | ns<br>ns | |
| $t_{sk(O)}$ | Output-to-output Skew[h] | | | | 150 | ps | |
| $t_{sk(PP)}$ | Device-to-device Skew (in PLL and divider bypass) | | | | 1.5 | ns | |
| DC | Output duty cycle | | 45 | 50 | 55 | % | PLL locked |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.55 to 2.4V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 6 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 6 | ns | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ)[i] | | TBD | | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | TBD | | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1 σ) | | TBD | | ps | |
| BW | PLL closed loop bandwidth[j]<br>PLL mode, external feedback | ÷ 4 feedback[c]<br>÷ 8 feedback[d] | | | TBD<br>TBD | kHz<br>kHz | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | | 10 | ms | |

a All AC characteristics are design targets and subject to change upon device characterization.

b AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.

c ÷4 PLL feedback (high frequency range) requires VCO_SEL=0, PLL_EN=1, $\overline{\text{BYPASS}}$=1 and MR/$\overline{\text{OE}}$=0.

d ÷8 PLL feedback (low frequency range) requires VCO_SEL=1, PLL_EN=1, $\overline{\text{BYPASS}}$=1 and MR/$\overline{\text{OE}}$=0.

e In bypass mode, the MPC9653 divides the input reference clock.

f The input frequency $f_{ref}$ must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$.

g $V_{CMR}$ (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ or $V_{PP}$ impacts static phase offset $t_{(\varnothing)}$.

h See application section for part-to-part skew calculation in PLL zero-delay mode.

i See application section for a jitter calculation for other confidence factors than 1 σ.

j -3 dB point of PLL transfer characteristics.

**Table 7: DC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = 0°C to 70°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | -0.3 | | 0.7 | V | LVCMOS |
| $V_{PP}$ | Peak-to-peak input voltage (PCLK) | 250 | | | mV | LVPECL |
| $V_{CMR}$[a] | Common Mode Range (PCLK) | 1.0 | | $V_{CC}$-0.6 | V | LVPECL |
| $V_{OH}$ | Output High Voltage | 1.8 | | | V | $I_{OH}$=-15 mA[b] |
| $V_{OL}$ | Output Low Voltage | | | 0.6 | V | $I_{OL}$= 15 mA |
| $Z_{OUT}$ | Output impedance | | 17 - 20 | | Ω | |
| $I_{IN}$ | Input Current | | | ±200 | µA | $V_{IN}$=$V_{CC}$ or GND |
| $I_{CC\_PLL}$ | Maximum PLL Supply Current | | 2.0 | 5.0 | mA | $V_{CCA}$ Pin |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (DC) specification.

b The MPC9653 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.

**Table 8: AC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = 0°C to 70°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input reference frequency<br>PLL mode, external feedback<br><br>Input reference frequency in PLL bypass mode | ÷4 feedback[c]<br>÷8 feedback[d] | 50<br>25<br><br>0 | | 100<br>50<br><br>200 | MHz<br>MHz<br><br>MHz | PLL locked<br>PLL locked |
| $f_{VCO}$ | VCO lock frequency range[e] | | 200 | | 400 | MHz | |
| $f_{MAX}$ | Output Frequency | ÷4 feedback[c]<br>÷8 feedback[d] | 50<br>25 | | 100<br>50 | MHz<br>MHz | PLL locked<br>PLL locked |
| $V_{PP}$ | Peak-to-peak input voltage (PCLK) | | 500 | | 1000 | mV | LVPECL |
| $V_{CMR}$[f] | Common Mode Range (PCLK) | | 1.2 | | $V_{CC}$-0.6 | V | LVPECL |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | | 60 | % | |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) | PCLK to FB_IN | | ±100 | | ps | PLL locked |
| $t_{PD}$ | Propagation Delay (PLL and divider bypass)<br>(PLL bypass) | PCLK to Q0-7<br>PCLK to Q0-7 | TBD<br>TBD | | TBD<br>TBD | ns<br>ns | |
| $t_{sk(O)}$ | Output-to-output Skew[g] | | | | 150 | ps | |
| $t_{sk(PP)}$ | Device-to-device Skew (in PLL and divider bypass) | | | | TBD | ns | |
| DC | Output duty cycle | | 45 | 50 | 55 | % | PLL locked |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.6 to 1.8V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 6 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 6 | ns | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ)[h] | | TBD | | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | TBD | | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1 σ) | | TBD | | ps | |
| BW | PLL closed loop bandwidth[i]<br>PLL mode, external feedback | ÷ 4 feedback[c]<br>÷ 8 feedback[d] | | | TBD<br>TBD | kHz<br>kHz | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | | 10 | ms | |

a All AC characteristics are design targets and subject to change upon device characterization.

b AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.

c ÷4 PLL feedback (high frequency range) requires VCO_SEL=0, PLL_EN=1, $\overline{\text{BYPASS}}$=1 and MR/$\overline{\text{OE}}$=0.

d ÷8 PLL feedback (low frequency range) requires VCO_SEL=1, PLL_EN=1, $\overline{\text{BYPASS}}$=1 and MR/$\overline{\text{OE}}$=0.

e The input frequency $f_{ref}$ must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$.

f $V_{CMR}$ (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ or $V_{PP}$ impacts static phase offset $t_{(\varnothing)}$.

g See application section for part-to-part skew calculation in PLL zero-delay mode.

h See application section for a jitter calculation for other confidence factors than 1 σ.

i -3 dB point of PLL transfer characteristics.

## APPLICATIONS INFORMATION

### Programming the MPC9653

The MPC9653 supports output clock frequencies from 25 to 112.5 MHz. Two different feedback divider configurations can be used to achieve the desired frequency operation range. The feedback divider (VCO_SEL) should be used to situate the VCO in the frequency lock range between 200 and 450 (400) MHz for stable and optimal operation. Two operating frequency ranges are supported: 25 to 61.5 MHz and 50 to 112.5 MHz[3]. Table 9 illustrates the configurations supported by the MPC9653. PLL zero-delay is supported if $\overline{BYPASS}$=1, PLL_EN=1 and the input frequency is within the specified PLL reference frequency range.

3. For 2.5V operation, the operating frequency ranges are 25 to 50 MHz and 50 to 100 MHz.

**Table 9: MPC9653 Configurations (QFB connected to FB_IN)**

| $\overline{BYPASS}$ | PLL_EN | VCO_SEL | Operation | Frequency | | |
|---|---|---|---|---|---|---|
| | | | | Ratio | Output range ($f_{Q0-7}$) | VCO |
| 0 | X | X | Test mode: PLL and divider bypass | $f_{Q0-7} = f_{REF}$ | 0-200 MHz | n/a |
| 1 | 0 | 0 | Test mode: PLL bypass | $f_{Q0-7} = f_{REF} \div 4$ | 0-50 MHz | n/a |
| 1 | 0 | 1 | Test mode: PLL bypass | $f_{Q0-7} = f_{REF} \div 8$ | 0-25 MHz | n/a |
| 1 | 1 | 0 | PLL mode (high frequency range) | $f_{Q0-7} = f_{REF}$ | 50 to 112.5 MHz ($V_{CC}$=3.3V)<br>50 to 100 MHz ($V_{CC}$=2.5V) | $f_{VCO} = f_{REF} \cdot 4$ |
| 1 | 1 | 1 | PLL mode (low frequency range) | $f_{Q0-7} = f_{REF}$ | 25 to 61.5 MHz ($V_{CC}$=3.3V)<br>25 to 50 MHz ($V_{CC}$=2.5V) | $f_{VCO} = f_{REF} \cdot 8$ |

4

### Power Supply Filtering

The MPC9653 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the $V_{CCA\_PLL}$ power supply impacts the device characteristics, for instance I/O jitter. The MPC9653 provides separate power supplies for the output buffers ($V_{CC}$) and the phase-locked loop ($V_{CCA\_PLL}$) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the $V_{CC\_PLL}$ pin for the MPC9653. Figure 3 illustrates a typical power supply filter scheme. The MPC9653 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor $R_F$. From the data sheet the $I_{CCA}$ current (the current sourced through the $V_{CC\_PLL}$ pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V ($V_{CC}$=3.3V or $V_{CC}$=2.5V) must be maintained on the $V_{CC\_PLL}$ pin. The resistor $R_F$ shown in Figure 3 "$V_{CC\_PLL}$ Power Supply Filter" must have a resistance of 9-10Ω ($V_{CC}$=2.5V) to meet the voltage drop criteria.

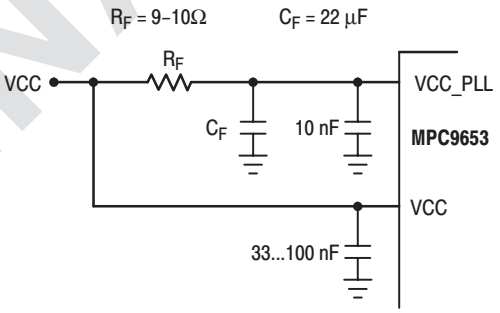



**Figure 3. $V_{CC\_PLL}$ Power Supply Filter**

The minimum values for $R_F$ and the filter capacitor $C_F$ are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3 "$V_{CC\_PLL}$ Power Supply Filter", the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9653 has several de-

sign features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

### Using the MPC9653 in zero–delay applications

Nested clock trees are typical applications for the MPC9653. Designs using the MPC9653 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC9653 clock driver allows for its use as a zero delay buffer. One example configuration is to use a ÷4 output as a feedback to the PLL and configuring all other outputs to a divide-by-4 mode. The propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

### Calculation of part-to-part skew

The MPC9653 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9653 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

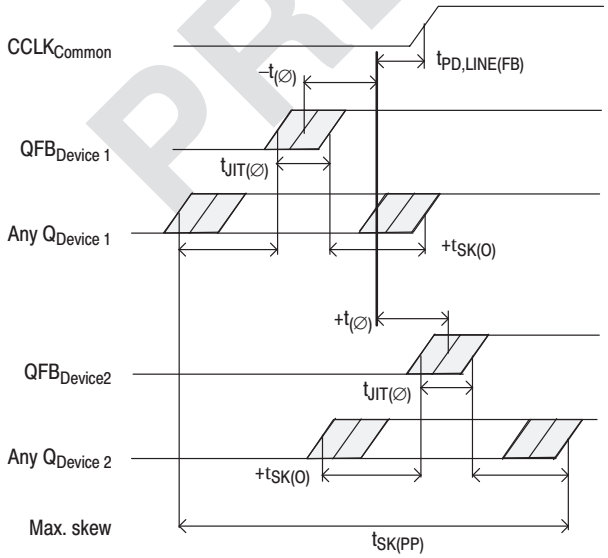



**Figure 4. MPC9653 max. device-to-device skew**

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 10.

**Table 10: Confidence Facter CF**

| CF | Probability of clock edge within the distribution |
|---|---|
| ± 1σ | 0.68268948 |
| ± 2σ | 0.95449988 |
| ± 3σ | 0.99730007 |
| ± 4σ | 0.99993663 |
| ± 5σ | 0.99999943 |
| ± 6σ | 0.99999999 |

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of -295 ps to 295 ps[1] relative to CCLK:

$$t_{SK(PP)} = [–100ps...100ps] + [–150ps...150ps] + [(15ps \cdot –3)...(15ps \cdot 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [–295ps...295ps] + t_{PD,\ LINE(FB)}$$

Due to the frequency dependence of the I/O jitter, Figure 5 “Max. I/O Jitter versus frequency” can be used for a more precise timing performance analysis.

TBD
See MPC961C application section for an example I/O jitter characteristics

**Figure 5. Max. I/O Jitter versus frequency**

### Driving Transmission Lines

The MPC9653 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}$÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9653 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can

drive multiple series terminated lines. Figure 6 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9653 clock driver is effectively doubled due to its capability to drive multiple lines.

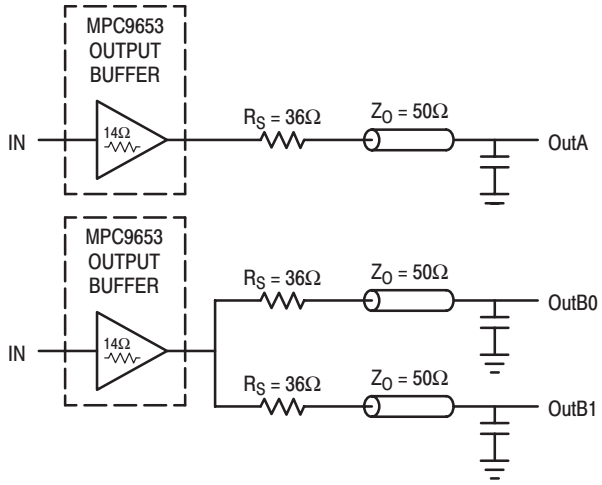



**Figure 6. Single versus Dual Transmission Lines**

The waveform plots in Figure 7 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9653 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9653. The output waveform in Figure 7 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S ( Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\Omega \parallel 50\Omega$$
$$R_S = 36\Omega \parallel 36\Omega$$
$$R_0 = 14\Omega$$
$$V_L = 3.0 ( 25 \div (18+17+25)$$
$$= 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

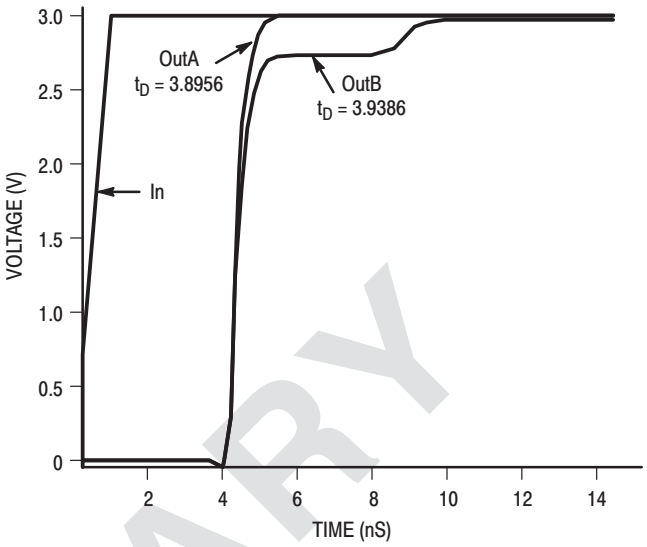
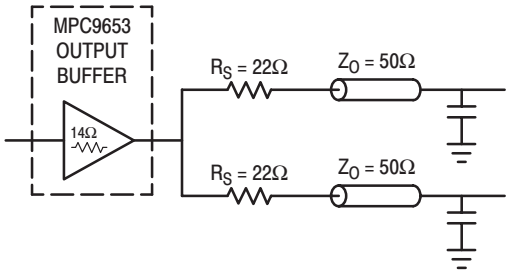



**Figure 7. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 8 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




$14\Omega + 22\Omega \parallel 22\Omega = 50\Omega \parallel 50\Omega$
$25\Omega = 25\Omega$

**Figure 8. Optimized Dual Line Termination**

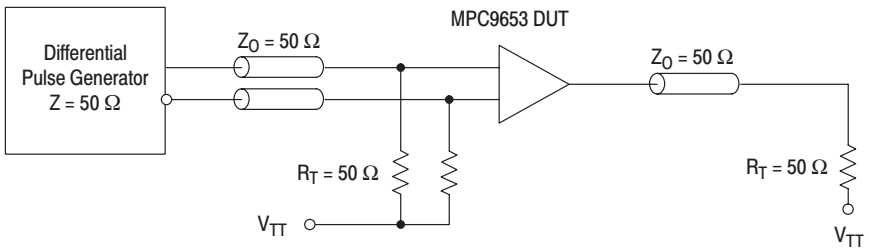
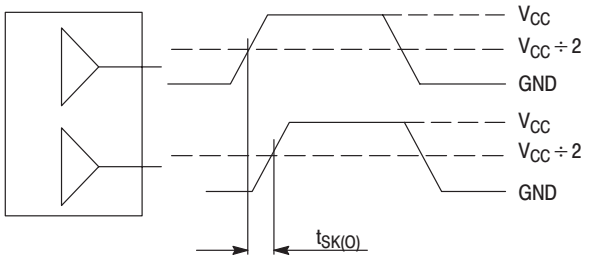



**Figure 9. PCLK MPC9653 AC test reference**




The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 10. Output–to–output Skew $t_{SK(O)}$**

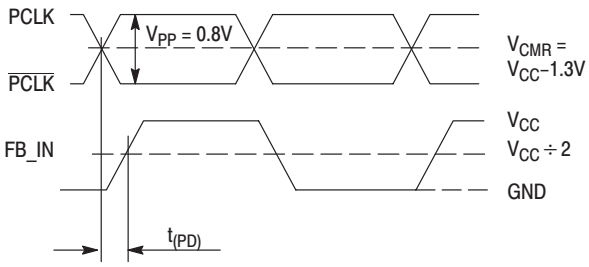
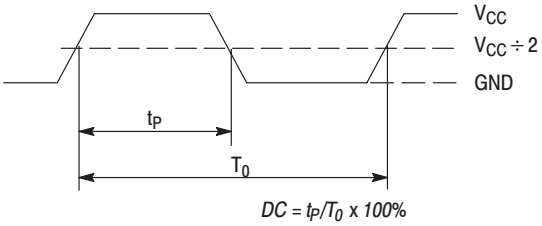
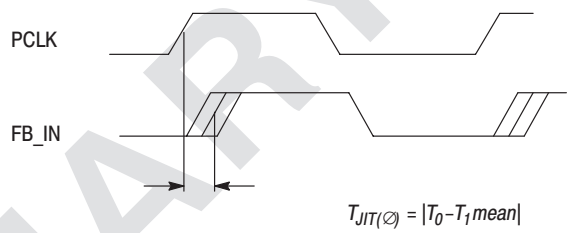



**Figure 11. Propagation delay ($t_{(PD)}$, static phase offset) test reference**



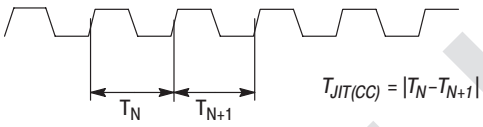

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 12. Output Duty Cycle (DC)**



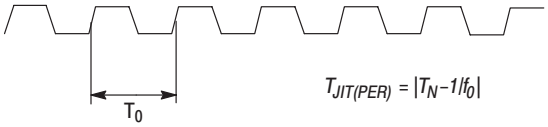

The deviation in $t_0$ for a controlled edge with respect to a $t_0$ mean in a random sample of cycles

**Figure 13. I/O Jitter**




The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

**Figure 14. Cycle–to–cycle Jitter**




The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

**Figure 15. Period Jitter**

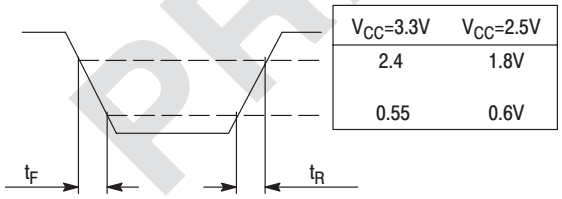



**Figure 16. Output Transition Time Test Reference**

**Order Number: MPC9658/D**
**Rev 0, 11/2001**

*Product Preview*

# 3.3V/2.5V 1:10 LVCMOS PLL Clock Generator

**MPC9658**

**LOW VOLTAGE**
**3.3V/2.5V LVCMOS 1:10**
**PLL CLOCK GENERATOR**

**FA SUFFIX**
32 LEAD LQFP PACKAGE
CASE 873A

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The MPC9658 is a 3.3V or 2.5V compatible, 1:10 PLL based clock generator and zero-delay buffer targeted for high performance low-skew clock distribution in mid-range to high-performance telecom, networking and computing applications. With output frequencies up to 200 MHz and output skews less than 150 ps[1] the device meets the needs of the most demanding clock applications. The MPC9658 is specified for the extended temperature range of –40°C to +85°C.

**Features**

- 1:10 PLL based low-voltage clock generator
- Supports zero-delay operation
- 2.5V or 3.3V power supply
- Generates clock signals up to 200 MHz
- Maximum output skew of 150 ps[1]
- Differential LVPECL reference clock input
- External PLL feedback
- Drives up to 20 clock lines
- 32 lead LQFP packaging
- Ambient temperature range –40°C to +85°C
- Pin and function compatible to the MPC958

**Functional Description**

The MPC9658 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9658 requires the connection of the QFB output to the feedback input to close the PLL feedback path (external feedback). With the PLL locked, the output frequency is equal to the reference frequency of the device and VCO_SEL selects the operating frequency range of 50 to 100 MHz or 100 to 200 MHz. The two available post-PLL dividers selected by VCO_SEL (divide-by-2 or divide-by-4) and the reference clock frequency determine the VCO frequency. Both must be selected to match the VCO frequency range. The internal VCO of the MPC9658 is running at either 2x or 4x of the reference clock frequency.

The MPC9658 has a differential LVPECL reference input along with an external feedback input. The MPC9658 is ideal for use as a zero delay, low skew fanout buffer. The device performance has been tuned and optimized for zero delay performance.

The PLL_EN and $\overline{\text{BYPASS}}$ controls select the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is bypassing the PLL and routed either to the output dividers or directly to the outputs. The PLL bypass configurations are fully static and the minimum clock frequency specification and all other PLL characteristics do not apply. The outputs can be disabled (high-impedance) and the device reset by asserting the MR/$\overline{\text{OE}}$ pin. Asserting MR/$\overline{\text{OE}}$ also causes the PLL to loose lock due to missing feedback signal presence at FB_IN. Deasserting MR/$\overline{\text{OE}}$ will enable the outputs and close the phase locked loop, enabling the PLL to recover to normal operation.

The MPC9658 is fully 2.5V and 3.3V compatible and requires no external loop filter components. The inputs (except PCLK) accept LVCMOS except signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9658 outputs can drive one or two traces giving the devices an effective fanout of 1:16. The device is packaged in a 7x7 $mm^2$ 32-lead LQFP package.

1. Final specification of this parameter is pending characterization.



**Rev 0**

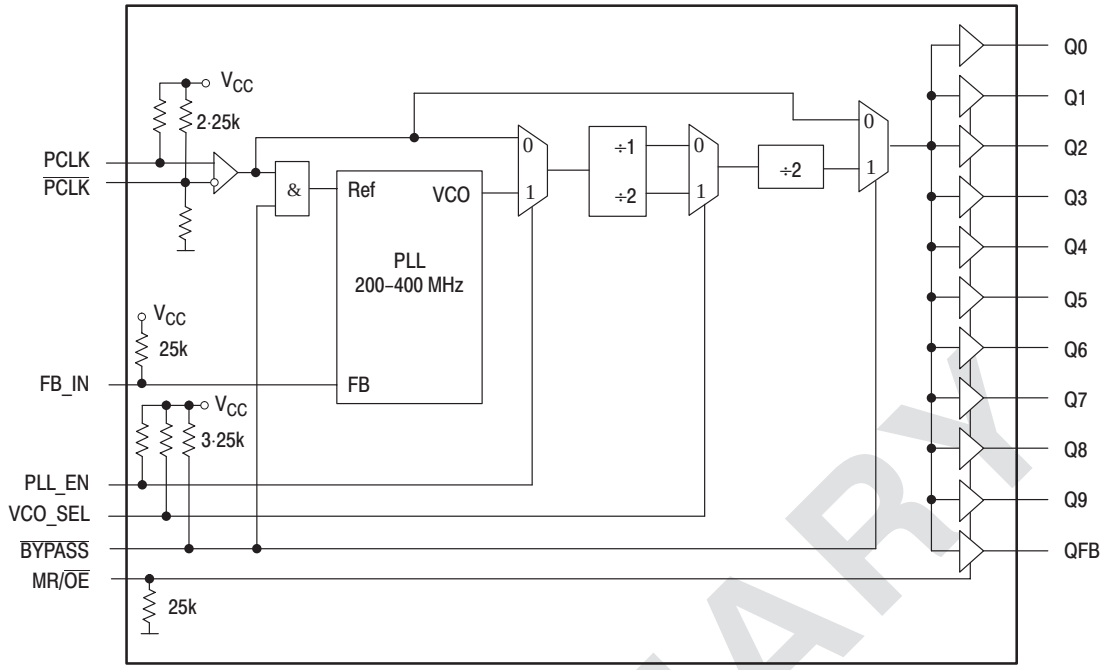


**Figure 1. MPC9658 Logic Diagram**

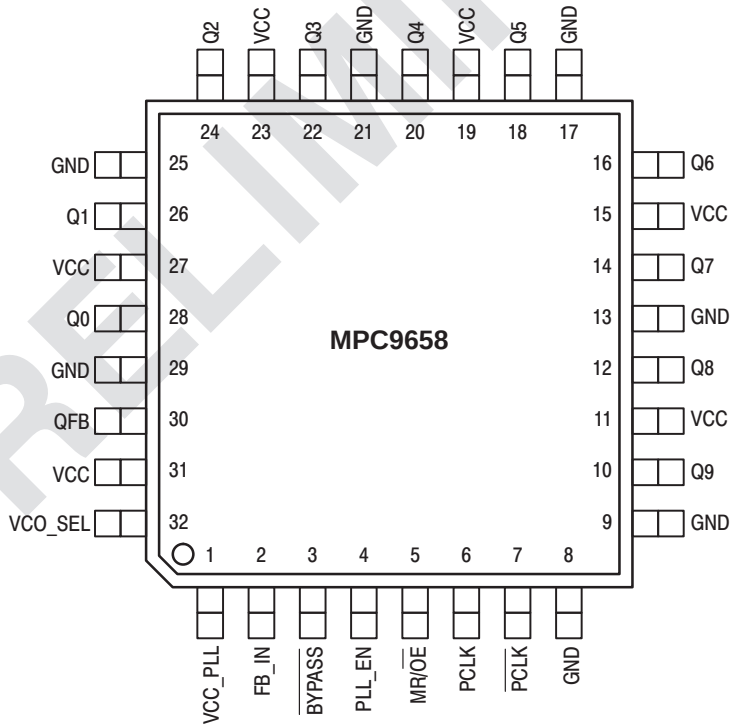


**Figure 2. MPC9658 32–Lead Package Pinout** (Top View)

**Table 1: PIN CONFIGURATION**

| Pin | I/O | Type | Function |
|---|---|---|---|
| PCLK, $\overline{\text{PCLK}}$ | Input | LVPECL | PECL reference clock signal |
| FB_IN | Input | LVCMOS | PLL feedback signal input, connect to QFB |
| VCO_SEL | Input | LVCMOS | Operating frequency range select |
| $\overline{\text{BYPASS}}$ | Input | LVCMOS | PLL and output divider bypass select |
| PLL_EN | Input | LVCMOS | PLL enable/disable |
| MR/$\overline{\text{OE}}$ | Input | LVCMOS | Output enable/disable (high-impedance tristate) and device reset |
| Q0-9 | Output | LVCMOS | Clock outputs |
| QFB | Output | LVCMOS | Clock output for PLL feedback, connect to FB_IN |
| GND | Supply | Ground | Negative power supply (GND) |
| VCC_PLL | Supply | VCC | PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin $V_{CC\_PLL}$. Please see applications section for details. |
| VCC | Supply | VCC | Positive power supply for I/O and core. All VCC pins must be connected to the positive power supply for correct operation |

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**Table 2: FUNCTION TABLE**

| Control | Default | 0 | 1 |
|---|---|---|---|
| PLL_EN | 1 | Test mode with PLL bypassed. The reference clock (PCLK) is substituted for the internal VCO output. MPC9658 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable. | Selects the VCO output[a] |
| $\overline{\text{BYPASS}}$ | 1 | Test mode with PLL and output dividers bypassed. The reference clock (PCLK) is directly routed to the outputs. MPC9658 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable. | Selects the output dividers. |
| VCO_SEL | 1 | VCO ÷ 1 (High frequency range). $f_{REF} = f_{Q0-9} = 2 \cdot f_{VCO}$ | VCO ÷ 2 (Low output range). $f_{REF} = f_{Q0-9} = 4 \cdot f_{VCO}$ |
| MR/$\overline{\text{OE}}$ | 0 | Outputs enabled (active) | Outputs disabled (high-impedance state) and reset of the device. During reset the PLL feedback loop is open. The VCO is tied to its lowest frequency. The MPC9658 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (PCLK). |

a. PLL operation requires BYPASS=1 and PLL_EN=1.

**Table 3: GENERAL SPECIFICATIONS**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output Termination Voltage | | $V_{CC} \div 2$ | | V | |
| MM | ESD Protection (Machine Model) | 200 | | | V | |
| HBM | ESD Protection (Human Body Model) | 2000 | | | V | |
| LU | Latch–Up Immunity | 200 | | | mA | |
| $C_{PD}$ | Power Dissipation Capacitance | | 10 | | pF | Per output |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | Inputs |

**Table 4: ABSOLUTE MAXIMUM RATINGS[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage Temperature | -65 | 125 | °C | |

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 5: DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40°C to 85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | | | 0.8 | V | LVCMOS |
| $V_{PP}$ | Peak-to-peak input voltage (PCLK) | 250 | | | mV | LVPECL |
| $V_{CMR}$[a] | Common Mode Range (PCLK) | 1.0 | | $V_{CC}$-0.6 | V | LVPECL |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$=-24 mA[b] |
| $V_{OL}$ | Output Low Voltage | | | 0.55<br>0.30 | V<br>V | $I_{OL}$= 24 mA<br>$I_{OL}$= 12 mA |
| $Z_{OUT}$ | Output impedance | | 14 - 17 | | Ω | |
| $I_{IN}$ | Input Current[c] | | | ±200 | µA | $V_{IN}$=$V_{CC}$ or GND |
| $I_{CC\_PLL}$ | Maximum PLL Supply Current | | 3.0 | 5.0 | mA | $V_{CC\_PLL}$ Pin |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (DC) specification.
b The MPC9658 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.
c Inputs have pull-down resistors affecting the input current.

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**Table 6: AC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40°C to 85°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input reference frequency<br>PLL mode, external feedback<br><br>Input reference frequency in PLL bypass mode[e] | ÷2 feedback[c]<br>÷4 feedback[d] | 100<br>50<br><br>0 | | 200<br>100<br><br>200 | MHz<br>MHz<br><br>MHz | PLL locked<br>PLL locked |
| $f_{VCO}$ | VCO lock frequency range[f] | | 200 | | 400 | MHz | |
| $f_{MAX}$ | Output Frequency | ÷2 feedback[c]<br>÷4 feedback[d] | 100<br>50 | | 200<br>100 | MHz<br>MHz | PLL locked<br>PLL locked |
| $V_{PP}$ | Peak-to-peak input voltage (PCLK) | | 500 | | 1000 | mV | LVPECL |
| $V_{CMR}$[g] | Common Mode Range (PCLK) | | 1.2 | | $V_{CC}$-0.9 | V | LVPECL |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | | 60 | % | |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) | PCLK to FB_IN | | ±100 | | ps | PLL locked |
| $t_{PD}$ | Propagation Delay (PLL and divider bypass)<br>(PLL bypass) | PCLK to Q0-9<br>PCLK to Q0-9 | TBD<br>TBD | | TBD<br>TBD | ns<br>ns | |
| $t_{sk(O)}$ | Output-to-output Skew[h] | | | | 150 | ps | |
| DC | Output duty cycle | | 45 | 50 | 55 | % | PLL locked |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.55 to 2.4V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 6 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 6 | ns | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ)[i] | | TBD | | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | TBD | | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1 σ) | | TBD | | ps | |
| BW | PLL closed loop bandwidth[j] | ÷ 2 feedback[c]<br>÷ 4 feedback[d] | | | TBD<br>TBD | kHz<br>kHz | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | | 10 | ms | |

a All AC characteristics are design targets and subject to change upon device characterization.
b AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
c ÷2 PLL feedback (high frequency range) requires VCO_SEL=0, PLL_EN=1, $\overline{\text{BYPASS}}$=1 and MR/$\overline{\text{OE}}$=0.
d ÷4 PLL feedback (low frequency range) requires VCO_SEL=1, PLL_EN=1, $\overline{\text{BYPASS}}$=1 and MR/$\overline{\text{OE}}$=0.
e In bypass mode, the MPC9658 divides the input reference clock.
f The input frequency $f_{ref}$ must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$.
g $V_{CMR}$ (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ or $V_{PP}$ impacts static phase offset $t_{(\varnothing)}$.
h See application section for part-to-part skew calculation in PLL zero-delay mode.
i See application section for a jitter calculation for other confidence factors than 1 σ.
j -3 dB point of PLL transfer characteristics.

**Table 7: DC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40°C to 85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | -0.3 | | 0.7 | V | LVCMOS |
| $V_{PP}$ | Peak-to-peak input voltage (PCLK) | 250 | | | mV | LVPECL |
| $V_{CMR}$[a] | Common Mode Range (PCLK) | 1.0 | | $V_{CC}$-0.6 | V | LVPECL |
| $V_{OH}$ | Output High Voltage | 1.8 | | | V | $I_{OH}$=-15 mA[b] |
| $V_{OL}$ | Output Low Voltage | | | 0.6 | V | $I_{OL}$= 15 mA |
| $Z_{OUT}$ | Output impedance | | 17 - 20 | | Ω | |
| $I_{IN}$ | Input Current | | | ±200 | µA | $V_{IN}$=$V_{CC}$ or GND |
| $I_{CC\_PLL}$ | Maximum PLL Supply Current | | 2.0 | 5.0 | mA | $V_{CCA}$ Pin |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (DC) specification.

b The MPC9658 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.

**Table 8: AC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40°C to 85°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input reference frequency<br>PLL mode, external feedback<br><br>Input reference frequency in PLL bypass mode | ÷2 feedback[c]<br>÷4 feedback[d] | 100<br>50<br><br>0 | | 200<br>100<br><br>200 | MHz<br>MHz<br><br>MHz | PLL locked<br>PLL locked |
| $f_{VCO}$ | VCO lock frequency range[e] | | 200 | | 400 | MHz | |
| $f_{MAX}$ | Output Frequency | ÷2 feedback[c]<br>÷4 feedback[d] | 100<br>50 | | 200<br>100 | MHz<br>MHz | PLL locked<br>PLL locked |
| $V_{PP}$ | Peak-to-peak input voltage (PCLK) | | 500 | | 1000 | mV | LVPECL |
| $V_{CMR}$[f] | Common Mode Range (PCLK) | | 1.2 | | $V_{CC}$-0.6 | V | LVPECL |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | | 60 | % | |
| $t_{(\varnothing)}$ | Propagation Delay (static phase offset) | PCLK to FB_IN | | ±100 | | ps | PLL locked |
| $t_{PD}$ | Propagation Delay (PLL and divider bypass)<br>(PLL bypass) | PCLK to Q0-9<br>PCLK to Q0-9 | TBD<br>TBD | | TBD<br>TBD | ns<br>ns | |
| $t_{sk(O)}$ | Output-to-output Skew[g] | | | | 150 | ps | |
| DC | Output duty cycle | | 45 | 50 | 55 | % | PLL locked |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.6 to 1.8V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 6 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 6 | ns | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ)[h] | | TBD | | ps | |
| $t_{JIT(PER)}$ | Period Jitter | RMS (1 σ) | | TBD | | ps | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter | RMS (1 σ) | | TBD | | ps | |
| BW | PLL closed loop bandwidth[i] | ÷ 2 feedback[c]<br>÷ 4 feedback[d] | | | TBD<br>TBD | kHz<br>kHz | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | | 10 | ms | |

a All AC characteristics are design targets and subject to change upon device characterization.

b AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.

c ÷2 PLL feedback (high frequency range) requires VCO_SEL=0, PLL_EN=1, $\overline{\text{BYPASS}}$=1 and MR/$\overline{\text{OE}}$=0.

d ÷4 PLL feedback (low frequency range) requires VCO_SEL=1, PLL_EN=1, $\overline{\text{BYPASS}}$=1 and MR/$\overline{\text{OE}}$=0.

e The input frequency $f_{ref}$ must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$.

f $V_{CMR}$ (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ or $V_{PP}$ impacts static phase offset $t_{(\varnothing)}$.

g See application section for part-to-part skew calculation in PLL zero-delay mode.

h See application section for a jitter calculation for other confidence factors than 1 σ.

i -3 dB point of PLL transfer characteristics.

## APPLICATIONS INFORMATION

### Programming the MPC9658

The MPC9658 supports output clock frequencies from 50 to 200 MHz. Two different feedback divider configurations can be used to achieve the desired frequency operation range. The feedback divider (VCO_SEL) should be used to situate the VCO in the frequency lock range between 200 and 400 MHz for stable and optimal operation. Two operating frequency ranges are supported: 50 to 100 MHz and 100 to 200 MHz. Table 9 illustrates the configurations supported by the MPC9658. PLL zero-delay is supported if $\overline{BYPASS}$=1, PLL_EN=1 and the input frequency is within the specified PLL reference frequency range.

**Table 9: MPC9658 Configurations (QFB connected to FB_IN)**

| $\overline{BYPASS}$ | PLL_EN | VCO_SEL | Operation | Frequency | | |
|---|---|---|---|---|---|---|
| | | | | Ratio | Output range ($f_{Q0-9}$) | VCO |
| 0 | X | X | Test mode: PLL and divider bypass | $f_{Q0-9} = f_{REF}$ | 0-200 MHz | n/a |
| 1 | 0 | 0 | Test mode: PLL bypass | $f_{Q0-9} = f_{REF} \div 2$ | 0-100 MHz | n/a |
| 1 | 0 | 1 | Test mode: PLL bypass | $f_{Q0-9} = f_{REF} \div 4$ | 0-50 MHz | n/a |
| 1 | 1 | 0 | PLL mode (high frequency range) | $f_{Q0-9} = f_{REF}$ | 50 to 100 MHz | $f_{VCO} = f_{REF} \cdot 4$ |
| 1 | 1 | 1 | PLL mode (low frequency range) | $f_{Q0-9} = f_{REF}$ | 100 to 200 MHz | $f_{VCO} = f_{REF} \cdot 2$ |

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### Power Supply Filtering

The MPC9658 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the $V_{CCA\_PLL}$ power supply impacts the device characteristics, for instance I/O jitter. The MPC9658 provides separate power supplies for the output buffers ($V_{CC}$) and the phase-locked loop ($V_{CCA\_PLL}$) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the $V_{CC\_PLL}$ pin for the MPC9658. Figure 3 illustrates a typical power supply filter scheme. The MPC9658 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor $R_F$. From the data sheet the $I_{CCA}$ current (the current sourced through the $V_{CC\_PLL}$ pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V ($V_{CC}$=3.3V or $V_{CC}$=2.5V) must be maintained on the $V_{CC\_PLL}$ pin. The resistor $R_F$ shown in Figure 3 "$V_{CC\_PLL}$ Power Supply Filter" must have a resistance of 9-10Ω ($V_{CC}$=2.5V) to meet the voltage drop criteria.

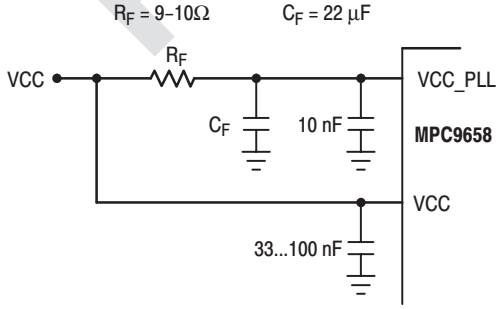



**Figure 3. $V_{CC\_PLL}$ Power Supply Filter**

The minimum values for $R_F$ and the filter capacitor $C_F$ are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3 "$V_{CC\_PLL}$ Power Supply Filter", the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9658 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

### Using the MPC9658 in zero–delay applications

Nested clock trees are typical applications for the MPC9658. Designs using the MPC9658 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC9658 clock driver allows for its use as a zero delay buffer. One example configuration is to use a ÷4 output as a feedback to the PLL and configuring all other outputs to a divide-by-4 mode. The propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

### Calculation of part-to-part skew

The MPC9658 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9658 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

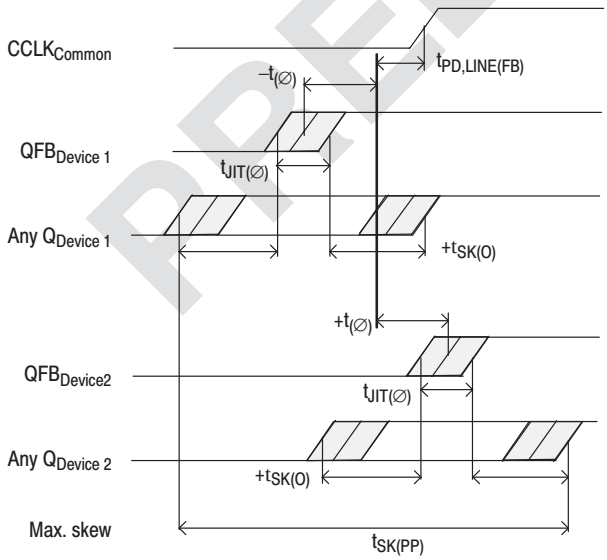



**Figure 4. MPC9658 max. device-to-device skew**

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 10.

**Table 10: Confidence Facter CF**

| CF | Probability of clock edge within the distribution |
|---|---|
| ± 1σ | 0.68268948 |
| ± 2σ | 0.95449988 |
| ± 3σ | 0.99730007 |
| ± 4σ | 0.99993663 |
| ± 5σ | 0.99999943 |
| ± 6σ | 0.99999999 |

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of -295 ps to 295 ps[1] relative to CCLK:

$$t_{SK(PP)} = [–100ps...100ps] + [–150ps...150ps] + [(15ps \cdot –3)...(15ps \cdot 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [–295ps...295ps] + t_{PD,\ LINE(FB)}$$

Due to the frequency dependence of the I/O jitter, Figure 5 “Max. I/O Jitter versus frequency” can be used for a more precise timing performance analysis.

TBD
See MPC961C application section for an example I/O jitter characteristics

**Figure 5. Max. I/O Jitter versus frequency**

### Driving Transmission Lines

The MPC9658 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}$÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9658 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can

drive multiple series terminated lines. Figure 6 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9658 clock driver is effectively doubled due to its capability to drive multiple lines.

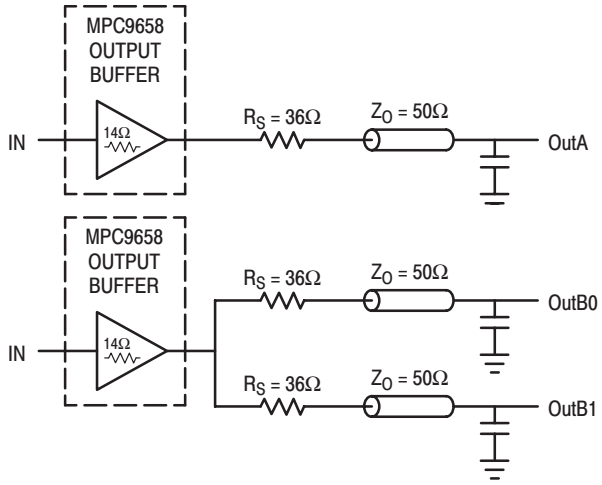



**Figure 6. Single versus Dual Transmission Lines**

The waveform plots in Figure 7 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9658 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9658. The output waveform in Figure 7 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S ( Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\Omega \parallel 50\Omega$$
$$R_S = 36\Omega \parallel 36\Omega$$
$$R_0 = 14\Omega$$
$$V_L = 3.0 ( 25 \div (18+17+25)$$
$$= 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

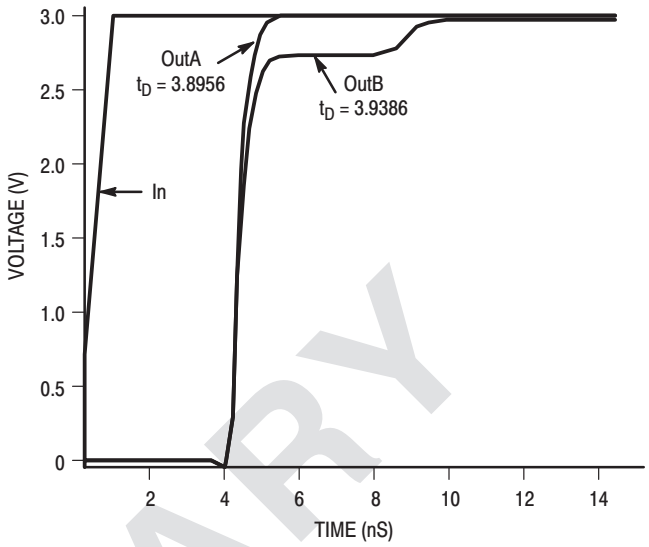
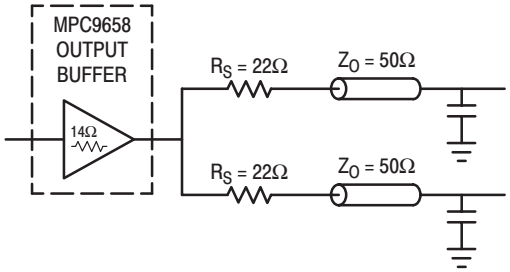



**Figure 7. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 8 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




$14\Omega + 22\Omega \parallel 22\Omega = 50\Omega \parallel 50\Omega$
$25\Omega = 25\Omega$

**Figure 8. Optimized Dual Line Termination**

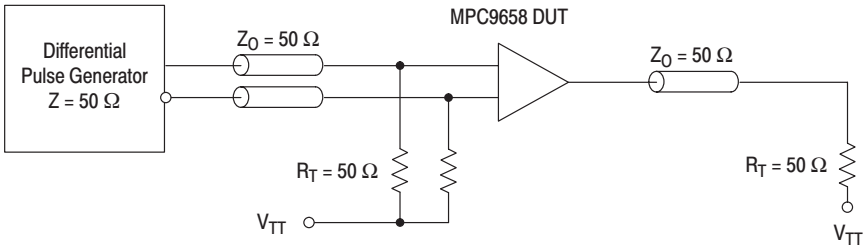
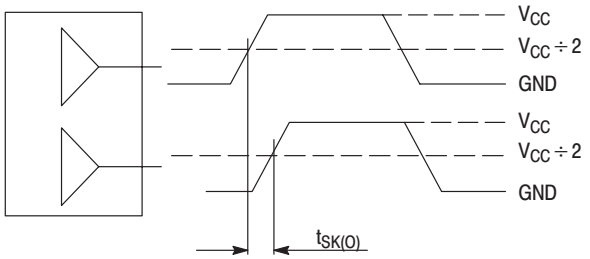



**Figure 9. PCLK MPC9658 AC test reference**




The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 10. Output–to–output Skew $t_{SK(O)}$**

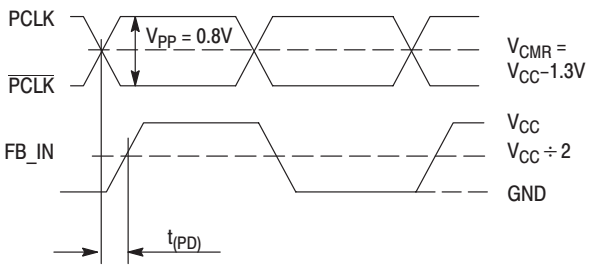
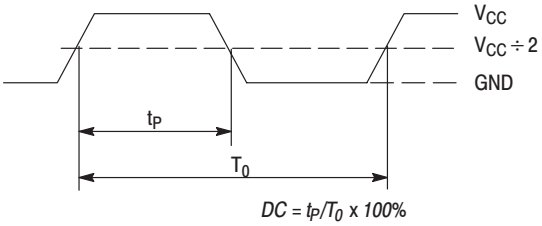
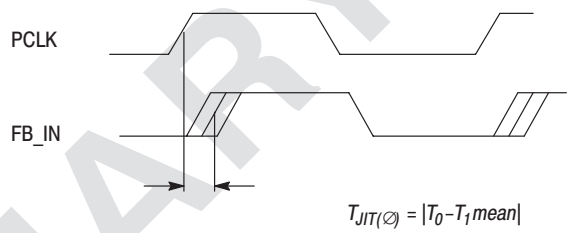



**Figure 11. Propagation delay ($t_{(PD)}$, static phase offset) test reference**



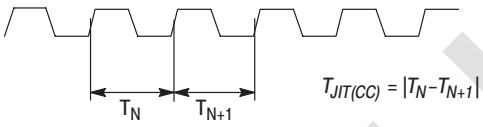

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 12. Output Duty Cycle (DC)**



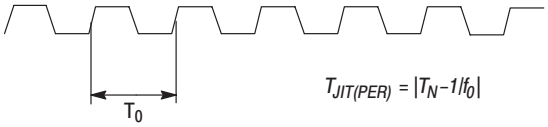

The deviation in $t_0$ for a controlled edge with respect to a $t_0$ mean in a random sample of cycles

**Figure 13. I/O Jitter**




The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

**Figure 14. Cycle–to–cycle Jitter**




The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

**Figure 15. Period Jitter**

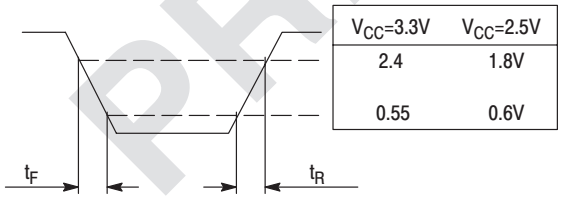



**Figure 16. Output Transition Time Test Reference**

# Chapter Five
# LVCMOS Fanout Buffer Data Sheets

**LVCMOS Fanout Buffer Device Index**

# 1:6 PCI Clock Generator/ Fanout Buffer

**MPC905**

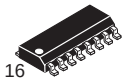
**1:6 PCI CLOCK GENERATOR/ FANOUT BUFFER**

The MPC905 is a six output clock generation device targeted to provide the clocks required in a 3.3V or 5.0V PCI environment. The device operates from a 3.3V supply and can interface to either a TTL input or an external crystal. The inputs to the device can be driven with 5.0V when the $V_{CC}$ is at 3.3V. The outputs of the MPC905 meet all of the specifications of the PCI standard.

- Six Low Skew Outputs
- Synchronous Output Enables for Power Management
- Low Voltage Operation
- XTAL Oscillator Interface
- 16-Lead SOIC Package
- 5.0V Tolerant Enable Inputs

The MPC905 device is targeted for PCI bus or processor bus environments with up to 12 clock loads. Each of the six outputs on the MPC905 can drive two series terminated 50Ω transmission lines. This capability effectively makes the MPC905 a 1:12 fanout buffer.

The MPC905 offers two synchronous enable inputs to allow users flexibility in developing power management features for their designs. Both enable signals are active HIGH inputs. A logic '0' on the Enable1 will pull outputs 0 to 4 into the logic '0' state. A logic '1' on the Enable1 input will result in outputs 0 to 4 to be toggling. A logic '0' on Enable2 will cause output BLK5 to a logic '0' state, whereas a logic '1' on Enable2 will cause output BLK5 to toggle. The oscillator remains on.




**D SUFFIX**
PLASTIC SOIC PACKAGE
CASE 751B-05

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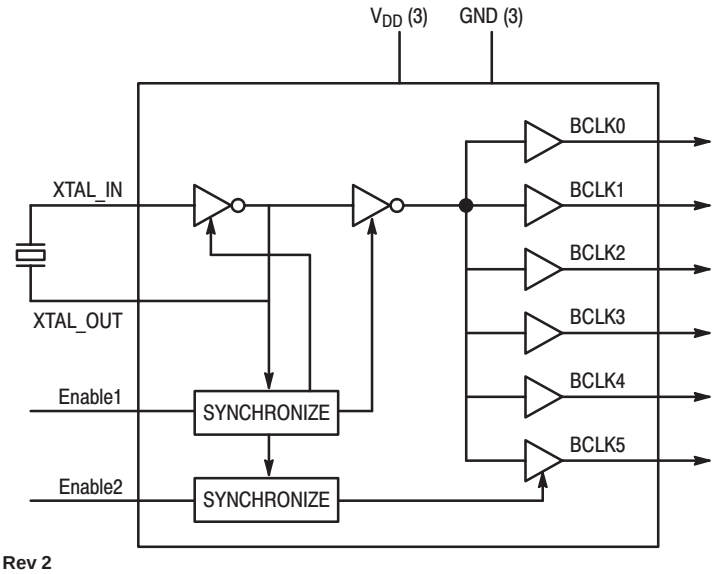
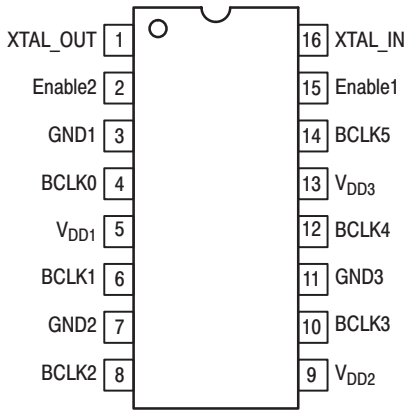
The Enable2 input can be used to disable any high power device for system power savings during periods of inactivity. Both enable inputs are synchronized internal to the chip so that the output disabling will happen only when the outputs are already LOW. This feature guarantees no runt pulses will be generated during enabling and disabling.




Rev 2

**Pinout: 16-Lead Plastic Package** (Top View)



## PIN CONFIGURATIONS

| Pin | I/O | Type | Function |
|---|---|---|---|
| XTAL_IN, XTAL_OUT | Input | Analog | Crystal Oscillator Terminals |
| Enable1, Enable2 | Input | LVCMOS | Output Enable |
| BCLK0 – BCLK5 | Output | LVCMOS | Clock Outputs |
| $V_{DD}$ | | Supply | Positive Power Supply |
| GND | | Supply | Negative Power Supply |

## FUNCTION TABLE

| ENABLE1 | ENABLE2 | Outputs 0 to 4 | Output 5 | OSC (On/Off) |
|---|---|---|---|---|
| 0 | 0 | Low | Low | ON |
| 0 | 1 | Low | Toggling | ON |
| 1 | 0 | Toggling | Low | ON |
| 1 | 1 | Toggling | Toggling | ON |

## ABSOLUTE MAXIMUM RATINGS*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | –0.5 | 4.6 | V |
| $V_{IN}$ | Input Voltage | –0.5 | $V_{CC}$ + 0.5 | V |
| $T_{oper}$ | Operating Temperature Range | 0 | +70 | °C |
| $T_{stg}$ | Storage Temperature Range | –65 | +150 | °C |
| $T_{sol}$ | Soldering Temperature Range (10 Sec) | | +260 | °C |
| $T_j$ | Junction Temperature Range | | +125 | °C |
| ESD | Static Discharge Voltage | 1500 | | V |
| $I_{Latch}$ | Latch Up Current | 50 | | mA |

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_A$ | Ambient Temperature Range | 0 | 70 | °C |
| $V_{CC}$ | Positive Supply Voltage (Functional Range) | 3.0 | 3.6 | V |
| $t_{DC}$in | $T_{high}$ (at XTAL_IN Input)<br>$T_{low}$ (at XTAL_IN Input) | 0.44T[1]<br>0.44T[1] | 0.56T[1]<br>0.56T[1] | T = Period |

1. When using External Source for reference, requirement to meet PCI clock duty cycle requirement on the output.

## DC CHARACTERISTICS ($T_A$ = 0–70°C; $V_{DD}$ = 3.3V ±0.3V)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | 2.0 | | 5.5[2] | V | |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.8 | V | |
| $V_{OH}$ | High Level Output Voltage | | 2.4 | | | V | $I_{OH}$ = –36mA[1] |
| $V_{OL}$ | Low Level Output Voltage | | | | 0.4 | V | $I_{OL}$ = 36mA[1] |
| $I_{IH}$ | Input High Current | | | | 2.5[2] | µA | |
| $I_{IL}$ | Input Low Current | | | | 2.5 | µA | |
| $I_{CC}$ | Power Supply Current | DC<br>33MHz<br>66MHz | | 20<br>37<br>78 | <br>45<br>95 | µA<br>mA<br>mA | |
| $C_{IN}$ | Input Capacitance | XTAL_IN<br>Others | | | 9.0<br>4.5 | pF | |

1. The MPC905 can drive 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to $V_{TT}$ = $V_{CC}$/2. Alternately, the device drives up to two 50Ω series terminated transmission lines per output.
2. XTAL_IN input will sink up to 10mA when driven to 5.5V. There are no reliability concerns associated with the condition. Note that the Enable1 input must be a logic HIGH. Do not take the Enable1 input to a logic LOW with >$V_{CC}$ volts on the XTAL_IN input.

**AC CHARACTERISTICS** ($T_A$ = 0–70°C; $V_{DD}$ = 3.3V ±0.3V)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $F_{max}$ | Maximum Operating Frequency | Using External Crystal<br>Using External Clock Source | –<br>DC | | 50<br>100 | MHz | |
| $t_{pw}$ | Output Pulse Width | HIGH (Above 2.0V)<br>LOW (Below 0.8V)<br>HIGH (Above 2.0V)<br>LOW (Below 0.8V) | 0.40T[1]<br>0.40T[1]<br>0.45T[2]<br>0.45T[2] | | 0.60T[1]<br>0.60T[1]<br>0.55T[2]<br>0.55T[2] | | T = Periods |
| $t_{per}$ | Output Period | | T – 400ps | | | | T = Desired Period |
| $t_{os}$ | Output-to-Output Skew | Rising Edges<br>Falling Edges | | | 400<br>500 | ps | |
| $t_r$, $t_f$ | Rise/Fall Times (Slew Rate) | | 1 | | 4 | V/ns | Series Terminated Transmission Lines |
| $t_{EN}$ | Enable Time | Enable1<br>Enable2 | | | 5<br>4 | ms<br>Cycles | |
| $t_{DIS}$ | Disable Time | Enable1<br>Enable2 | | | 4<br>4 | Cycles | |
| $A_{osc}$ | XTAL_IN to XTAL_OUT Oscillator Gain | | 6 | | | db | |
| Phase | Loop Phase Shift Modulo 360° + | | 30 | | | Degrees | |

1. Assuming input duty cycle specs from Recommended Operationg Conditions table are met.
2. Assuming external crystal or 50% duty cycle external reference is used.

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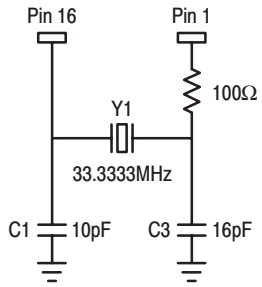



**Figure 1. Crystal Oscillator Interface**
(Fundamental)

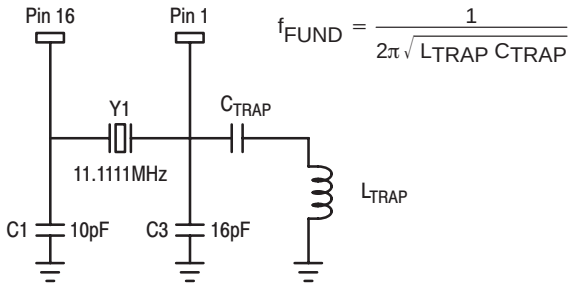



**Figure 2. Crystal Oscillator Interface**
(3rd Overtone)

**Table 1. Crystal Specifications**

| Parameter | Value |
|---|---|
| Crystal Cut | Fundamental AT Cut |
| Resonance | Parallel Resonance* |
| Frequency Tolerance | ±75ppm at 25°C |
| Frequency/Temperature Stability | ±150pm 0 to 70°C |
| Operating Range | 0 to 70°C |
| Shunt Capacitance | 5–7pF |
| Equivalent Series Resistance (ESR) | 50 to 80Ω |
| Correlation Drive Level | 100μW |
| Aging | 5ppm/Yr (First 3 Years) |

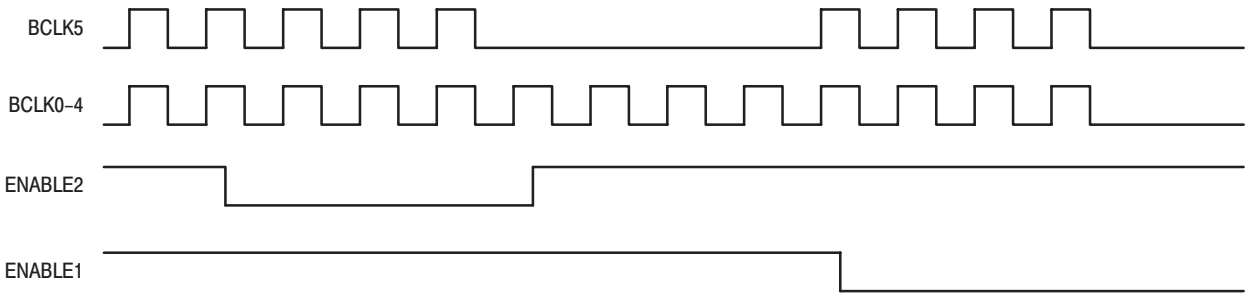



**Figure 3. Enable Timing Diagram**

## APPLICATIONS INFORMATION

### Driving Transmission Lines

The MPC905 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC905 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC905 clock driver is effectively doubled due to its capability to drive multiple lines.

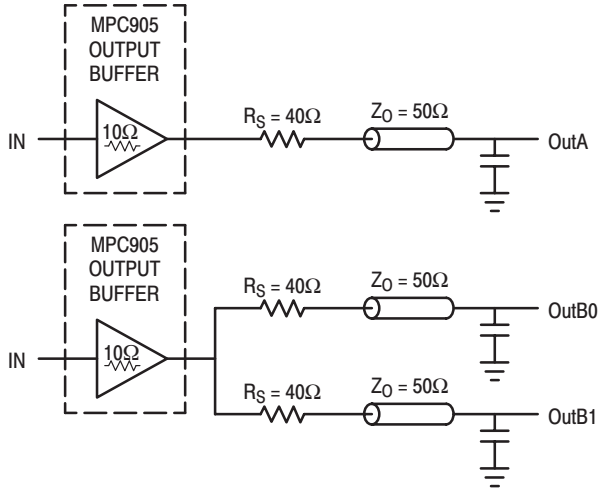



**Figure 4. Single versus Dual Transmission Lines**

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC905 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 40Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS ( Zo / Rs + Ro + Zo) = 3.0 (25/55) = 1.36V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.73V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

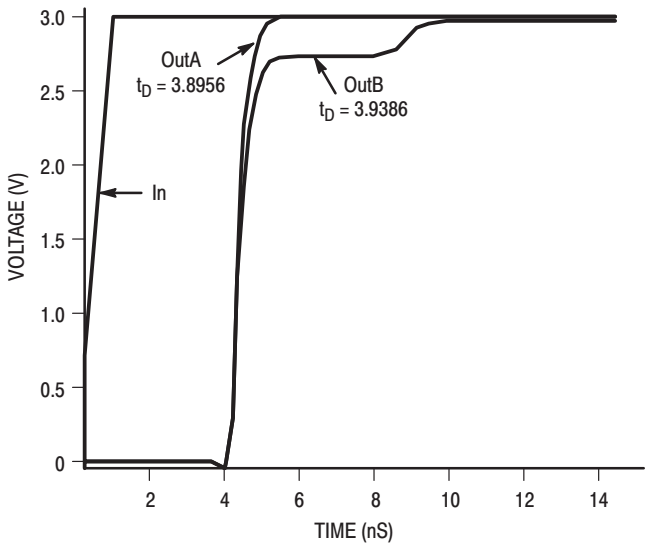
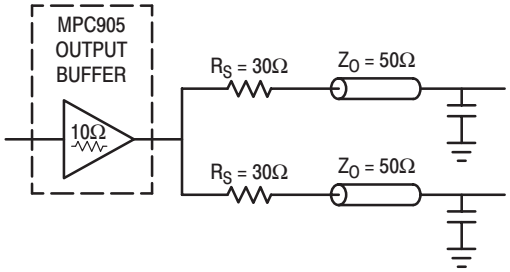



**Figure 5. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




$10\Omega + 30\Omega \parallel 30\Omega = 50\Omega \parallel 50\Omega$
$25\Omega = 25\Omega$

**Figure 6. Optimized Dual Line Termination**

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# Low Voltage 1:18 Clock Distribution Chip

**MPC940L**

**LOW VOLTAGE 1:18 CLOCK DISTRIBUTION CHIP**

The MPC940L is a 1:18 low voltage clock distribution chip with 2.5V or 3.3V LVCMOS output capabilities. The device features the capability to select either a differential LVPECL or an LVCMOS compatible input. The 18 outputs are 2.5V or 3.3V LVCMOS compatible and feature the drive strength to drive 50Ω series or parallel terminated transmission lines. With output–to–output skews of 150ps, the MPC940L is ideal as a clock distribution chip for the most demanding of synchronous systems. The 2.5V outputs also make the device ideal for supplying clocks for a high performance microprocessor based design. For a similar device at a lower price/performance point the reader is referred to the MPC9109.

- LVPECL or LVCMOS Clock Input
- 2.5V LVCMOS Outputs for Pentium II Microprocessor Support
- 150ps Maximum Output–to–Output Skew
- Maximum Output Frequency of 250MHz
- 32–Lead LQFP Packaging
- Dual or Single Supply Device:
  - Dual $V_{CC}$ Supply Voltage, 3.3V Core and 2.5V Output
  - Single 3.3V $V_{CC}$ Supply Voltage for 3.3V Outputs
  - Single 2.5V $V_{CC}$ Supply Voltage for 2.5V I/O

**FA SUFFIX**
32–LEAD LQFP PACKAGE
CASE 873A–02

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With a low output impedance (≈20Ω), in both the HIGH and LOW logic states, the output buffers of the MPC940L are ideal for driving series terminated transmission lines. With a 20Ω output impedance the 940L has the capability of driving two series terminated lines from each output. This gives the device an effective fanout of 1:36. If a lower output impedance is desired please see the MPC942 data sheet.

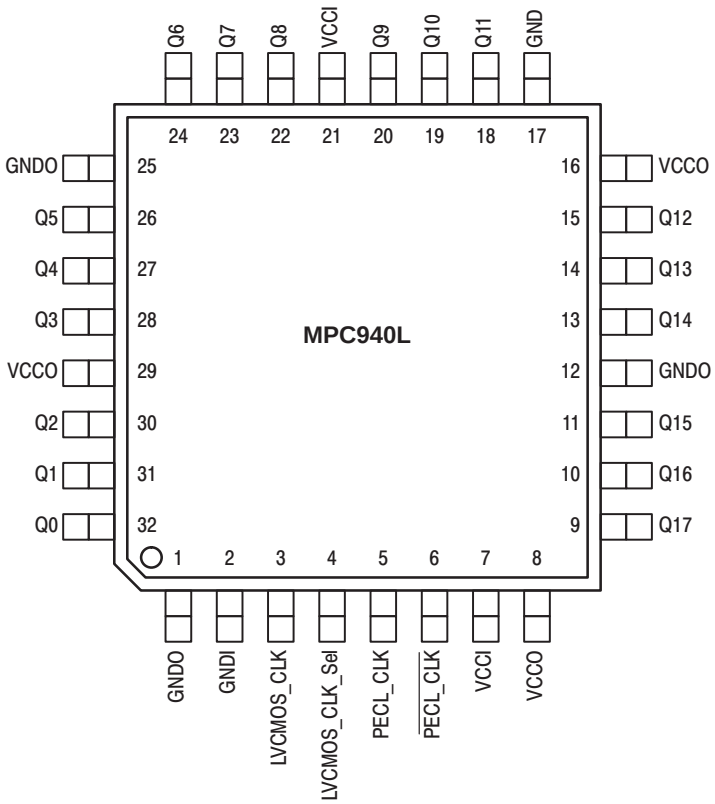
The differential LVPECL inputs of the MPC940L allow the device to interface directly with a LVPECL fanout buffer like the MC100EP111 to build very wide clock fanout trees or to couple to a high frequency clock source. The LVCMOS input provides a more standard interface for applications requiring only a single clock distribution chip at relatively low frequencies. In addition, the two clock sources can be used to provide for a test clock interface as well as the primary system clock. A logic HIGH on the LVCMOS_CLK_Sel pin will select the LVCMOS level clock input. All inputs of the MPC940L have internal pullup/pulldown resistor so they can be left open if unused.

The MPC940L is a single or dual supply device. The device power supply offers a high degree of flexibility. The device can operate with a 3.3V core and 3.3V output, a 3.3V core and 2.5V outputs as well as a 2.5V core and 2.5V outputs. The 32–lead LQFP package was chosen to optimize performance, board space and cost of the device. The 32–lead LQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

**Rev 3**

## LOGIC DIAGRAM


**Pinout: 32–Lead TQFP** (Top View)




### FUNCTION TABLE

| LVCMOS_CLK_Sel | Input |
|---|---|
| 0 | PECL_CLK |
| 1 | LVCMOS_CLK |

### POWER SUPPLY VOLTAGES

| Supply Pin | Voltage Level |
|---|---|
| VCCI | 2.5V or 3.3V ± 5% |
| VCCO | 2.5V or 3.3V ± 5% |

### PIN CONFIGURATIONS

| Pin | I/O | Type | Function |
|---|---|---|---|
| PECL_CLK<br>$\overline{\text{PECL\_CLK}}$ | Input | LVPECL | Reference Clock Input |
| LVCMOS_CLK | Input | LVCMOS | Alternative Reference Clock Input |
| LVCMOS_CLK_SEL | Input | LVCMOS | Selects Clock Source |
| Q0–Q17 | Output | LVCMOS | Clock Outputs |
| VCCO | | Supply | Output Positive Power Supply |
| VCCI | | Supply | Core Positive Power Supply |
| GNDO | | Supply | Output Negative Power Supply |
| GNDI | | Supply | Core Negative Power Supply |

**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 3.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_{IN}$ | Input Current | | ±20 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CCI}$ = 3.3V ±5%; $V_{CCO}$ = 3.3V ±5%)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | CMOS_CLK | 2.4 | | $V_{CCI}$ | V | |
| $V_{IL}$ | Input LOW Voltage | CMOS_CLK | | | 0.8 | V | |
| $V_{PP}$ | Peak–to–Peak Input Voltage | PECL_CLK | 500 | | 1000 | mV | |
| $V_{CMR}$ | Common Mode Range | PECL_CLK | $V_{CC}$–1.4 | | $V_{CC}$–0.6 | V | |
| $V_{OH}$ | Output HIGH Voltage | | 2.4 | | | V | $I_{OH}$ = –20mA |
| $V_{OL}$ | Output LOW Voltage | | | | 0.5 | V | $I_{OH}$ = 20mA |
| $I_{IN}$ | Input Current | | | | ±200 | µA | |
| $C_{IN}$ | Input Capacitance | | | 4.0 | | pF | |
| $C_{pd}$ | Power Dissipation Capacitance | | | 10 | | pF | per output |
| $Z_{OUT}$ | Output Impedance | | 18 | 23 | 28 | Ω | |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | 0.5 | 1.0 | mA | |

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CCI}$ = 3.3V ±5%; $V_{CCO}$ = 3.3V ±5%)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $F_{max}$ | Maximum Input Frequency | | | | 250 | MHz | |
| $t_{PLH}$ | Propagation Delay | PECL_CLK ≤ 150MHz<br>CMOS_CLK ≤ 150MHz | 2.0<br>1.8 | 2.7<br>2.5 | 3.4<br>3.0 | ns | Note 1. |
| $t_{PLH}$ | Propagation Delay | PECL_CLK > 150MHz<br>CMOS_CLK > 150MHz | 2.0<br>1.8 | 2.9<br>2.4 | 3.7<br>3.2 | ns | |
| $t_{sk(o)}$ | Output–to–Output Skew | PECL_CLK<br>CMOS_CLK | | | 150<br>150 | ps | Note 1. |
| $t_{sk(pp)}$ | Part–to–Part Skew | PECL_CLK < 150MHz<br>CMOS_CLK < 150MHz | | | 1.4<br>1.2 | ns | Notes 1., 2. |
| $t_{sk(pp)}$ | Part–to–Part Skew | PECL_CLK > 150MHz<br>CMOS_CLK > 150MHz | | | 1.7<br>1.4 | ns | Notes 1., 2. |
| $t_{sk(pp)}$ | Part–to–Part Skew | PECL_CLK<br>CMOS_CLK | | | 850<br>750 | ps | Notes 1., 3. |
| DC | Output Duty Cycle | $f_{CLK}$ < 134 MHz<br>$f_{CLK}$ ≤ 250 MHz | 45<br>40 | 50<br>50 | 55<br>60 | %<br>% | Input DC = 50%<br>Input DC = 50% |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.3 | | 1.1 | ns | 0.5 – 2.4 V |

1. Tested using standard input levels, Production tested @ 150MHz.
2. Across temperature and voltage ranges, Includes output skew.
3. For a specific temperature and voltage, Includes output skew.

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**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CCI}$ = 3.3V ±5%; $V_{CCO}$ = 2.5V ±5%)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | CMOS_CLK | 2.4 | | $V_{CCI}$ | V | |
| $V_{IL}$ | Input LOW Voltage | CMOS_CLK | | | 0.8 | V | |
| $V_{PP}$ | Peak–to–Peak Input Voltage | PECL_CLK | 500 | | 1000 | mV | |
| $V_{CMR}$ | Common Mode Range | PECL_CLK | $V_{CC}$–1.4 | | $V_{CC}$–0.6 | V | |
| $V_{OH}$ | Output HIGH Voltage | | 1.8 | | | V | $I_{OH}$ = –20mA |
| $V_{OL}$ | Output LOW Voltage | | | | 0.5 | V | $I_{OH}$ = 20mA |
| $I_{IN}$ | Input Current | | | | ±200 | µA | |
| $C_{IN}$ | Input Capacitance | | | 4.0 | | pF | |
| $C_{pd}$ | Power Dissipation Capacitance | | | 10 | | pF | per output |
| $Z_{OUT}$ | Output Impedance | | | 23 | | Ω | |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | 0.5 | 1.0 | mA | |

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CCI}$ = 3.3V ±5%; $V_{CCO}$ = 2.5V ±5%)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $F_{max}$ | Maximum Input Frequency | | | | 250 | MHz | |
| $t_{PLH}$ | Propagation Delay | PECL_CLK ≤ 150MHz<br>CMOS_CLK ≤ 150MHz | 2.0<br>1.7 | 2.8<br>2.5 | 3.5<br>3.0 | ns | Note 1. |
| $t_{PLH}$ | Propagation Delay | PECL_CLK > 150MHz<br>CMOS_CLK > 150MHz | 2.0<br>1.8 | 2.9<br>2.5 | 3.8<br>3.3 | ns | |
| $t_{sk(o)}$ | Output–to–Output Skew | PECL_CLK<br>CMOS_CLK | | | 150<br>150 | ps | Note 1. |
| $t_{sk(pp)}$ | Part–to–Part Skew | PECL_CLK < 150MHz<br>CMOS_CLK < 150MHz | | | 1.5<br>1.3 | ns | Notes 1., 2. |
| $t_{sk(pp)}$ | Part–to–Part Skew | PECL_CLK > 150MHz<br>CMOS_CLK > 150MHz | | | 1.8<br>1.5 | ns | Notes 1., 2. |
| $t_{sk(pp)}$ | Part–to–Part Skew | PECL_CLK<br>CMOS_CLK | | | 850<br>750 | ps | Notes 1., 3. |
| DC | Output Duty Cycle | $f_{CLK}$ < 134 MHz<br>$f_{CLK}$ ≤ 250 MHz | 45<br>40 | 50<br>50 | 55<br>60 | %<br>% | Input DC = 50%<br>Input DC = 50% |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.3 | | 1.2 | ns | 0.5 – 1.8 V |

1. Tested using standard input levels, Production tested @ 150MHz.
2. Across temperature and voltage ranges, Includes output skew.
3. For a specific temperature and voltage, Includes output skew.

**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CCI}$ = 2.5V ±5%; $V_{CCO}$ = 2.5V ±5%)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | CMOS_CLK | 2.0 | | $V_{CCI}$ | V | |
| $V_{IL}$ | Input LOW Voltage | CMOS_CLK | | | 0.8 | V | |
| $V_{PP}$ | Peak–to–Peak Input Voltage | PECL_CLK | 500 | | 1000 | mV | |
| $V_{CMR}$ | Common Mode Range | PECL_CLK | $V_{CC}$–1.0 | | $V_{CC}$–0.6 | V | |
| $V_{OH}$ | Output HIGH Voltage | | 1.8 | | | V | $I_{OH}$ = –12mA |
| $V_{OL}$ | Output LOW Voltage | | | | 0.5 | V | $I_{OH}$ = 12mA |
| $I_{IN}$ | Input Current | | | | ±200 | µA | |
| $C_{IN}$ | Input Capacitance | | | 4.0 | | pF | |
| $C_{pd}$ | Power Dissipation Capacitance | | | 10 | | pF | per output |
| $Z_{OUT}$ | Output Impedance | | 18 | 23 | 28 | Ω | |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | 0.5 | 1.0 | mA | |

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CCI}$ = 2.5V ±5%; $V_{CCO}$ = 2.5V ±5%)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $F_{max}$ | Maximum Input Frequency | | | | 200 | MHz | |
| $t_{PLH}$ | Propagation Delay | PECL_CLK ≤ 150MHz<br>CMOS_CLK ≤ 150MHz | 2.6<br>2.3 | 4.0<br>3.1 | 5.2<br>4.0 | ns | Note 1. |
| $t_{PLH}$ | Propagation Delay | PECL_CLK > 150MHz<br>CMOS_CLK > 150MHz | 2.8<br>2.3 | 3.8<br>3.1 | 5.0<br>4.0 | ns | |
| $t_{sk(o)}$ | Output–to–Output Skew | PECL_CLK<br>CMOS_CLK | | | 200<br>200 | ps | Note 1. |
| $t_{sk(pp)}$ | Part–to–Part Skew | PECL_CLK < 150MHz<br>CMOS_CLK < 150MHz | | | 2.6<br>1.7 | ns | Notes 1., 2. |
| $t_{sk(pp)}$ | Part–to–Part Skew | PECL_CLK > 150MHz<br>CMOS_CLK > 150MHz | | | 2.2<br>1.7 | ns | Notes 1., 2. |
| $t_{sk(pp)}$ | Part–to–Part Skew | PECL_CLK<br>CMOS_CLK | | | 1.2<br>1.0 | ns | Notes 1., 3. |
| DC | Output Duty Cycle | $f_{CLK}$ < 134 MHz<br>$f_{CLK}$ ≤ 250 MHz | 45<br>40 | 50<br>50 | 55<br>60 | %<br>% | Input DC = 50%<br>Input DC = 50% |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.3 | | 1.2 | ns | 0.5 – 1.8 V |

1. Tested using standard input levels, Production tested @ 150MHz.
2. Across temperature and voltage ranges, Includes output skew.
3. For a specific temperature and voltage, Includes output skew.

5

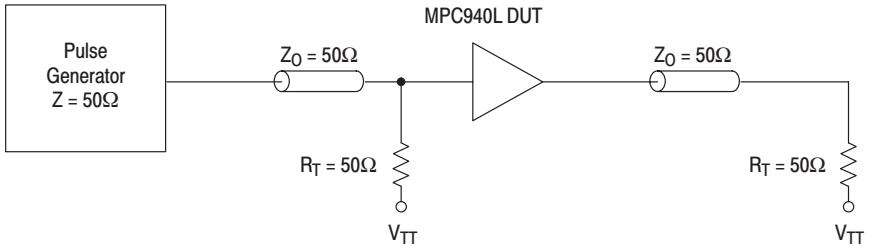



**Figure 1. LVCMOS_CLK MPC940L AC test reference for $V_{cc}$ = 3.3V and $V_{cc}$ = 2.5V**

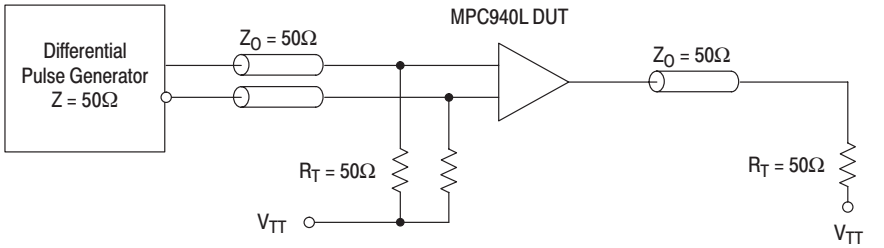



**Figure 2. PECL_CLK MPC940L AC test reference for $V_{cc}$ = 3.3V and $V_{cc}$ = 2.5V**

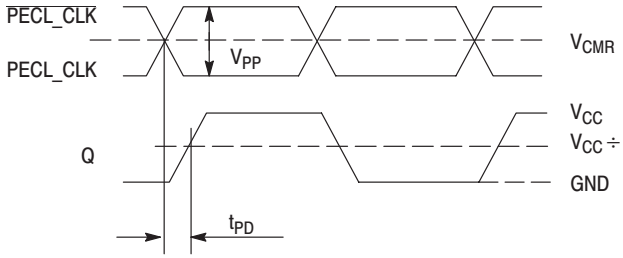



**Figure 3. Propagation delay ($t_{PD}$) test reference**

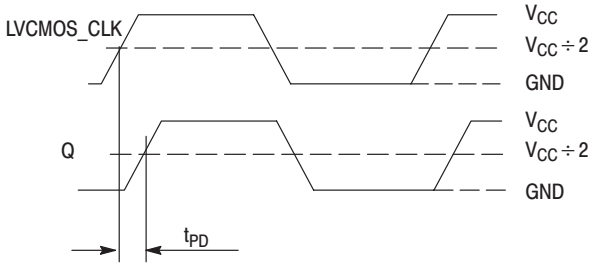
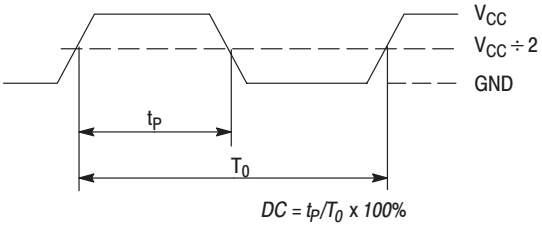
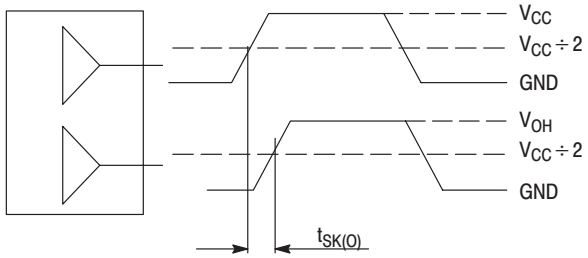



**Figure 4. LVCMOS Propagation delay ($t_{PD}$) test reference**



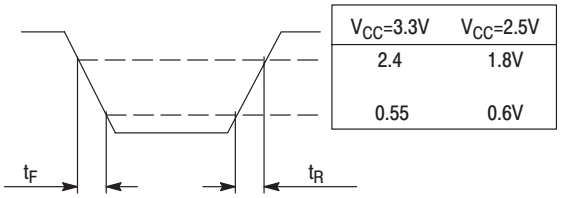

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 5. Output Duty Cycle (DC)**



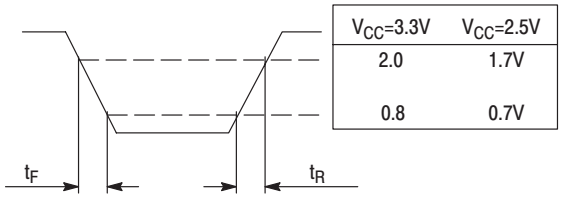

The pin–to–pin skew is defined as the worst case difference in propagation delay between any two similar delay path within a single device

**Figure 6. Output–to–output Skew $t_{SK(O)}$**




| $V_{CC}$=3.3V | $V_{CC}$=2.5V |
|---|---|
| 2.4 | 1.8V |
| 0.55 | 0.6V |

**Figure 7. Output Transition Time Test Reference**




| $V_{CC}$=3.3V | $V_{CC}$=2.5V |
|---|---|
| 2.0 | 1.7V |
| 0.8 | 0.7V |

**Figure 8. Input Transition Time Test Reference**

# Low Voltage 1:27 Clock Distribution Chip

**MPC941**

**LOW VOLTAGE 3.3V/2.5V 1:27 CLOCK DISTRIBUTION CHIP**

The MPC941 is a 1:27 low voltage clock distribution chip. The device features the capability to select either a differential LVPECL or an LVCMOS compatible input. The 27 outputs are LVCMOS compatible and feature the drive strength to drive 50Ω series or parallel terminated transmission lines. With output–to–output skews of 250ps, the MPC941 is ideal as a clock distribution chip for the most demanding of synchronous systems. For a similar product with a smaller number of outputs, please consult the MPC940 data sheet.

- LVPECL or LVCMOS Clock Input
- 250ps Maximum Output–to–Output Skew
- Drives Up to 54 Independent Clock Lines
- Maximum Output Frequency of 250MHz
- High Impedance Output Enable
- Extended Temperature Range: –40°C to +85°C
- 48–Lead LQFP Packaging
- 3.3V or 2.5V $V_{CC}$ Supply Voltage

**FA SUFFIX**
48–LEAD LQFP PACKAGE
CASE 932–02

With a low output impedance, in both the HIGH and LOW logic states, the output buffers of the MPC941 are ideal for driving series terminated transmission lines. More specifically, each of the 27 MPC941 outputs can drive two series terminated 50Ω transmission lines. With this capability, the MPC941 has an effective fanout of 1:54. With this level of fanout, the MPC941 provides enough copies of low skew clocks for most high performance synchronous systems.

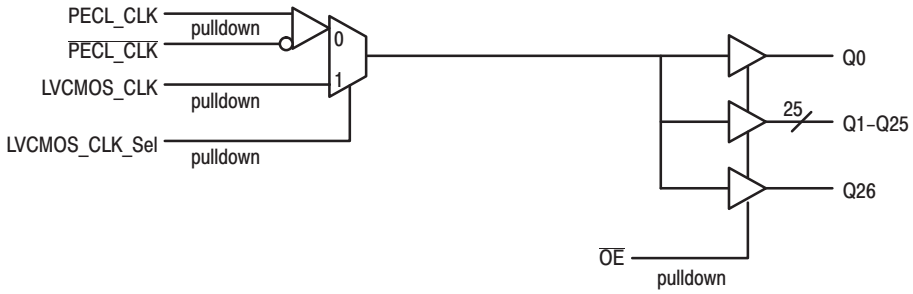
The differential LVPECL inputs of the MPC941 allow the device to interface directly with an LVPECL fanout buffer like the MC100EP111 to build very wide clock fanout trees or to couple to a high frequency clock source. The LVCMOS input provides a more standard interface for applications requiring only a single clock distribution chip at relatively low frequencies. In addition, the two clock sources can be used as a test clock interface as well as the primary system clock. A logic HIGH on the LVCMOS_CLK_Sel pin will select the LVCMOS level clock input.

The MPC941 is fully 3.3V and 2.5V compatible. The 48–lead LQFP package was chosen to optimize performance, board space and cost of the device. The 48–lead LQFP has a 7x7mm body size.

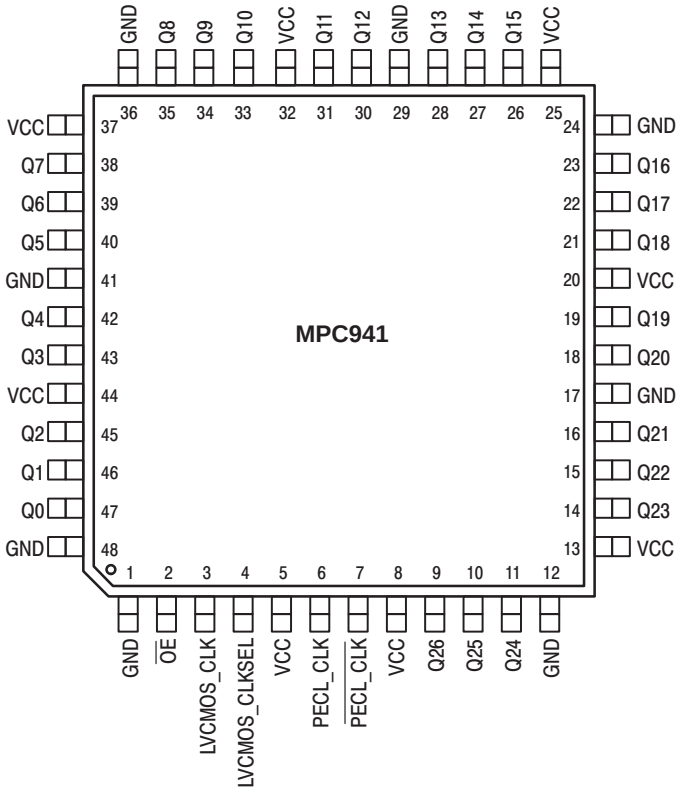


**Rev 4**

**LOGIC DIAGRAM**




**Pinout: 48–Lead QFP** (Top View)




**FUNCTION TABLE**

| LVCMOS_CLK_Sel | Input |
|---|---|
| 0 | PECL_CLK |
| 1 | LVCMOS_CLK |

**Table 1: PIN CONFIGURATIONS**

| Pin | I/O | Type | Function |
|---|---|---|---|
| PECL_CLK, $\overline{\text{PECL\_CLK}}$ | Input | LVPECL | LVPECL differential reference clock inputs |
| LVCMOS_CLK | Input | LVCMOS | Alternative reference clock input |
| LVCMOS_CLK_Sel | Input | LVCMOS | Input reference clock select |
| $\overline{\text{OE}}$ | Input | LVCMOS | Output tristate control |
| GND | | Supply | Negative voltage supply output bank (GND) |
| VCC | | Supply | Positive voltage supply |
| Q0 - Q26 | Output | LVCMOS | Clock outputs |

**Table 2: ABSOLUTE MAXIMUM RATINGS***

| Symbol | Characteristics | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V |
| $I_{IN}$ | DC Input Current | | ±20 | mA |
| $I_{OUT}$ | DC Output Current | | ±50 | mA |
| $T_S$ | Storage temperature | -40 | 125 | °C |

* Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

**Table 3: DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40 to +85°C)

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | LVCMOS_CLK | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | LVCMOS_CLK | -0.3 | | 0.8 | V | LVCMOS |
| $I_{IN}$ | Input current | | | | ±120[a] | µA | |
| $V_{PP}$ | Peak-to-peak input voltage | PECL_CLK, $\overline{\text{PECL\_CLK}}$ | 500 | | | mV | LVPECL |
| $V_{CMR}$ | Common Mode Range | PECL_CLK, $\overline{\text{PECL\_CLK}}$ | 1.2 | | $V_{CC}$-0.8 | V | LVPECL |
| $V_{OH}$ | Output High Voltage | | 2.4 | | | V | $I_{OH}$=-24 mA[b] |
| $V_{OL}$ | Output Low Voltage | | | | 0.55<br>0.40 | V<br>V | $I_{OL}$= 24mA [b]<br>$I_{OL}$=12mA |
| $I_{OZ}$ | Output tristate leakage current | | | | 100 | µA | |
| $Z_{OUT}$ | Output impedance | | | 14 - 17 | | Ω | |
| $C_{PD}$ | Power Dissipation Capacitance | | | 7-8 | 10 | pF | Per Output |
| $C_{IN}$ | Input capacitance | | | 4.0 | | pF | |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | | 5 | mA | All $V_{CC}$ Pins |
| $V_{TT}$ | Output termination voltage | | | $V_{CC}$÷2 | | V | |

a. Input pull-up / pull-down resistors influence input current.
b. The MPC941 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

**Table 4: AC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40 to +85°C)[a]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Output Frequency | 0 | | 250[b] | MHz | |
| $t_r$, $t_f$ | LVCMOS_CLK Input Rise/Fall Time | | | 1.0[c] | ns | 0.8 to 2.0V |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay PECL_CLK to any Q<br>LVCMOS_CLK to any Q | 1.2<br>0.9 | 1.8<br>1.5 | 2.6<br>2.3 | ns<br>ns | |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | ns | |
| $t_{sk(O)}$ | Output-to-output Skew PECL_CLK to any Q<br>LVCMOS_CLK to any Q | | 125<br>125 | 250<br>250 | ps | |
| $t_{sk(PP)}$ | Device-to-device Skew PECL_CLK to any Q<br>LVCMOS_CLK to any Q | | | 1000<br>1000 | ps<br>ps | For a given $T_A$ and $V_{CC}$, any Q |
| $t_{sk(PP)}$ | Device-to-device Skew PECL_CLK to any Q<br>LVCMOS_CLK to any Q | | | 1400<br>1400 | ps<br>ps | For any $T_A$, $V_{CC}$ and Q |
| $DC_Q$ | Output Duty Cycle PECL_CLK to any Q<br>LVCMOS_CLK to any Q | 45<br>45 | 50<br>50 | 60<br>55 | %<br>% | $DC_{REF}$ = 50%<br>$DC_{REF}$ = 50% |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.2 | | 1.0 | ns | 0.55 to 2.4V |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
b. AC characteristics are guaranteed up to $f_{max}$. Please refer to applications section for information on power consumption versus operating frequency and thermal management.
c. Fast input signal transition times are required to maintain part-to-part skew specification. If part-to-part skew is not critical to the application, signal transition times smaller than 3 ns can be applied to the MPC941.

**Table 5: DC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40 to +85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage LVCMOS_CLK | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage LVCMOS_CLK | -0.3 | | 0.7 | V | LVCMOS |
| $I_{IN}$ | Input current | | | ±120[a] | µA | |
| $V_{PP}$ | Peak-to-peak input voltage PECL_CLK, $\overline{\text{PECL\_CLK}}$ | 500 | | | mV | LVPECL |
| $V_{CMR}$ | Common Mode Range PECL_CLK, $\overline{\text{PECL\_CLK}}$ | 1.1 | | $V_{CC}$-0.7 | V | LVPECL |
| $V_{OH}$ | Output High Voltage | 1.8 | | | V | $I_{OH}$=-15 mA[b] |
| $V_{OL}$ | Output Low Voltage | | | 0.6 | V | $I_{OL}$= 15 mA[b] |
| $I_{OZ}$ | Output tristate leakage current | | | 100 | µA | |
| $Z_{OUT}$ | Output impedance | | 18 – 20 | | Ω | |
| $C_{PD}$ | Power Dissipation Capacitance | | 7–8 | 10 | pF | Per Output |
| $C_{IN}$ | Input capacitance | | 4.0 | | pF | |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | 5 | mA | All $V_{CC}$ Pins |
| $V_{TT}$ | Output termination voltage | | $V_{CC}$÷2 | | V | |

a. Input pull-up / pull-down resistors influence input current.
b. The MPC941 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

5

**Table 6: AC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40 to +85°C)[a]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Output Frequency | 0 | | 250[b] | MHz | |
| $t_r$, $t_f$ | LVCMOS_CLK Input Rise/Fall Time | | | 1.0[c] | ns | 0.7 to 1.7V |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay PECL_CLK to any Q<br>LVCMOS_CLK to any Q | 1.3<br>1.0 | 2.1<br>1.8 | 2.9<br>2.6 | ns<br>ns | |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | ns | |
| $t_{sk(O)}$ | Output-to-output Skew PECL_CLK to any Q<br>LVCMOS_CLK to any Q | | 125<br>125 | 250<br>250 | ps | |
| $t_{sk(PP)}$ | Device-to-device Skew PECL_CLK to any Q<br>LVCMOS_CLK to any Q | | | 1200<br>1200 | ps<br>ps | For a given $T_A$ and $V_{CC}$, any Q |
| $t_{sk(PP)}$ | Device-to-device Skew PECL_CLK to any Q<br>LVCMOS_CLK to any Q | | | 1600<br>1600 | ps<br>ps | For any $T_A$, $V_{CC}$ and Q |
| $DC_Q$ | Output Duty Cycle PECL_CLK to any Q<br>LVCMOS_CLK to any Q | 45<br>45 | 50<br>50 | 60<br>55 | %<br>% | $DC_{REF}$ = 50%<br>$DC_{REF}$ = 50% |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.2 | | 1.0 | ns | 0.6 to 1.6V |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
b. AC characteristics are guaranteed up to $f_{max}$. Please refer to the applications section for information on power consumption versus operating frequency and thermal management.
c. Fast input signal transition times are required to maintain part-to-part skew specification. If part-to-part skew is not critical to the application, signal transition times smaller than 3 ns can be applied to the MPC941.

## APPLICATIONS INFORMATION

### Driving Transmission Lines

The MPC941 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC941 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 1 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC941 clock driver is effectively doubled due to its capability to drive multiple lines.

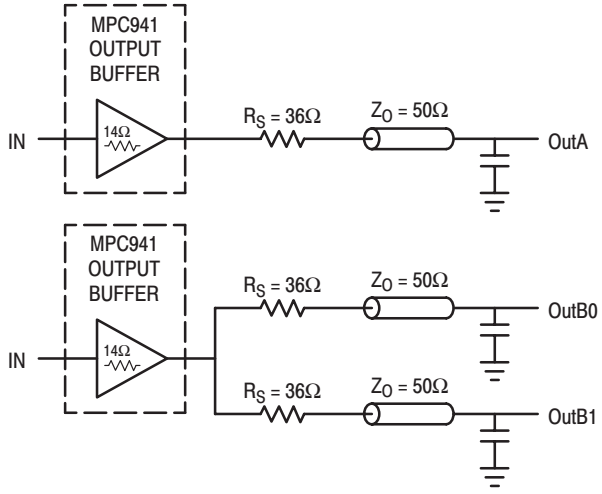



**Figure 1. Single versus Dual Transmission Lines**

The waveform plots of Figure 2 “Single versus Dual Waveforms” show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC941 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC941. The output waveform in Figure 2 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

VL = VS ( Zo / (Rs + Ro +Zo))
Zo = 50Ω || 50Ω
Rs = 36Ω || 36Ω
Ro = 14Ω
VL = 3.0 (25 / (18 + 14 + 25) = 3.0 (25 / 57)
= 1.31V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

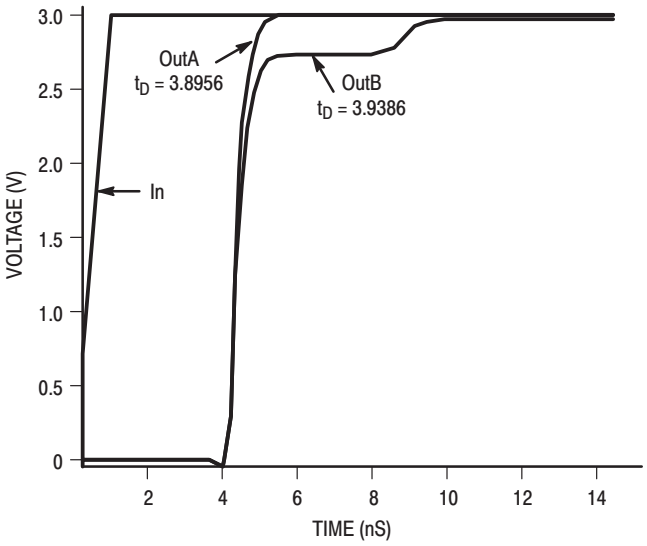
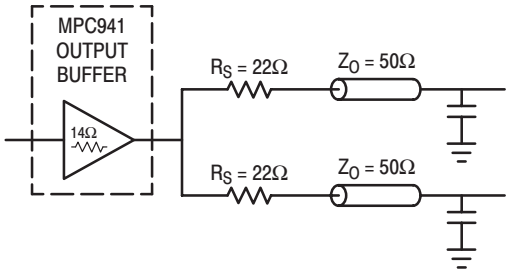



**Figure 2. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 3 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




14Ω + 22Ω || 22Ω = 50Ω || 50Ω
25Ω = 25Ω

**Figure 3. Optimized Dual Line Termination**

**Power Consumption of the MPC941 and Thermal Management**

The MPC941 AC specification is guaranteed for the entire operating frequency range up to 250 MHz. The MPC941 power consumption and the associated long-term reliability may decrease the maximum frequency limit, depending on operating conditions such as clock frequency, supply voltage, output loading, ambient temperture, vertical convection and thermal conductivity of package and board. This section describes the impact of these parameters on the junction temperature and gives a guideline to estimate the MPC941 die junction temperature and the associated device reliability. For a complete analysis of power consumption as a function of operating conditions and associated long term device reliability please refer to the application note AN1545. According the AN1545, the long-term device reliability is a function of the die junction temperature:

**Table 7: Die junction temperature and MTBF**

| Junction temperature (°C) | MTBF (Years) |
|---|---|
| 100 | 20.4 |
| 110 | 9.1 |
| 120 | 4.2 |
| 130 | 2.0 |

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Increased power consumption will increase the die junction temperature and impact the device reliability (MTBF). According to the system-defined tolerable MTBF, the die junction temperature of the MPC941 needs to be controlled and the thermal impedance of the board/package should be optimized. The power dissipated in the MPC941 is represented in equation 1.

Where $I_{CCQ}$ is the static current consumption of the MPC941, $C_{PD}$ is the power dissipation capacitance per output, $(M)\Sigma C_L$ represents the external capacitive output load, N is the number of active outputs (N is always 27 in case of the MPC941). The MPC941 supports driving transmission lines to maintain high signal integrity and tight timing parameters. Any transmission line will hide the lumped capacitive load at the end of the board trace, therefore, $\Sigma C_L$ is zero for controlled transmission line systems and can be eliminated from equation 1. Using parallel termination output termination results in equation 2 for power dissipation.

In equation 2, P stands for the number of outputs with a parallel or thevenin termination, $V_{OL}$, $I_{OL}$, $V_{OH}$ and $I_{OH}$ are a function of the output termination technique and $DC_Q$ is the clock signal duty cyle. If transmission lines are used $\Sigma C_L$ is zero in equation 2 and can be eliminated. In general, the use of controlled transmission line techniques eliminates the impact of the lumped capacitive loads at the end lines and greatly reduces the power dissipation of the device. Equation 3 describes the die junction temperature $T_J$ as a function of the power consumption.

Where $R_{thja}$ is the thermal impedance of the package (junction to ambient) and $T_A$ is the ambient temperature. According to Table 7, the junction temperature can be used to estimate the long-term device reliability. Further, combining equation 1 and equation 2 results in a maximum operating frequency for the MPC941 in a series terminated transmission line system.

$T_{J,MAX}$ should be selected according to the MTBF system requirements and Table 7. $R_{thja}$ can be derived from Table 8. The $R_{thja}$ represent data based on 1S2P boards, using 2S2P boards will result in a lower thermal impedance than indicated below.

**Table 8: Thermal package impedance of the 48ld LQFP**

| Convection, LFPM | $R_{thja}$ (1P2S board), K/W |
|---|---|
| Still air | 78 |
| 100 lfpm | 68 |
| 200 lfpm | 59 |
| 300 lfpm | 56 |
| 400 lfpm | 54 |
| 500 lfpm | 53 |

If the calculated maximum frequency is below 250 MHz, it becomes the upper clock speed limit for the given application conditions. The following eight derating charts describe the safe frequency operation range for the MPC941. The charts were calculated for a maximum tolerable die junction temperature of 110°C (120°C), corresponding to a estimated MTBF of 9.1 years (4 years), a supply voltage of either 3.3V or 2.5V and series terminated transmission line or capacitive loading. Depending on a given set of these operating conditions and the available device convection a decision on the maximum operating frequency can be made.

$$P_{TOT} = \left[ I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left( N \cdot C_{PD} + \sum_{M} C_L \right) \right] \cdot V_{CC} \qquad \text{Equation 1}$$

$$P_{TOT} = V_{CC} \cdot \left[ I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left( N \cdot C_{PD} + \sum_{M} C_L \right) \right] + \sum_{P} \left[ DC_Q \cdot I_{OH} \cdot (V_{CC} - V_{OH}) + (1 - DC_Q) \cdot I_{OL} \cdot V_{OL} \right] \qquad \text{Equation 2}$$

$$T_J = T_A + P_{TOT} \cdot R_{thja} \qquad \text{Equation 3}$$

$$f_{CLOCK,MAX} = \frac{1}{C_{PD} \cdot N \cdot V_{CC}^2} \cdot \left[ \frac{T_{J,MAX} - T_A}{R_{thja}} - (I_{CCQ} \cdot V_{CC}) \right] \qquad \text{Equation 4}$$

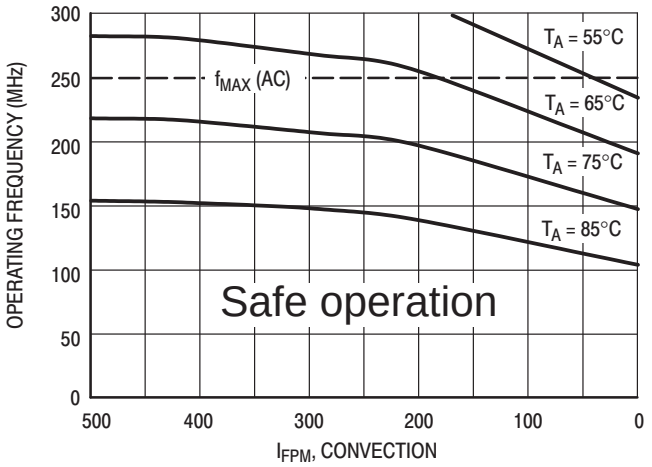


**Figure 4. Maximum MPC941 frequency, $V_{CC}$ = 3.3V, MTBF 9.1 years, driving series terminated transmission lines**

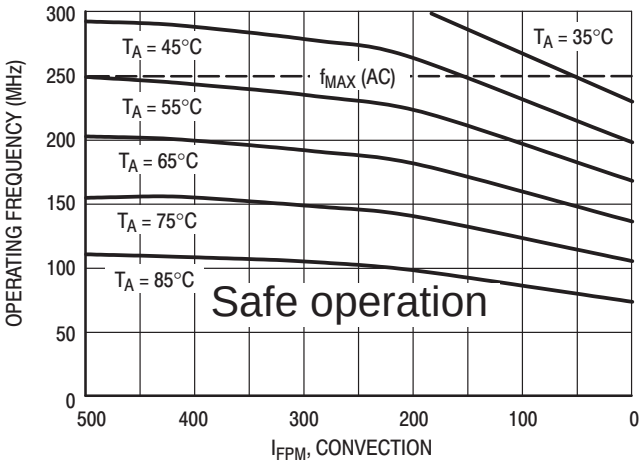


**Figure 5. Maximum MPC941 frequency, $V_{CC}$ = 3.3V, MTBF 9.1 years, 4 pF load per line**

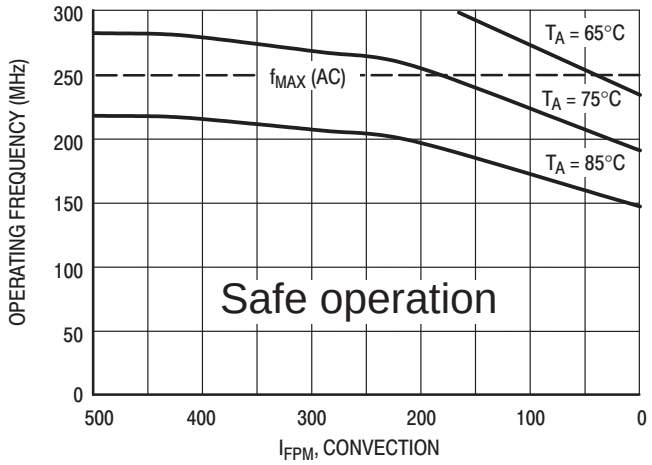


**Figure 6. Maximum MPC941 frequency, $V_{CC}$ = 3.3V, MTBF 4 years, driving series terminated transmission lines**

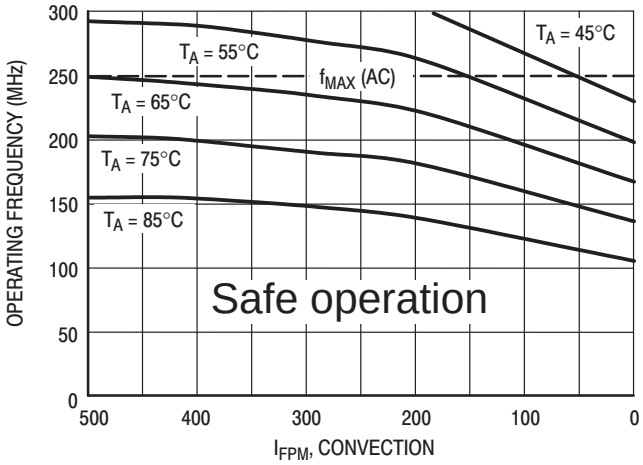


**Figure 7. Maximum MPC941 frequency, $V_{CC}$ = 3.3V, MTBF 4 years, 4 pF load per line**

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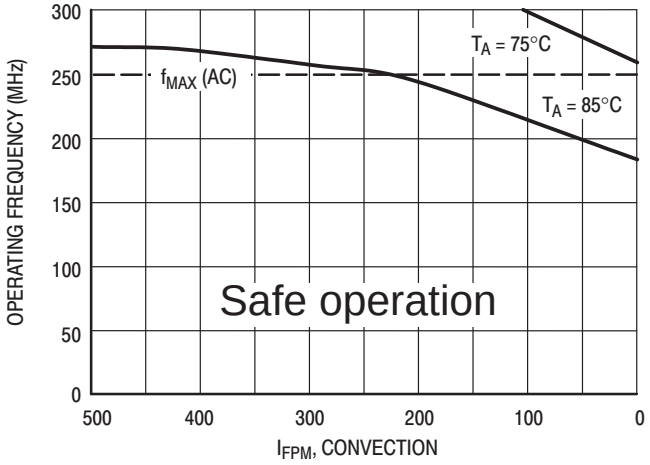



**Figure 8. Maximum MPC941 frequency, $V_{CC}$ = 2.5V, MTBF 9.1 years, driving series terminated transmission lines**

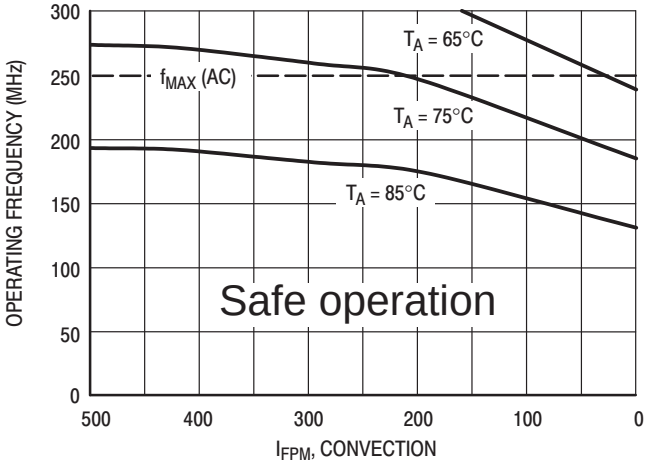



**Figure 9. Maximum MPC941 frequency, $V_{CC}$ = 2.5V, MTBF 9.1 years, 4 pF load per line**

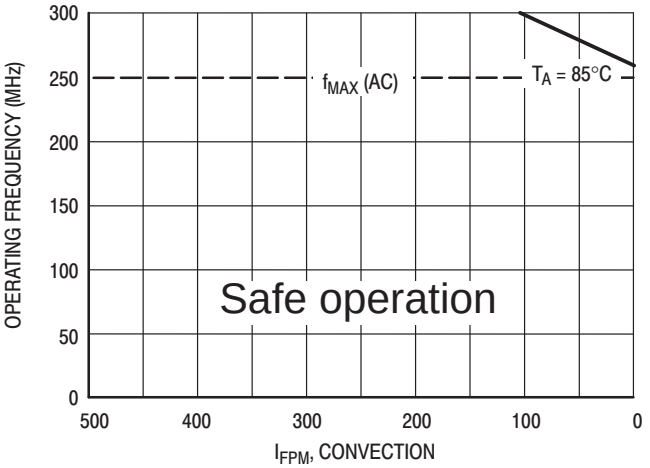



**Figure 10. Maximum MPC941 frequency, $V_{CC}$ = 2.5V, MTBF 4 years, driving series terminated transmission lines**

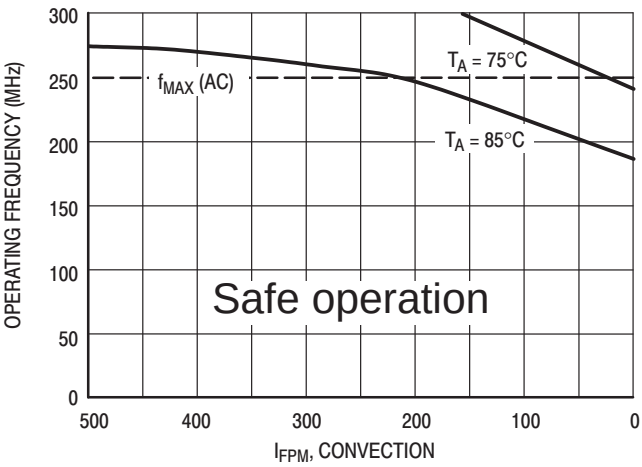



**Figure 11. Maximum MPC941 frequency, $V_{CC}$ = 2.5V, MTBF 4 years, 4 pF load per line**

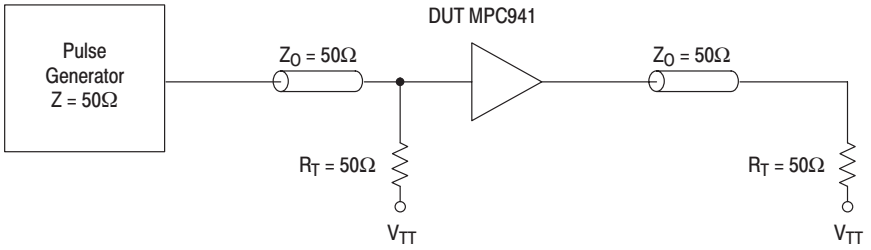



**Figure 12. LVCMOS_CLK MPC941 AC test reference for $V_{cc}$ = 3.3V and $V_{cc}$ = 2.5V**

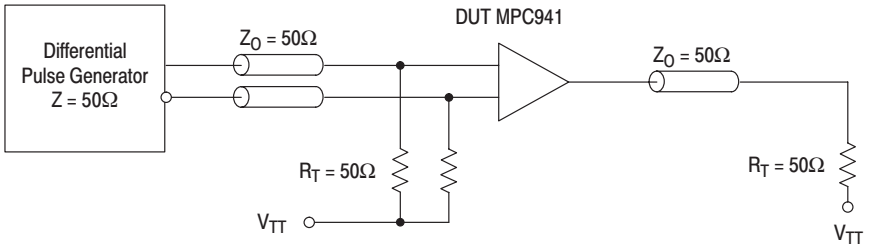



**Figure 13. PECL_CLK MPC941 AC test reference for $V_{cc}$ = 3.3V and $V_{cc}$ = 2.5V**

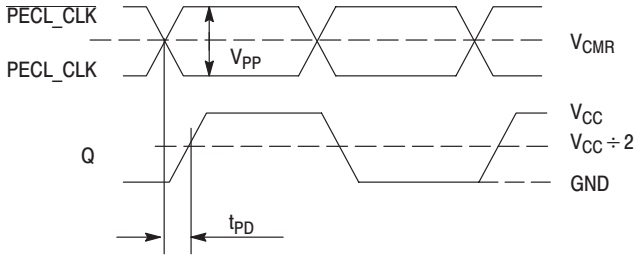



**Figure 14. LVPECL Propagation delay ($t_{PD}$) test reference**

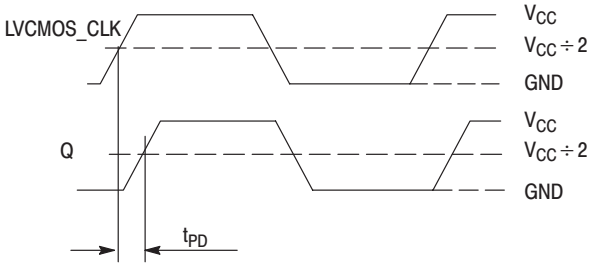
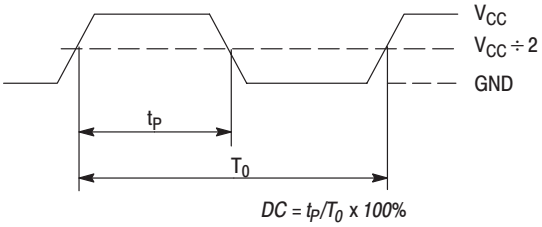
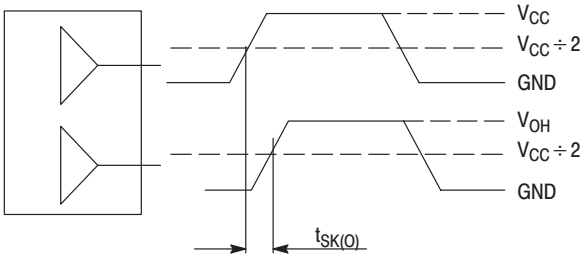



**Figure 15. LVCMOS Propagation delay ($t_{PD}$) test reference**



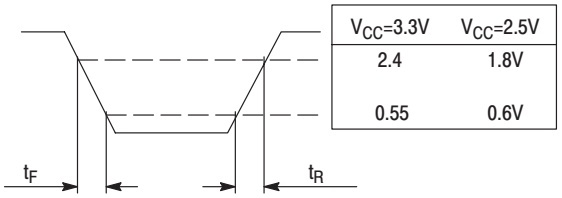

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 16. Output Duty Cycle (DC)**



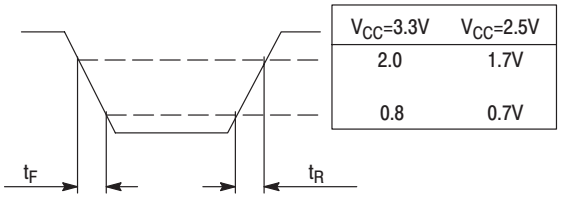

The pin–to–pin skew is defined as the worst case difference in propagation delay between any two similar delay paths within a single device

**Figure 17. Output–to–output Skew $t_{SK(O)}$**




| $V_{CC}$=3.3V | $V_{CC}$=2.5V |
|---|---|
| 2.4 | 1.8V |
| 0.55 | 0.6V |

**Figure 18. Output Transition Time Test Reference**




| $V_{CC}$=3.3V | $V_{CC}$=2.5V |
|---|---|
| 2.0 | 1.7V |
| 0.8 | 0.7V |

**Figure 19. Input Transition Time Test Reference**

# Low Voltage 1:18 Clock Distribution Chip

**MPC942C**

**LOW VOLTAGE 1:18 CLOCK DISTRIBUTION CHIP**

The MPC942 is a 1:18 low voltage clock distribution chip with 2.5V or 3.3V LVCMOS output capabilities. The device is offered in two versions; the MPC942C has an LVCMOS input clock while the MPC942P has a LVPECL input clock. The 18 outputs are 2.5V or 3.3V LVCMOS compatible and feature the drive strength to drive 50Ω series or parallel terminated transmission lines. With output–to–output skews of 200ps, the MPC942 is ideal as a clock distribution chip for the most demanding of synchronous systems. The 2.5V outputs also make the device ideal for supplying clocks for a high performance Pentium II™ microprocessor based design.

- LVCMOS/LVTTL Clock Input
- 2.5V LVCMOS Outputs for Pentium II Microprocessor Support
- 150ps Maximum Targeted Output–to–Output Skew
- Maximum Output Frequency of 250MHz @ 3.3 $V_{CC}$
- 32–Lead TQFP Packaging
- Single 3.3V or 2.5V Supply

**FA SUFFIX**
32–LEAD TQFP PACKAGE
CASE 873A–02

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With a low output impedance (≈12Ω), in both the HIGH and LOW logic states, the output buffers of the MPC942 are ideal for driving series terminated transmission lines. With an output impedance of 12Ω the MPC942 can drive two series terminated transmission lines from each output. This capability gives the MPC942 an effective fanout of 1:36. The MPC942 provides enough copies of low skew clocks for most high performance synchronous systems.

The LVCMOS/LVTTL input of the MPC942C provides a more standard LVCMOS interface. The OE pins will place the outputs into a high impedance state. The OE pin has an internal pullup resistor.

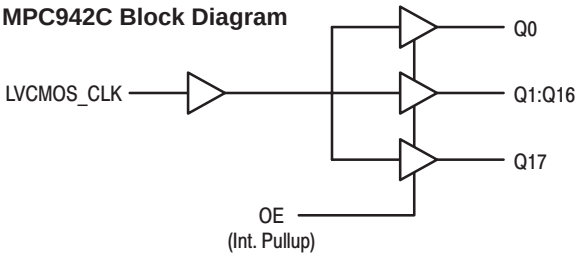
The MPC942 is a single supply device. The $V_{CC}$ power pins require either 2.5V or 3.3V. The 32–lead TQFP package was chosen to optimize performance, board space and cost of the device. The 32–lead TQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

Pentium II is a trademark of Intel Corporation.

**Rev 0**

## LOGIC DIAGRAM

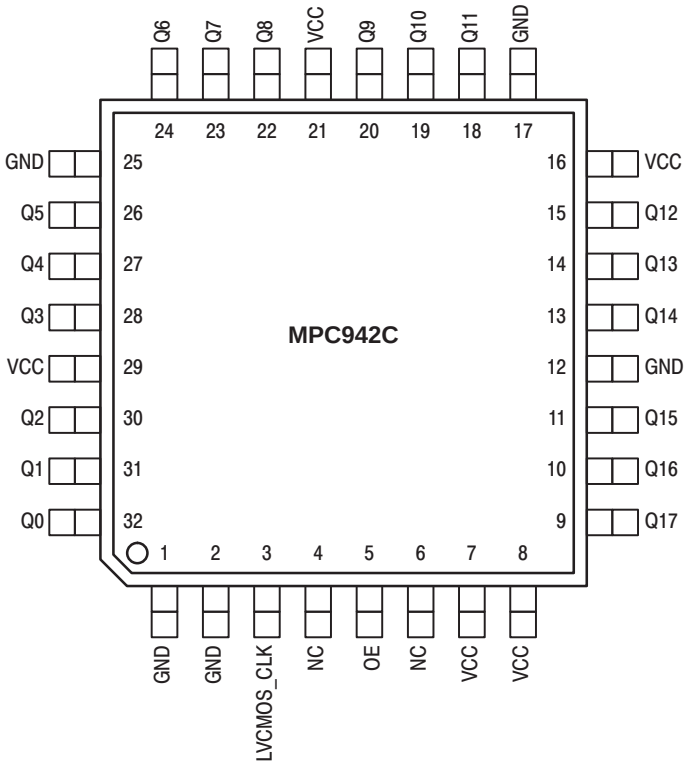
**MPC942C Block Diagram**




**FUNCTION TABLE**

| OE | Output |
|---|---|
| 0 | HIGH IMPEDANCE |
| 1 | OUTPUTS ENABLED |

**Pinout: 32–Lead** (Top View)




5

**ABSOLUTE MAXIMUM RATING**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 3.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | Input Current | | ±20 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CCI}$ = 2.5V ±5%, $V_{CCO}$ = 2.5V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | $V_{CCI}$ | V | |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | |
| $V_{OH}$ | Output HIGH Voltage | 2.0 | | | V | $I_{OH}$ = –16 mA |
| $V_{OL}$ | Output LOW Voltage | | | 0.5 | V | $I_{OL}$ = 16 mA |
| $I_{IN}$ | Input Current | | | ±200 | µA | |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | |
| $C_{PD}$ | Power Dissipation Capacitance | | 14 | | pF | Per Output |
| $Z_{OUT}$ | Output Impedance | | 12 | | Ω | |
| $I_{CC}$ | Maximum Quiescent Supply Current | | 0.5 | | mA | |

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CCI}$ = 2.5V ±5%, $V_{CCO}$ = 2.5V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $F_{max}$ | Maximum Frequency | | | 200 | MHz | |
| $t_{PLH}$ | Propagation Delay | 1.5 | | 2.8 | ns | |
| $t_{sk(o)}$ | Output–to–Output Skew | | | 200 | ps | |
| $t_{sk(pr)}$ | Part–to–Part Skew | | | 1.3 | ns | Notes 1, 2 |
| $t_{sk(pr)}$ | Part–to–Part Skew | | | 600 | ps | Notes 1, 3 |
| $d_t$ | Duty Cycle | 45 | | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.2 | | 1.0 | ns | |

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**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CCI}$ = 3.3V ±5%, $V_{CCO}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | 2.4 | | $V_{CCI}$ | V | |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | $I_{OH}$ = –20 mA |
| $V_{OL}$ | Output LOW Voltage | | | 0.5 | V | $I_{OL}$ = 20 mA |
| $I_{IN}$ | Input Current | | | ±200 | µA | |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | |
| $C_{PD}$ | Power Dissipation Capacitance | | 14 | | pF | Per Output |
| $Z_{OUT}$ | Output Impedance | | 12 | | Ω | |
| $I_{CC}$ | Maximum Quiescent Supply Current | | 0.5 | | mA | |

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CCI}$ = 3.3V ±5%, $V_{CCO}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $F_{max}$ | Maximum Frequency | | | 250 | MHz | |
| $t_{PLH}$ | Propagation Delay | 1.3 | | 2.3 | ns | Note 1 |
| $t_{sk(o)}$ | Output–to–Output Skew | | | 200 | ps | |
| $t_{sk(pr)}$ | Part–to–Part Skew | | | 1.0 | ns | Notes 1, 2 |
| $t_{sk(pr)}$ | Part–to–Part Skew | | | 500 | ps | Notes 1, 3 |
| $d_t$ | Duty Cycle | 45 | | 55 | % | |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.2 | | 1.0 | ns | |

1. Tested using standard input levels, production tested @ 133 MHz.
2. Across temperature and voltage ranges, includes output skew.
3. For a specific temperature and voltage, includes output skew.

# Low Voltage 1:18 Clock Distribution Chip

**MPC942P**

**LOW VOLTAGE 1:18 CLOCK DISTRIBUTION CHIP**

The MPC942 is a 1:18 low voltage clock distribution chip with 2.5V or 3.3V LVCMOS output capabilities. The device is offered in two versions; the MPC942C has an LVCMOS input clock while the MPC942P has a LVPECL input clock. The 18 outputs are 2.5V or 3.3V LVCMOS compatible and feature the drive strength to drive 50Ω series or parallel terminated transmission lines. With output–to–output skews of 200ps, the MPC942 is ideal as a clock distribution chip for the most demanding of synchronous systems. The 2.5V outputs also make the device ideal for supplying clocks for a high performance Pentium II™ microprocessor based design.

- LVPECL Clock Input
- 2.5V LVCMOS Outputs for Pentium II Microprocessor Support
- 200ps Maximum Targeted Output–to–Output Skew
- Maximum Output Frequency of 250MHz @ 3.3 $V_{CC}$
- 32–Lead LQFP Packaging
- Single 3.3V or 2.5V Supply

**FA SUFFIX**
32–LEAD LQFP PACKAGE
CASE 873A–02

With a low output impedance (≈12Ω), in both the HIGH and LOW logic states, the output buffers of the MPC942 are ideal for driving series terminated transmission lines. With an output impedance of 12Ω the MPC942 can drive two series terminated transmission lines from each output. This capability gives the MPC942 an effective fanout of 1:36. The MPC942 provides enough copies of low skew clocks for most high performance synchronous systems.

The differential LVPECL inputs of the MPC942P allow the device to interface directly with a LVPECL fanout buffer like the MC100EP111 to build very wide clock fanout trees or to couple to a high frequency clock source. The OE pins will place the outputs into a high impedance state. The OE pin has an internal pullup resistor.

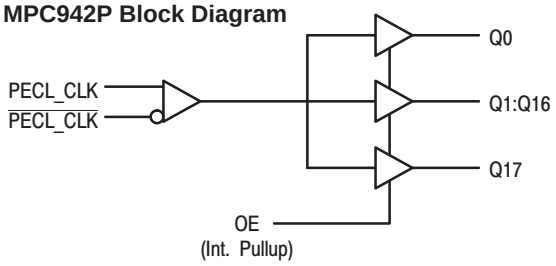
The MPC942 is a single supply device. The $V_{CC}$ power pins require either 2.5V or 3.3V. The 32–lead LQFP package was chosen to optimize performance, board space and cost of the device. The 32–lead LQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

Pentium II is a trademark of Intel Corporation.

**Rev 1**

## LOGIC DIAGRAM

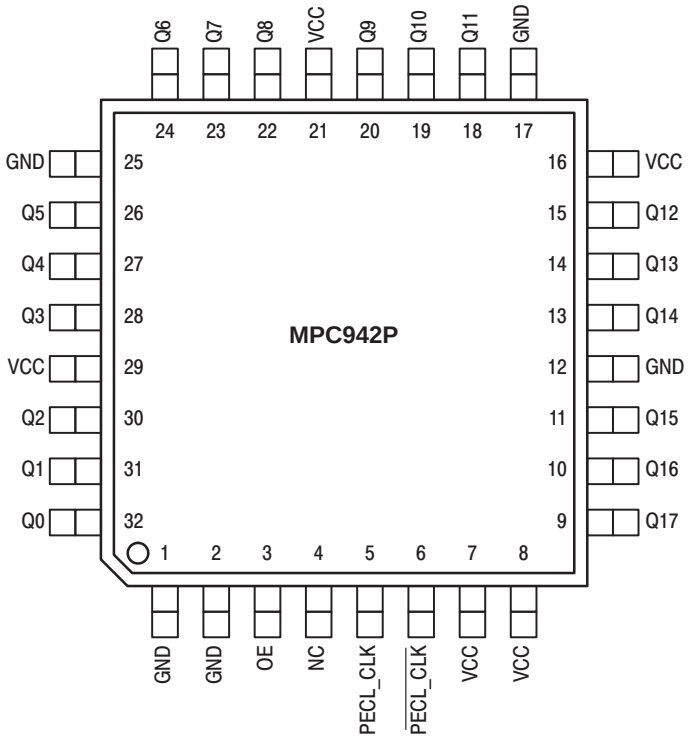
**MPC942P Block Diagram**




**FUNCTION TABLE**

| OE | Output |
|---|---|
| 0 | HIGH IMPEDANCE |
| 1 | OUTPUTS ENABLED |

**Pinout: 32–Lead** (Top View)




## ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 3.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | Input Current | | ±20 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 2.5V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | $V_{CC}$ | V | |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | |
| $V_{PP}$ | Input Swing PECL_CLK | 0.6 | | 1.0 | V | |
| $V_X$ | Input Crosspoint PECL_CLK | $V_{CC}$–1.0 | | $V_{CC}$–0.6 | V | |
| $V_{OH}$ | Output HIGH Voltage | 2.0 | | | V | $I_{OH}$ = –16 mA |
| $V_{OL}$ | Output LOW Voltage | | | 0.5 | V | $I_{OL}$ = 16 mA |
| $I_{IN}$ | Input Current | | | ±200 | µA | |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | |
| $C_{PD}$ | Power Dissipation Capacitance | | 14 | | pF | Per Output |
| $Z_{OUT}$ | Output Impedance | | 12 | | Ω | |
| $I_{CC}$ | Maximum Quiescent Supply Current | | 0.5 | 5.0 | mA | |

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 2.5V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $F_{max}$ | Maximum Frequency | | | 200 | MHz | |
| $t_{PLH}$ | Propagation Delay | 1.8 | | 4.0 | ns | |
| $t_{PHL}$ | Propagation Delay | 2.0 | | 4.3 | ns | |
| $t_{sk(o)}$ | Output–to–Output Skew | | | 200 | ps | |
| $t_{sk(pr)}$ | Part–to–Part Skew | | | 2.2 | ns | Note 2 |
| $t_{sk(pr)}$ | Part–to–Part Skew | | | 1.3 | ps | Note 1 |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.1 | | 1.0 | ns | |

1. For a specific temperature and voltage, includes output skew.
2. Across temperature and voltage ranges, includes output skew.

**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | 2.4 | | $V_{CC}$ | V | |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | |
| $V_{PP}$ | Input Swing PECL.CLK | 0.6 | | 1.0 | V | |
| $V_X$ | Input Crosspoint PECL_CLK | $V_{CC}$–1.0 | | $V_{CC}$–0.6 | V | |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | $I_{OH}$ = –20 mA |
| $V_{OL}$ | Output LOW Voltage | | | 0.6 | V | $I_{OL}$ = 20 mA |
| $I_{IN}$ | Input Current | | | ±200 | µA | |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | |
| $C_{PD}$ | Power Dissipation Capacitance | | 14 | | pF | Per Output |
| $Z_{OUT}$ | Output Impedance | | 12 | | Ω | |
| $I_{CC}$ | Maximum Quiescent Supply Current | | 0.5 | 5.0 | mA | |

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $F_{max}$ | Maximum Frequency | | | 250 | MHz | |
| $t_{PLH}$ | Propagation Delay | 1.5 | | 3.2 | ns | |
| $t_{PHL}$ | Propagation Delay | 1.5 | | 3.6 | ns | |
| $t_{sk(o)}$ | Output–to–Output Skew | | | 200 | ps | |
| $t_{sk(pr)}$ | Part–to–Part Skew | | | 1.7 | ns | Note 2 |
| $t_{sk(pr)}$ | Part–to–Part Skew | | | 1.0 | ps | Note 1 |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.1 | | 1.0 | ns | |

1. For a specific temperature and voltage, includes output skew.
2. Across temperature and voltage ranges, includes output skew.

*Product Preview*

# 2.5V and 3.3V LVCMOS Clock Fanout Buffer

# MPC9443

**LOW VOLTAGE SUPPLY 2.5V AND 3.3V LVCMOS CLOCK FANOUT BUFFER**

**FA SUFFIX**
48–LEAD LQFP PACKAGE
CASE 932–03

5

The MPC9443 is a 2.5V and 3.3V compatible 1:16 clock distribution buffer designed for low-voltage high-performance telecom, networking and computing applications. The device supports 3.3V, 2.5V and dual supply voltage (mixed-voltage) applications. The MPC9443 offers 16 low-skew outputs which are divided into 4 individually configurable banks. Each output bank can be individually supplied by 2.5V or 3.3V, individually set to run at 1X or 1/2X of the input clock frequency or be disabled (logic low output state). Two selectable LVPECL compatible inputs support differential clock distribution systems. In addition, one selectable LVCMOS input is provided for LVCMOS clock distribution systems. The MPC9443 is specified for the extended temperature range of –40 to +85°C.

**Features**

- Configurable 16 outputs LVCMOS clock distribution buffer
- Compatible to single, dual and mixed 3.3V/2.5V voltage supply
- Output clock frequency up to 250 MHz
- Designed for high-performance telecom, networking and computer applications
- Supports applications requiring clock redundancy
- Max. output skew of 200 ps (100 ps within one bank)
- Selectable output configurations per output bank
- Individually per-bank high–impedance tristate
- Output disable (stop in logic low state) control
- 48 ld LQFP package
- Ambient operating temperature range of –40 to 85°C

**Functional Description**

The MPC9443 is a full static design supporting clock frequencies up to 250 MHz. The signals are generated and retimed on-chip to ensure minimal skew between the three output banks.

Two independent LVPECL compatible clock inputs are available. This feature supports redundant differential clock sources. In addition, the MPC9443 supports single-ended LVCMOS clock distribution systems. Each of the four output banks can be individually supplied by 2.5V or 3.3V, supporting mixed voltage applications. The FSELx pins choose between division of the input reference frequency by one or two. The frequency divider can be set individually for each output bank. The MPC9443 output banks are high–impedance tristated by deasserting the $\overline{OE}_N$ pins. Asserting $\overline{OE}_N$ will the enable output banks. Please see Output Tristate Control on page 3 for details. The outputs can be synchronously stopped (logic low state). The outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9443 outputs can drive one or two traces giving the devices an effective fanout of 1:32. The device is packaged in a 7x7 $mm^2$ 48-lead LQFP package

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.
**Rev 0**

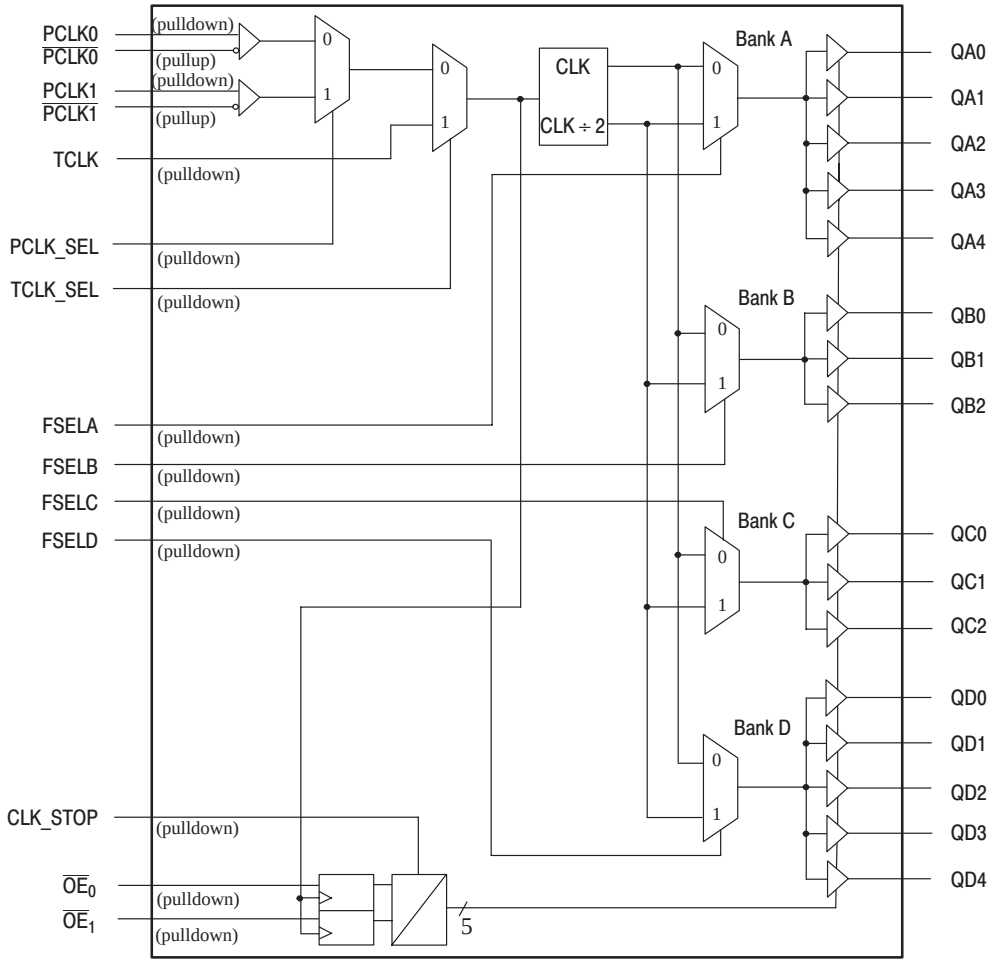



**Figure 1. MPC9443 Logic Diagram**

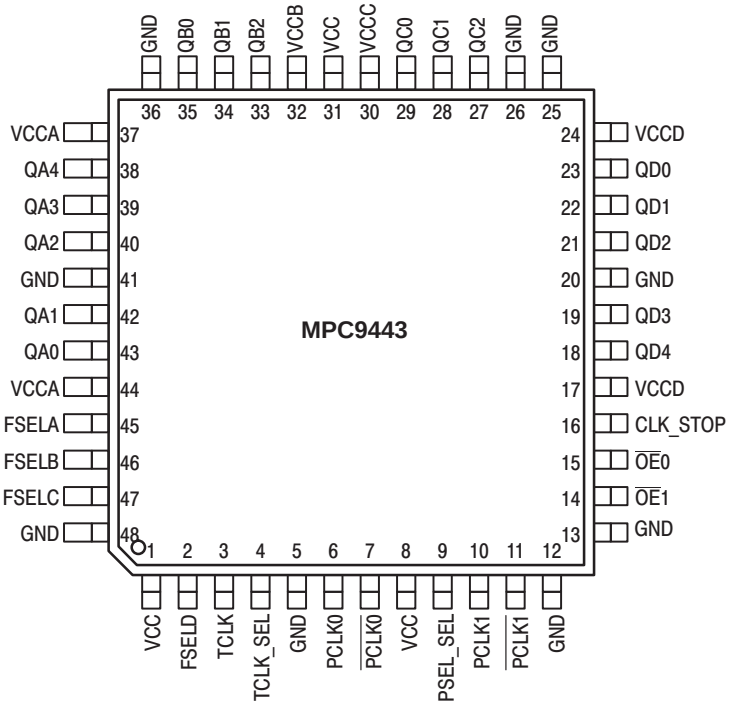



**Figure 2. 48–Lead Package Pinout** (Top View)

**Table 1: Pin Configuration**

| Pin | I/O | Type | Function |
|---|---|---|---|
| TCLK | Input | LVCMOS | LVCMOS clock inputs |
| PCLK0, $\overline{PCLK0}$ | Input | LVCMOS | LVPECL differential clock input |
| PCLK1, $\overline{PCLK1}$ | Input | LVCMOS | LVPECL differential clock input |
| $FSEL_A$, $FSEL_B$, $FSEL_C$, $FSEL_D$ | Input | LVCMOS | Output bank divide select input |
| TCLK_SEL | Input | LVCMOS | LVCMOS/LVPECL clock input select |
| PCLK_SEL | Input | LVCMOS | PCLK0/PCLK1 clock input select |
| $\overline{OE}_0$, $\overline{OE}_1$ | Input | LVCMOS | Output tristate control |
| CLK_STOP | Input | LVCMOS | Synchronous output enable/disable (clock stop) control |
| GND | | Supply | Negative voltage supply |
| $V_{CCA}$, $V_{CCB}$, $V_{CCC}$, $V_{CCD}$ | | Supply | Positive voltage supply output bank (VCC) |
| $V_{CC}$ | | Supply | Positive voltage supply core (VCC) |
| QA0 to QA4 | Output | LVCMOS | Bank A outputs |
| QB0 to QB2 | Output | LVCMOS | Bank B outputs |
| QC0 to QC2 | Output | LVCMOS | Bank C outputs |
| QD0 to QD4 | Output | LVCMOS | Bank D outputs |

**Table 2: Supported Single and Dual Supply Configurations**

| Supply voltage configuration | $V_{CC}$[a] | $V_{CCA}$[b] | $V_{CCB}$[c] | $V_{CCC}$[d] | $V_{CCD}$[e] | GND |
|---|---|---|---|---|---|---|
| 3.3V supply | 3.3V | 3.3V | 3.3V | 3.3V | 3.3V | 0 V |
| Mixed mode supply | 3.3V | 3.3V or 2.5V | 3.3V or 2.5V | 3.3V or 2.5V | 3.3V or 2.5V | 0 V |
| 2.5V supply | 2.5V | 2.5V | 2.5V | 2.5V | 2.5V | 0 V |

a. $V_{CC}$ is the positive power supply of the device core and input circuitry. $V_{CC}$ voltage defines the input threshold and levels
b. $V_{CCA}$ is the positive power supply of the bank A outputs. $V_{CCA}$ voltage defines bank A output levels
c. $V_{CCB}$ is the positive power supply of the bank B outputs. $V_{CCB}$ voltage defines bank B output levels
d. $V_{CCC}$ is the positive power supply of the bank C outputs. $V_{CCC}$ voltage defines bank C output levels
e. $V_{CCD}$ is the positive power supply of the bank D outputs. $V_{CCD}$ voltage defines bank D output levels

**Table 3: Function Table (Controls)**

| Control | Default | 0 | 1 |
|---|---|---|---|
| TCLK_SEL | 0 | TCLK active (LVCMOS clock mode) | PCLK or PCLK1 active (LVPECL clock mode) |
| PCLK_SEL | 0 | PCLK0 active, PCLK1 inactive | PCLK1 active, PCLK0 inactive |
| $FSEL_A$ | 0 | $f_{QA0:4} = f_{REF}$ | $f_{QA0:4} = f_{REF} \div 2$ |
| $FSEL_B$ | 0 | $f_{QB0:2} = f_{REF}$ | $f_{QB0:2} = f_{REF} \div 2$ |
| $FSEL_C$ | 0 | $f_{QC0:2} = f_{REF}$ | $f_{QC0:2} = f_{REF} \div 2$ |
| $FSEL_D$ | 0 | $f_{QD0:4} = f_{REF}$ | $f_{QD0:4} = f_{REF} \div 2$ |
| CLK_STOP | 0 | Normal operation | Outputs are synchronously disabled (stopped) in logic low state |
| $\overline{OE}_0$, $\overline{OE}_1$ | 00 | Asynchronous output enable control. See Table 4. $\overline{OE}_N$ | |

**Table 4: Output Tristate Control ($\overline{OE}_N$)[a]**

| $\overline{OE}_0$ | $\overline{OE}_1$ | QA0 to QA4 | QB0 to QB2 | QC0 to QC2 | QD0 to QD4 | Total number of enabled outputs |
|---|---|---|---|---|---|---|
| 0 | 0 | Enabled | Enabled | Enabled | Enabled | 16 |
| 0 | 1 | Enabled | Disabled (tristate) | Disabled (tristate) | Enabled | 10 |
| 1 | 0 | Enabled | Enabled | Disabled (tristate) | Disabled (tristate) | 8 |
| 1 | 1 | Disabled (tristate) | Disabled (tristate) | Disabled (tristate) | Disabled (tristate) | 0 |

a. $\overline{OE}_N$ will tristate (high impedance) output banks independent on the logic state of the output and the status of CLK_STOP.

**Table 5: Absolute Maximum Ratings[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 4.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -40 | 125 | °C | |

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

**Table 6: DC Characteristics ($V_{CC}$ = $V_{CCA}$ = $V_{CCB}$ = $V_{CCC}$ = $V_{CCD}$ = 3.3V ± 5%, $T_A$ = –40 to +85°C)[a]**

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | TCLK0, TCLK1 | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | TCLK0, TCLK1 | -0.3 | | 0.8 | V | LVCMOS |
| $I_{IN}$ | Input current[b] | | | | 120 | µA | |
| $C_{IN}$ | Input capacitance | | | 4.0 | | pF | |
| $V_{OH}$ | Output High Voltage | | 2.4 | | | V | $I_{OH}$=-24 mA[c] |
| $V_{OL}$ | Output Low Voltage | | | | 0.55<br>0.30 | V<br>V | $I_{OL}$= 24mA[c]<br>$I_{OL}$= 12mA |
| $V_{PP}$ | Peak-to-peak input voltage[d] | PCLK, $\overline{PCLK}$ | 500 | | 1000 | mV | LVPECL |
| $V_{CMR}$[e] | Common Mode Range | PCLK, $\overline{PCLK}$ | 1.2 | | $V_{CC}$-0.8 | V | LVPECL |
| $Z_{OUT}$ | Output impedance | | | 14 - 17 | | Ω | |
| $C_{PD}$ | Power Dissipation Capacitance | | | 10 | | pF | Per Output |
| $I_{CCI}$ | Maximum Core Supply Current | | | | | mA | $V_{CC}$ Pin |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | | 1.0 | mA | All $V_{CC}$ Pins |
| $V_{TT}$ | Output termination voltage | | | $V_{CC}$÷2 | | V | |

a. DC specifications are design targets, final specification is pending device characterization
b. Input pull-up / pull-down resistors influence input current
c. The MPC9443 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.
d. Pending characterization
e. $V_{CMR}$ is the difference from $V_{CC}$ and the crosspoint of the differential input signal. Normal operation is obtained when the “high” input is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ specification.

**Table 7: AC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = V_{CCD} = 3.3V \pm 5\%$, $T_A = –40$ to $+85°C$)[a b]**

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency | | 0 | | 250 | MHz | |
| $f_{MAX}$ | Maximum Output Frequency | ÷1 output<br>÷2 output | 0<br>0 | | 250<br>125 | MHz<br>MHz | FSELx=0<br>FSELx=1 |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | 50 | 60 | % | |
| $t_r$, $t_f$ | TCLK0, TCLK1 Input Rise/Fall Time | | | | 3.0 | ns | 0.8 to 2.0V |
| $t_{PLH}$<br>$t_{PHL}$<br>$t_{PLH}$<br>$t_{PHL}$ | Propagation delay | $PCLK_n$ to any Q<br>$PCLK_n$ to any Q<br>TTL_CLK to any Q<br>TTL_CLK to any Q | | | | ns | |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | | ns | |
| $t_S$, $t_H$ | Setup, hold time (reference clock to $\overline{OE}_X$) | | | | | ns | |
| $t_{sk(O)}$ | Output-to-output Skew | Within one bank<br>Any output | | | 100[b]<br>200[b] | ps<br>ps | |
| $t_{sk(PP)}$ | Device-to-device Skew | | | | | ps<br>ps | |
| $DC_O$ | Output Duty Cycle | ÷1 output<br>÷2 output | 45<br>48 | 50<br>50 | 55<br>52 | %<br>% | $DC_{REF}$ = 50%<br>$DC_{REF}$ = 25%-75% |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.55 to 2.4V |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$
b. AC specifications are design targets, final specification is pending device characterization

**Table 8: DC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = V_{CCD} = 2.5V \pm 5\%$, $T_A = –40$ to $+85°C$)[a]**

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | TCLK0, TCLK1 | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | TCLK0, TCLK1 | -0.3 | | 0.7 | V | LVCMOS |
| $I_{IN}$ | Input current[b] | | | | 120 | µA | |
| $C_{IN}$ | Input capacitance | | | 4.0 | | pF | |
| $V_{OH}$ | Output High Voltage | | 1.8 | | | V | $I_{OH}$= -15 mA[c] |
| $V_{OL}$ | Output Low Voltage | | | | 0.6 | V | $I_{OL}$= 15 mA[c] |
| $V_{PP}$ | Peak-to-peak input voltage | PCLK, $\overline{PCLK}$ | 500 | | 1000 | mV | LVPECL |
| $V_{CMR}$[d] | Common Mode Range | PCLK, $\overline{PCLK}$ | 1.1 | | $V_{CC}$-0.7 | V | LVPECL |
| $Z_{OUT}$ | Output impedance | | | 17 - 20 | | Ω | |
| $C_{PD}$ | Power Dissipation Capacitance | | | 10 | | pF | Per Output |
| $I_{CCI}$ | Maximum Core Supply Current | | | | | mA | $V_{CC}$ Pin |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | | 1.0 | mA | All $V_{CC}$ Pins |
| $V_{TT}$ | Output termination voltage | | | $V_{CC}$÷2 | | V | |

a. DC specifications are design targets, final specification is pending device characterization
b. Input pull-up / pull-down resistors influence input current
c. The MPC9443 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.
d. $V_{CMR}$ is the difference from $V_{CC}$ and the crosspoint of the differential input signal. Normal operation is obtained when the “high” input is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ specification.

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**Table 9: AC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = V_{CCD} = 2.5 \pm 5\%$, $T_A$ = –40 to +85°C)[a] [b]**

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency | | 0 | | 250 | MHz | |
| $f_{MAX}$ | Maximum Output Frequency | ÷1 output<br>÷2 output | 0<br>0 | | 250<br>125 | MHz<br>MHz | FSELx=0<br>FSELx=1 |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | 50 | 60 | % | |
| $t_r$, $t_f$ | Input Rise/Fall Time | TCLK0, TCLK1 | | | 3.0 | ns | 0.7 to 1.7V |
| $t_{PLH}$<br>$t_{PHL}$<br>$t_{PLH}$<br>$t_{PHL}$ | Propagation delay | $PCLK_n$ to any Q<br>$PCLK_n$ to any Q<br>TTL_CLK to any Q<br>TTL_CLK to any Q | | | | ns | |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | | ns | |
| $t_S$, $t_H$ | Setup, hold time (reference clock to $\overline{OE}_X$) | | | | | ns | |
| $t_{sk(O)}$ | Output-to-output Skew | Within one bank<br>Any output | | | 100[b]<br>200[b] | ps<br>ps | |
| $t_{sk(PP)}$ | Device-to-device Skew | | | | | ps<br>ps | |
| $DC_O$ | Output Duty Cycle | ÷1 output<br>÷2 output | 45<br>48 | 50<br>50 | 55<br>52 | %<br>% | $DC_{REF}$ = 50%<br>$DC_{REF}$ = 25%-75% |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.6 to 1.8V |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$
b. AC specifications are design targets, final specification is pending device characterization

**Table 10: DC Characteristics ($V_{CC} = 3.3V \pm 5\%$, any $V_{CCA,B,C,D} = 2.5V \pm 5\%$ or $3.3V \pm 5\%$ (mixed), $T_A$ = –40 to +85°C)[a]**

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | TCLK0, TCLK1 | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | TCLK0, TCLK1 | -0.3 | | 0.8 | V | LVCMOS |
| $I_{IN}$ | Input current[b] | | | | 120 | µA | |
| $C_{IN}$ | Input capacitance | | | 4.0 | | pF | |
| $V_{OH}$ | Output High Voltage | 2.5V output<br>3.3V output | 1.7<br>2.0 | | | V | $I_{OH}$= -15 mA[c]<br>$I_{OH}$= -24 mA[c] |
| $V_{OL}$ | Output Low Voltage | 2.5V output<br>3.3V output | | | 0.6<br>0.55 | V | $I_{OL}$= 15 mA[c]<br>$I_{OL}$= 24 mA[c] |
| $V_{PP}$ | Peak-to-peak input voltage | PCLK, $\overline{PCLK}$ | 500 | | 1000 | mV | LVPECL |
| $V_{CMR}$[d] | Common Mode Range | PCLK, $\overline{PCLK}$ | 1.2 | | $V_{CC}$-0.8 | V | LVPECL |
| $Z_{OUT}$ | Output impedance | 2.5V output<br>3.3V output | | 17 - 20<br>14 - 17 | | Ω<br>Ω | |
| $C_{PD}$ | Power Dissipation Capacitance | | | 10 | | pF | Per Output |
| $I_{CCI}$ | Maximum Core Supply Current | | | | | mA | $V_{CC}$ Pin |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | | 1.0 | mA | All $V_{CC}$ Pins |
| $V_{TT}$ | Output termination voltage | | | $V_{CC}$÷2 | | V | |

a. DC specifications are design targets, final specification is pending device characterization
b. Input pull-up / pull-down resistors influence input current
c. The MPC9443 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.
d. $V_{CMR}$ is the difference from $V_{CC}$ and the crosspoint of the differential input signal. Normal operation is obtained when the “high” input is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ specification.

**Table 11: AC Characteristics ($V_{CC}$ = 3.3V ± 5%, any $V_{CCA,B,C,D}$ = 2.5V ± 5% or 3.3V ± 5% (mixed), $T_A$ = –40 to +85°C)[a] [b]**

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency | | 0 | | 250 | MHz | |
| $f_{MAX}$ | Maximum Output Frequency | ÷1 output<br>÷2 output | 0<br>0 | | 250<br>125 | MHz<br>MHz | SELx=0<br>SELx=1 |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | | 60 | % | |
| $t_r$, $t_f$ | Input Rise/Fall Time | TCLK0, TCLK1 | | | 3.0 | ns | 0.8 to 2.4V |
| $t_{PLH}$<br>$t_{PHL}$<br>$t_{PLH}$<br>$t_{PHL}$ | Propagation delay | $PCLK_n$ to any Q<br>$PCLK_n$ to any Q<br>TTL_CLK to any Q<br>TTL_CLK to any Q | | | | ns | |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | | ns | |
| $t_S$, $t_H$ | Setup, hold time (reference clock to $\overline{OE}_X$) | | | | | ns | |
| $t_{sk(O)}$ | Output-to-output Skew | Within one bank<br>Any output | | | 150[b]<br>250[b] | ps<br>ps | |
| $t_{sk(PP)}$ | Device-to-device Skew | | | | | ps<br>ps | |
| $DC_O$ | Output Duty Cycle | ÷1 output<br>÷2 output | 45<br>48 | 50<br>50 | 55<br>52 | %<br>% | $DC_{REF}$ = 50%<br>$DC_{REF}$ = 25%-75% |
| $t_r$, $t_f$ | Output Rise/Fall Time | 2.5V output<br>3.3V output | 0.1<br>0.1 | | 1.0<br>1.0 | ns<br>ns | 0.60 to 1.8V<br>0.55 to 2.4V |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$
b. AC specifications are design targets, final specification is pending device characterization

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## APPLICATIONS INFORMATION

### Driving Transmission Lines

The MPC9443 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}$÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9443 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3“Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9443 clock driver is effectively doubled due to its capability to drive multiple lines.



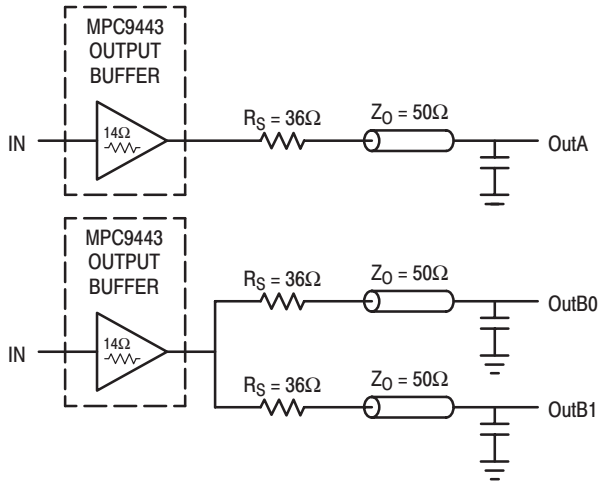



**Figure 3. Single versus Dual Transmission Lines**

The waveform plots in Figure 4“Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9443 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9443. The output waveform in Figure 4“Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S ( Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\Omega \parallel 50\Omega$$
$$R_S = 36\Omega \parallel 36\Omega$$
$$R_0 = 17\Omega$$
$$V_L = 3.0 ( 25 \div (18+17+25)$$
$$= 1.25V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

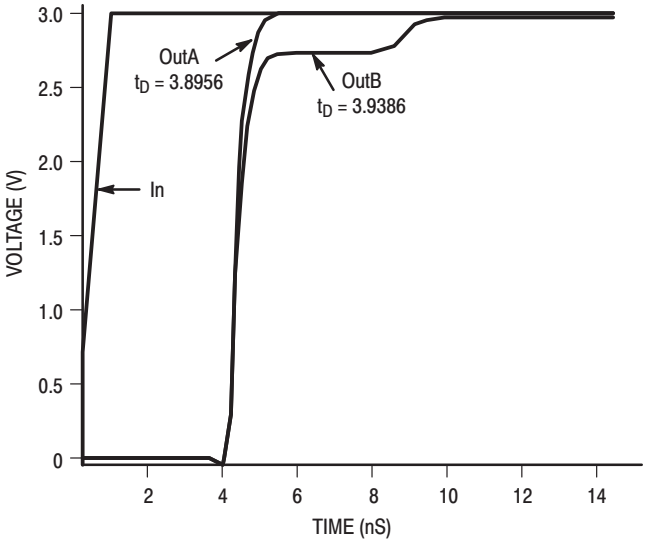
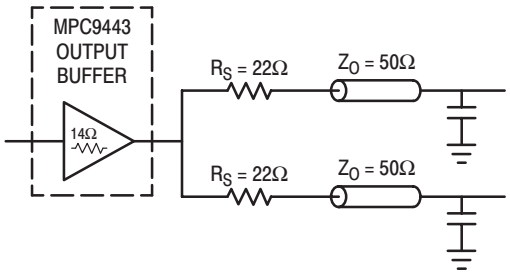



**Figure 4. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5“Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




14Ω + 22Ω || 22Ω = 50Ω || 50Ω
25Ω = 25Ω

**Figure 5. Optimized Dual Line Termination**

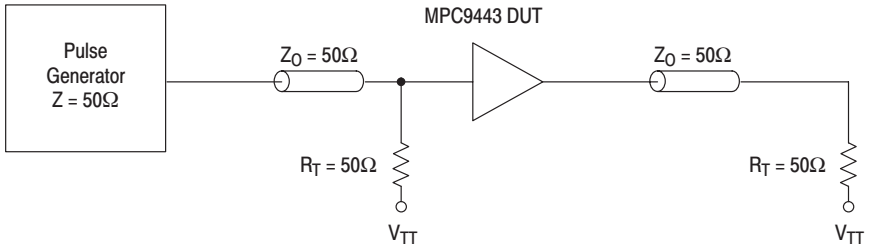



**Figure 6. TCLK MPC9443 AC test reference for $V_{cc}$ = 3.3V and $V_{cc}$ = 2.5V**

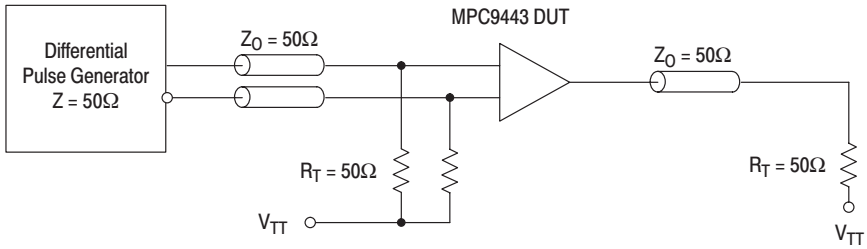
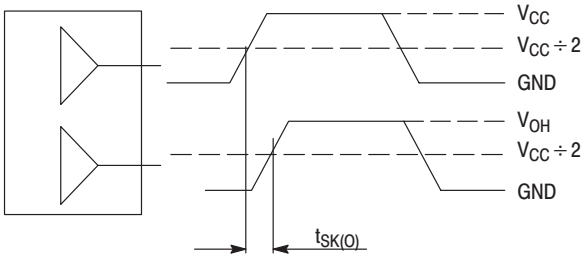



**Figure 7. PCLK0, PCLK1 MPC9443 AC test reference**




The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 8. Output–to–output Skew $t_{SK(O)}$**

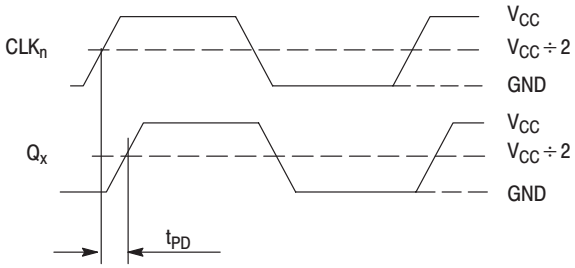
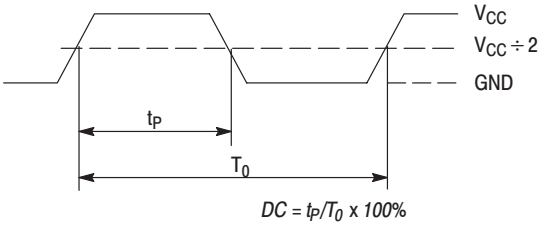



**Figure 9. Propagation delay ($t_{PD}$) test reference**




The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 10. Output Duty Cycle (DC)**

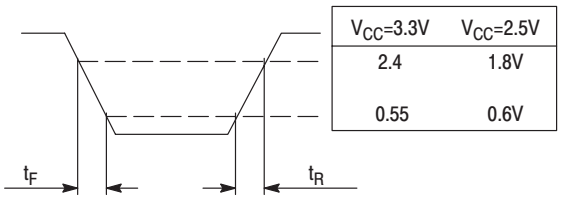



**Figure 11. Output Transition Time Test Reference**

*Product Preview*

# 2.5V and 3.3V LVCMOS Clock Fanout Buffer

**MPC9446**

**LOW VOLTAGE SINGLE OR DUAL SUPPLY 2.5V AND 3.3V LVCMOS CLOCK DISTRIBUTION BUFFER**

The MPC9446 is a 2.5V and 3.3V compatible 1:10 clock distribution buffer designed for low-voltage mid-range to high-performance telecom, networking and computing applications. Both 3.3V, 2.5V and dual supply voltages are supported for mixed-voltage applications. The MPC9446 offers 10 low-skew outputs and 2 selectable inputs for clock redundancy. The outputs are configurable and support 1:1 and 1:2 output to input frequency ratios. The MPC9446 is specified for the extended temperature range of –40 to 85°C.

**Features**

- Configurable 10 outputs LVCMOS clock distribution buffer
- Compatible to single, dual and mixed 3.3V/2.5V voltage supply
- Wide range output clock frequency up to 250 MHz
- Designed for mid-range to high-performance telecom, networking and computer applications
- Supports applications requiring clock redundancy
- Max. output skew of 200 ps (100 ps within one bank)
- Selectable output configurations per output bank
- Tristable outputs
- 32 ld LQFP package
- Ambient operating temperature range of –40 to 85°C

**FA SUFFIX**
LQFP PACKAGE
CASE 873A–02

**Functional Description**

The MPC9446 is a full static design supporting clock frequencies up to 250 MHz. The signals are generated and retimed on-chip to ensure minimal skew between the three output banks. Two independent LVCMOS compatible clock inputs are available. This feature supports redundant clock sources or the addition of a test clock into the system design. Each of the three output banks can be individually supplied by 2.5V or 3.3V supporting mixed voltage applications. The FSELx pins choose between division of the input reference frequency by one or two. The frequency divider can be set individually for each of the three output banks. The MPC9446 can be reset and the outputs are disabled by deasserting the $\overline{OE}$/MR pin (logic high state). Asserting $\overline{OE}$ will enable the outputs.

All inputs accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. Please consult the MPC9456 specification for a 1:10 mixed voltage buffer with LVPECL compatible inputs. For series terminated transmission lines, each of the MPC9446 outputs can drive one or two traces giving the devices an effective fanout of 1:20. The device is packaged in a 7x7 $mm^2$ 32-lead LQFP package.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.
**Rev 0**

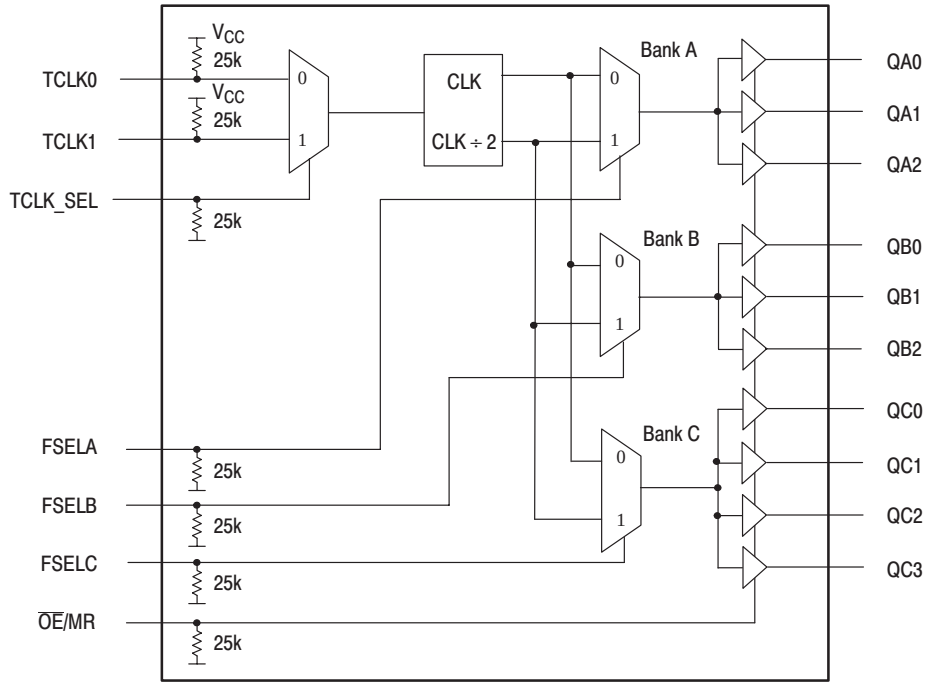



**Figure 1. MPC9446 Logic Diagram**

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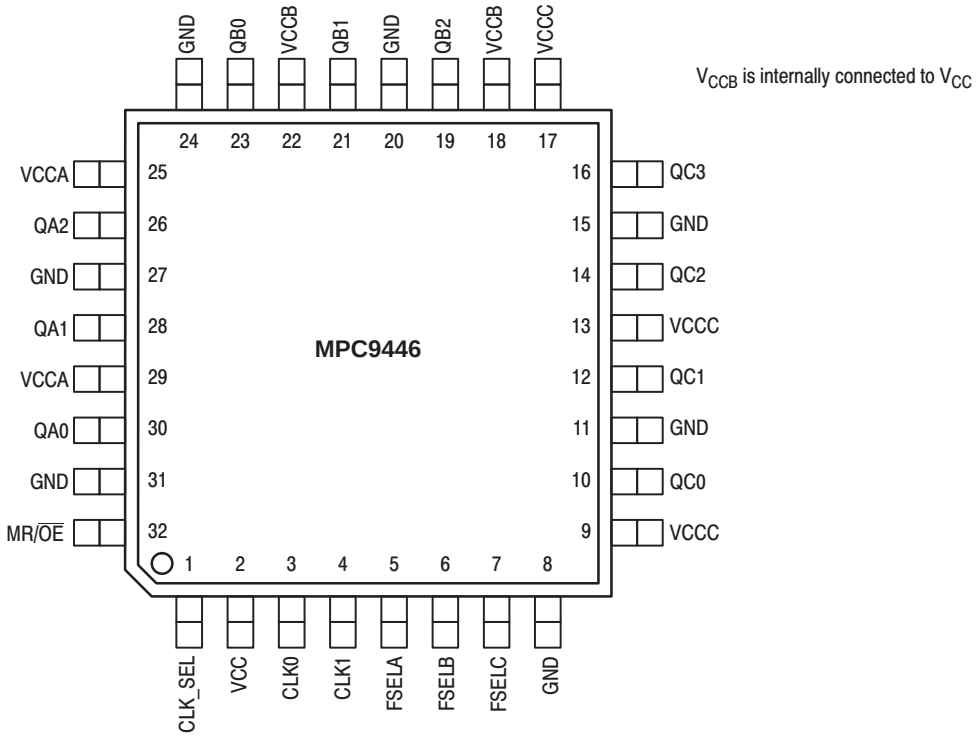



**Figure 2. Pinout: 32–Lead Package Pinout** (Top View)

**Table 1: Pin Configuration**

| Pin | I/O | Type | Function |
|---|---|---|---|
| CLK0:1 | Input | LVCMOS | LVCMOS clock inputs |
| FSELA, FSELB, FSELC | Input | LVCMOS | Output bank divide select input |
| MR/$\overline{OE}$ | Input | LVCMOS | Internal reset and output tristate control |
| GND | | Supply | Negative voltage supply output bank (GND) |
| VCCA, VCCB*, VCCC | | Supply | Positive voltage supply for output banks |
| VCC | | Supply | Positive voltage supply core (VCC) |
| QA0 - QA2 | Output | LVCMOS | Bank A outputs |
| QB0 - QB2 | Output | LVCMOS | Bank B outputs |
| QC0 - QC3 | Output | LVCMOS | Bank C outputs |

* $V_{CCB}$ is internally connected to $V_{CC}$.

**Table 2: Supported Single and Dual Supply Configurations**

| Supply voltage configuration | $V_{CC}$[a] | $V_{CCA}$[b] | $V_{CCB}$[c] | $V_{CCC}$[d] | GND |
|---|---|---|---|---|---|
| 3.3V | 3.3V | 3.3V | 3.3V | 3.3V | 0V |
| Mixed voltage supply | 3.3V | 3.3V or 2.5V | 3.3V | 3.3V or 2.5V | 0 V |
| 2.5V | 2.5V | 2.5V | 2.5V | 2.5V | 0 V |

a. $V_{CC}$ is the positive power supply of the device core and input circuitry. $V_{CC}$ voltage defines the input threshold and levels
b. $V_{CCA}$ is the positive power supply of the bank A outputs. $V_{CCA}$ voltage defines bank A output levels
c. $V_{CCB}$ is the positive power supply of the bank B outputs. $V_{CCB}$ voltage defines bank B output levels. $V_{CCB}$ is internally connected to $V_{CC}$.
d. $V_{CCC}$ is the positive power supply of the bank C outputs. $V_{CCC}$ voltage defines bank C output levels

**Table 3: Function Table (Controls)**

| Control | Default | 0 | 1 |
|---|---|---|---|
| CLK_SEL | 0 | TCLK0 | TCLK1 |
| FSELA | 0 | $f_{QA0:2} = f_{REF}$ | $f_{QA0:2} = f_{REF} \div 2$ |
| FSELB | 0 | $f_{QB0:2} = f_{REF}$ | $f_{QB0:2} = f_{REF} \div 2$ |
| FSELC | 0 | $f_{QC0:3} = f_{REF}$ | $f_{QC0:3} = f_{REF} \div 2$ |
| MR/$\overline{OE}$ | 0 | Outputs enabled | Internal reset Outputs disabled (tristate) |

**Table 4: Absolute Maximum Ratings[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 4.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -40 | 125 | °C | |

a. Absolute maximum continuos ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

**Table 5: DC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC}$ = 3.3V ± 5%, $T_A$ = –40 to +85°C)**[a]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | TCLK0, TCLK1 | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | TCLK0, TCLK1 | -0.3 | | 0.8 | V | LVCMOS |
| $I_{IN}$ | Input Current[b] | | | | 120 | µA | |
| $C_{IN}$ | Input Capacitance | | | 4.0 | | pF | |
| $V_{OH}$ | Output High Voltage | | 2.4 | | | V | $I_{OH}$=-24 mA[c] |
| $V_{OL}$ | Output Low Voltage | | | | 0.55<br>0.30 | V<br>V | $I_{OL}$= 24mA[c]<br>$I_{OL}$= 12mA |
| $Z_{OUT}$ | Output Impedance | | | 14 - 17 | | W | |
| $C_{PD}$ | Power Dissipation Capacitance | | | 10 | | pF | Per Output |
| $I_{CC}$ | Maximum Core Supply Current | | | | | mA | $V_{CC}$ Pins |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | | 1.0 | mA | All $V_{CCx}$ Pins |
| $V_{TT}$ | Output Termination Voltage | | | $V_{CC}$÷2 | | V | |

a. AC specifications are design targets, final specification is pending device characterization
b. Input pull-up / pull-down resistors influence input current
c. The MPC9446 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

**Table 6: AC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC}$ = 3.3V ± 5%, $T_A$ = –40 to +85°C)**[a] [b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency | | 0 | | 250 | MHz | |
| $f_{MAX}$ | Maximum Output Frequency | ÷1 output<br>÷2 output | 0<br>0 | | 250<br>125 | MHz<br>MHz | FSELx=0<br>FSELx=1 |
| $f_{refDC}$ | Reference Input Duty Cycle | | 25 | | 75 | % | |
| $t_r$, $t_f$ | TCLK0, TCLK1 Input Rise/Fall Time | | | | 3.0 | ns | 0.8 to 2.0V |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay | CLK to any Q<br>CLK to any Q | | | | ns | |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | | ns | |
| $t_{sk(O)}$ | Output-to-output Skew | Within one bank<br>Any output | | | 100[b]<br>200[b] | ps<br>ps | |
| $t_{sk(PP)}$ | Device-to-device Skew | | | | | ps<br>ps | |
| $DC_Q$ | Output Duty Cycle | ÷1 output<br>÷2 output | 45<br>48 | 50<br>50 | 55<br>52 | %<br>% | $DC_{REF}$ = 50%<br>$DC_{REF}$ = 25%-75% |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.55 to 2.4V |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$
b. AC specifications are design targets, final specification is pending device characterization

5

**Table 7: DC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC}$ = 2.5V ± 5%, $T_A$ = –40 to +85°C)**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | -0.3 | | 0.7 | V | LVCMOS |
| $V_{OH}$ | Output High Voltage | 1.8 | | | V | $I_{OH}$=-15 mA[a] |
| $V_{OL}$ | Output Low Voltage | | | 0.6 | V | $I_{OL}$= 15 mA |
| $Z_{OUT}$ | Output Impedance | | 17 - 20[b] | | W | |
| $I_{IN}$ | Input Current | | | | µA | |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | |
| $C_{PD}$ | Power Dissipation Capacitance | | 10 | | pF | Per Output |
| $I_{CC}$ | Maximum Core Supply Current | | | | mA | $V_{CC}$ Pin |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CCx}$ Pins |
| $V_{TT}$ | Output Termination Voltage | | $V_{CC}$÷2 | | V | |

a. The MPC9446 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.

**Table 8: AC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC}$ = 2.5 ± 5%, $T_A$ = –40 to +85°C)[a] [b]**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency | 0 | 250 | | MHz | |
| $f_{MAX}$ | Maximum Output Frequency ÷1 output<br>÷2 output | 0<br>0 | 250<br>125 | | MHz<br>MHz | FSELx=0<br>FSELx=1 |
| $f_{refDC}$ | Reference Input Duty Cycle | 25 | | 75 | % | |
| $t_r$, $t_f$ | TCLK0, TCLK1 Input Rise/Fall Time | | | 3.0 | ns | 0.7 to 1.7V |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay CLK to any Q<br>CLK to any Q | | | | ns | |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | ns | |
| $t_{sk(O)}$ | Output-to-output Skew Within one bank<br>Any output | | 100[b]<br>200[b] | | ps<br>ps | |
| $t_{sk(PP)}$ | Device-to-device Skew | | | | ps<br>ps | |
| $DC_O$ | Output Duty Cycle ÷1 output<br>÷2 output | 45<br>48 | 50<br>50 | 55<br>52 | %<br>% | $DC_{REF}$ = 50%<br>$DC_{REF}$ = 25%-75% |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.1 | | 1.0 | ns | 0.6 to 1.8V |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$
b. AC specifications are design targets, final specification is pending device characterization

**Table 9: AC Characteristics ($V_{CC}$ = 3.3V ± 5%, any $V_{CCA,B,C,D}$ = 2.5V ± 5% or 3.3V ± 5% (mixed), $T_A$ = –40 to +85°C)[a] [b] [c]**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $t_{sk(O)}$ | Output-to-output Skew Within one bank<br>Any output | | | | ps<br>ps | |
| $t_{sk(PP)}$ | Device-to-device Skew | | | | ps<br>ps | |
| $DC_O$ | Output Duty Cycle ÷1 output<br>÷2 output | 45<br>48 | 50<br>50 | 55<br>52 | %<br>% | $DC_{REF}$ = 50%<br>$DC_{REF}$ = 25%-75% |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$
b. AC specifications are design targets, final specification is pending device characterization
c. For all other AC specifications, refer to 2.5V or 3.3V tables according to the supply voltage of the output bank

## APPLICATIONS INFORMATION

### Driving Transmission Lines

The MPC9446 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}$÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9446 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3“Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9446 clock driver is effectively doubled due to its capability to drive multiple lines.

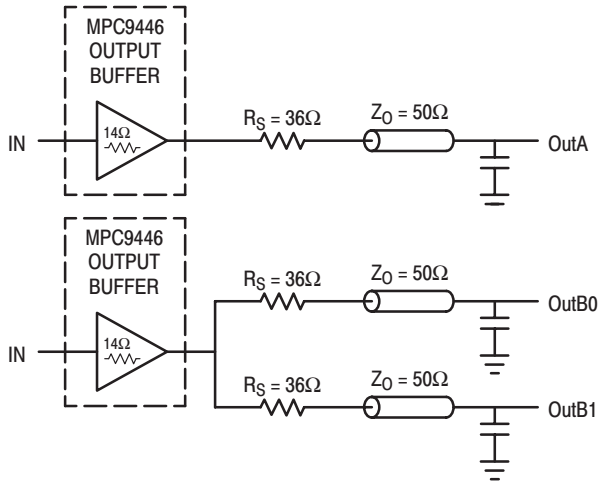



**Figure 3. Single versus Dual Transmission Lines**

The waveform plots in Figure 4“Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9446 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9446. The output waveform in Figure 4“Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S ( Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\Omega \parallel 50\Omega$$
$$R_S = 36\Omega \parallel 36\Omega$$
$$R_0 = 17\Omega$$
$$V_L = 3.0 ( 25 \div (18+17+25)$$
$$= 1.25V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

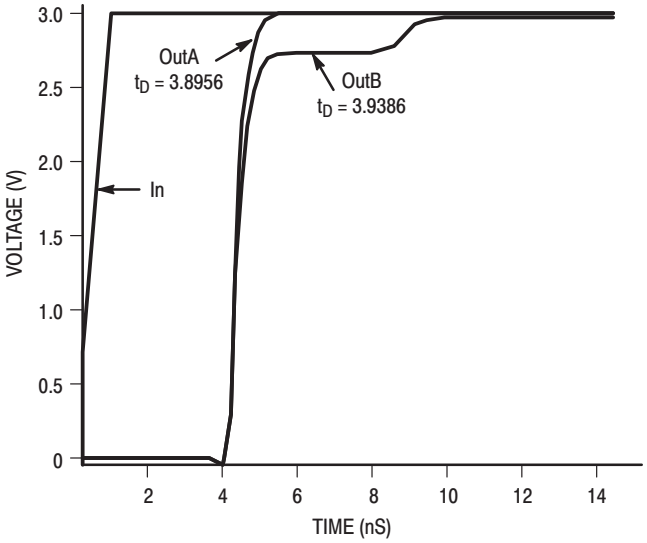
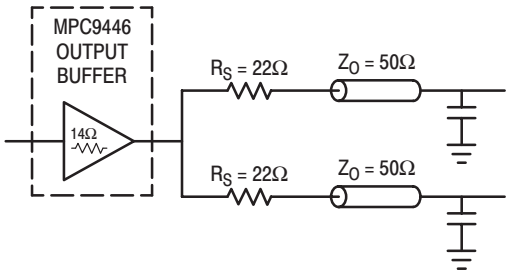



**Figure 4. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5“Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




$14\Omega + 22\Omega \parallel 22\Omega = 50\Omega \parallel 50\Omega$
$25\Omega = 25\Omega$

**Figure 5. Optimized Dual Line Termination**

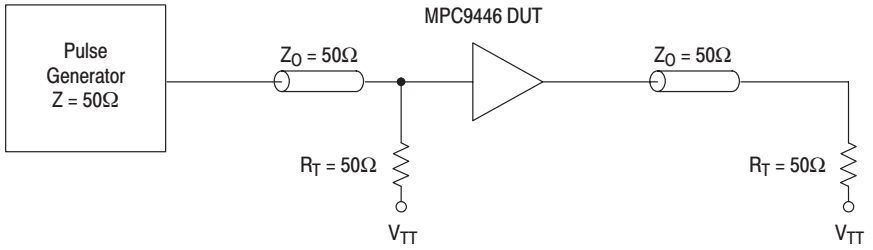



**Figure 6. TCLK0, TCLK1 MPC9446 AC test reference for $V_{cc}$ = 3.3V and $V_{cc}$ = 2.5V**

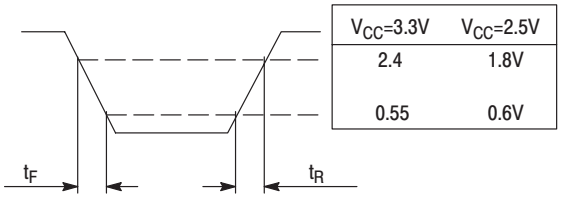



**Figure 7. Output Transition Time Test Reference**

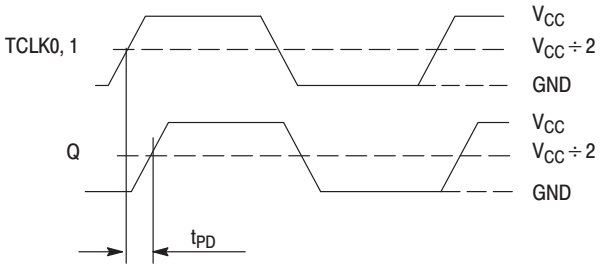
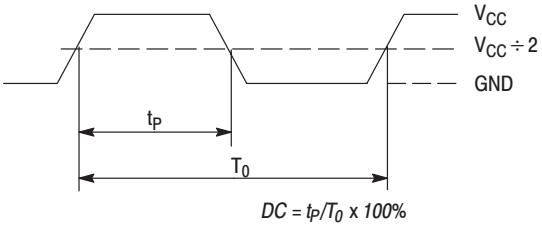


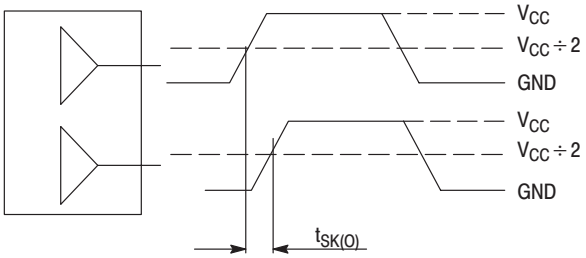

**Figure 8. Propagation delay ($t_{PD}$) test reference**

5




The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 9. Output Duty Cycle (DC)**




The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 10. Output–to–output Skew $t_{SK(O)}$**

**Order Number: MPC9447/D**
**Rev 0, 11/2001**

*Preliminary Information*

# 3.3V/2.5V 1:9 LVCMOS Clock Fanout Buffer

**MPC9447**

**LOW VOLTAGE**
**3.3 V/2.5 V LVCMOS 1:9**
**CLOCK FANOUT BUFFER**

**FA SUFFIX**
32–LEAD LQFP PACKAGE
CASE 873A

5

The MPC9447 is a 3.3V or 2.5V compatible, 1:9 clock fanout buffer targeted for high performance clock tree applications. With output frequencies up to 275[1] MHz and output skews less than 150 ps[1], the device meets the needs of most demanding clock applications.

**Features**

- 9 LVCMOS Compatible Clock Outputs
- 2 Selectable, LVCMOS Compatible Inputs
- Maximum Clock Frequency of 275[1] MHz
- Maximum Clock Skew of 150 ps[1]
- Synchronous Output Stop in Logic Low State Eliminates Output Runt Pulses
- High–Impedance Output Control
- 3.3V or 2.5V Power Supply
- Drives up to 18 Series Terminated Clock Lines
- Ambient Temperature Range –40°C to +85°C
- 32 Lead LQFP Packaging
- Supports Clock Distribution in Networking, Telecommunications, and Computer Applications
- Pin and Function Compatible to MPC947

**Functional Description**

MPC9447 is specifically designed to distribute LVCMOS compatible clock signals up to a frequency of 275[1] MHz. Each output provides a precise copy of the input signal with a near zero skew. The outputs buffers support driving of 50Ω terminated transmission lines on the incident edge: each is capable of driving either one parallel terminated or two series terminated transmission lines.

Two selectable independent LVCMOS compatible clock inputs are available, providing support of redundant clock source systems. The MPC9447 CLK_STOP control is synchronous to the falling edge of the input clock. It allows the start and stop of the output clock signal only in a logic low state, thus eliminating potential output runt pulses. Applying the OE control will force the outputs into high–impedance mode.

All inputs have an internal pull–up or pull–down resistor preventing unused and open inputs from floating. The device supports a 2.5V or 3.3V power supply and an ambient temperature range of –40°C to +85°C. The MPC9447 is pin and function compatible but performance–enhanced to the MPC947.



1. Final specification of this parameter is pending characterization.



**Rev 0**

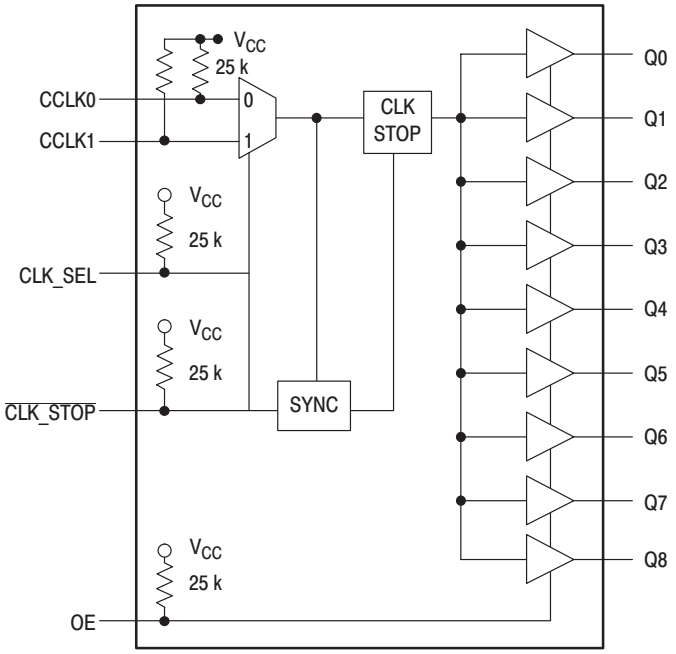



**Figure 1. Logic Diagram**

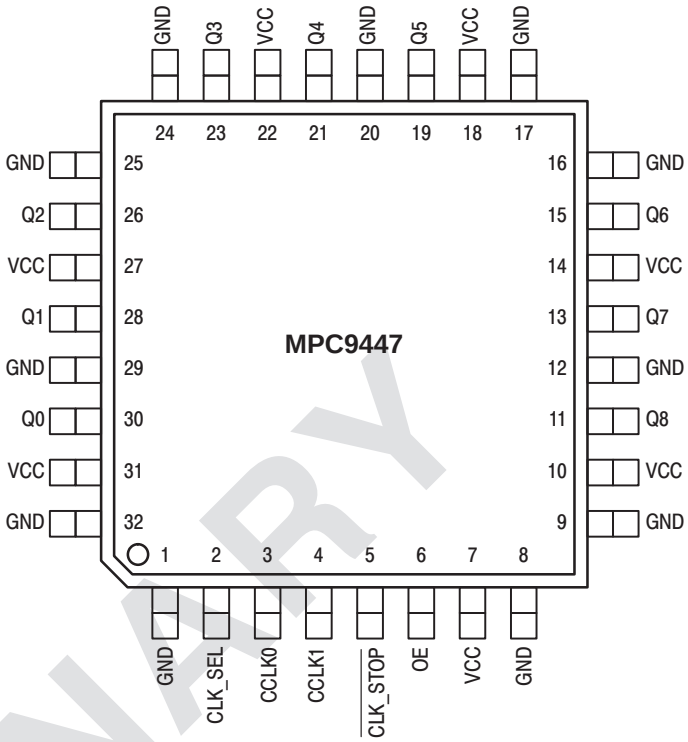



**Figure 2. 32–Lead Pinout** (Top View)

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**Table 1. Function Table**

| Control | Default | 0 | 1 |
|---|---|---|---|
| CLK_SEL | 1 | CLK0 input selected | CLK1 input selected |
| OE | 1 | Outputs disabled (high–impedance state)[a] | Outputs enabled |
| $\overline{\text{CLK\_STOP}}$ | 1 | Outputs synchronously stopped in logic low state | Outputs active |

a. OE = 0 will high–impedance tristate all outputs independent on $\overline{\text{CLK\_STOP}}$

**Table 2. Pin Configuration**

| Pin | I/O | Type | Function |
|---|---|---|---|
| CCLK0 | Input | LVCMOS | Clock signal input |
| CCLK1 | Input | LVCMOS | Alternative clock signal input |
| CLK_SEL | Input | LVCMOS | Clock input select |
| $\overline{\text{CLK\_STOP}}$ | Input | LVCMOS | Clock output enable/disable |
| OE | Input | LVCMOS | Output enable/disable (high–impedance tristate) |
| Q0–8 | Output | LVCMOS | Clock outputs |
| GND | Supply | Ground | Negative power supply (GND) |
| $V_{CC}$ | Supply | $V_{CC}$ | Positive power supply for I/O and core. All $V_{CC}$ pins must be connected to the positive power supply for correct operation |

**Table 3. General Specifications**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output termination voltage | | $V_{CC} \div 2$ | | V | |
| MM | ESD protection (Machine model) | 200 | | | V | |
| HBM | ESD protection (Human body model) | 2000 | | | V | |
| LU | Latch-up immunity | 200 | | | mA | |
| $C_{PD}$ | Power dissipation capacitance | | 10 | | pF | Per output |
| $C_{IN}$ | Input capacitance | | 4.0 | | pF | Inputs |

**Table 4. Absolute Maximum Ratings[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -65 | 125 | °C | |

a. Absolute maximum continuos ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 5. DC Characteristics** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = 40°C to +85°C )

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | | | 0.8 | V | LVCMOS |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$ = -24 mA[a] |
| $V_{OL}$ | Output Low Voltage | | | 0.55<br>0.30 | V<br>V | $I_{OL}$ = 24 mA<br>$I_{OL}$ = 12 mA |
| $Z_{OUT}$ | Output impedance | | 14 - 17 | | W | |
| $I_{IN}$ | Input Current[b] | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a. The MPC9447 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.

b. Inputs have pull-down or pull-up resistors affecting the input current.

**Table 6. AC Characteristics** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40°C to +85°C)[a b]

| Symbol | 5Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | Output frequency | | 0 | | 275 | MHz | |
| $f_{ref}$ | Input Frequency | | 0 | | 275 | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | 50 | 60 | % | |
| $t_r$, $t_f$ | CCLK0, CCLK1 Input Rise/Fall Time | | | | 1.0 | ns | 0.8 to 2.0V |
| $t_{sk(O)}$ | Output-to-output Skew | | | | 150 | ps | |
| $t_{sk(PP)}$ | Device-to-device Skew | | | | TBD | ps | |
| $DC_Q$ | Output Duty Cycle | | 45 | 50 | 55 | % | $DC_{REF}$ = 50% |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | CCLK0 or CCLK1 to any Q | | | TBD | ns | |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 11 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 11 | ns | |
| $t_S$ | Setup time | CLK_STOP to CCLK0, 1[c] | TBD | | | ns | |
| $t_H$ | Hold time | CLK_STOP to CCLK0, 1[c] | TBD | | | ns | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.55 to 2.4V |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ) | | TBD | | ps | |

a. All AC characteristics are design targets and subject to change upon device characterization

b. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$

c. Setup and hold times are referenced to the falling edge of the selected clock signal input



5

**Table 7. DC Characteristics** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40°C to +85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | -0.3 | | 0.7 | V | LVCMOS |
| $V_{OH}$ | Output High Voltage | 1.8 | | | V | $I_{OH}$ =-15 mA[a] |
| $V_{OL}$ | Output Low Voltage | | | 0.6 | V | $I_{OL}$ = 15 mA |
| $Z_{OUT}$ | Output impedance | | 17 - 20 | | W | |
| $I_{IN}$ | Input Current[b] | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

a. The MPC9447 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.
b. Inputs have pull-down or pull-up resistors affecting the input current.

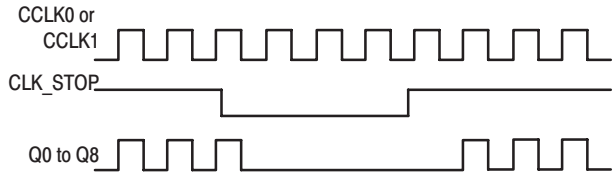
**Table 8. AC Characteristics** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40°C to +85°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | Output frequency | | 0 | | 275 | MHz | |
| $f_{ref}$ | Input Frequency | | 0 | | 275 | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | | 60 | % | |
| $t_r$, $t_f$ | CCLK0, CCLK1 Input Rise/Fall Time | | | | 1 | ns | 0.7 to 1.7V |
| $t_{sk(O)}$ | Output-to-output Skew[c] | | | | 150 | ps | |
| $t_{sk(PP)}$ | Device-to-device Skew | | | | TBD | ps | |
| $DC_Q$ | Output Duty Cycle | | 45 | 50 | 55 | % | $DC_{REF}$ = 50% |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | CCLK0 or CCLK1 to any Q | | | TBD | ns | |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 11 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | 11 | ns | |
| $t_S$ | Setup time | CLK_STOP to CCLK0[d] or CCLK1 | TBD | 0.0 | | ns | |
| $t_H$ | Hold time | CCLK0[c] or CCLK1 to CLK_STOP | TBD | 1.0 | | ns | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.6 to 1.8V |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ) | | TBD | | ps | |

a. All AC characteristics are design targets and subject to change upon device characterization
b. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$
c. See application section for part-to-part skew calculation
d. Setup and hold times are referenced to the falling edge of the selected clock signal input

## APPLICATION INFORMATION

**Figure 3. Output Clock Stop (CLK_STOP) Timing Diagram**




### Driving Transmission Lines

The MPC9447 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of 14Ω ($V_{CC}$ = 3.3 V) or 18Ω ($V_{CC}$ = 2.5V) the outputs can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC} \div 2$.

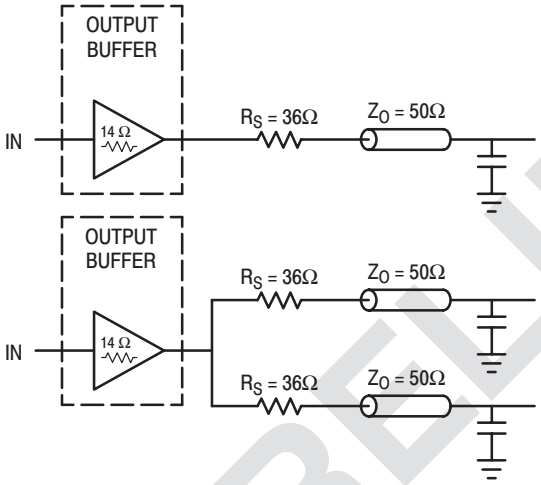



**Figure 4. Single versus Dual Transmission Lines**

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9447 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9447 clock driver is effectively doubled due to its capability to drive multiple lines. The waveform plots in figure 5 show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9447 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9447. The output waveform in figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

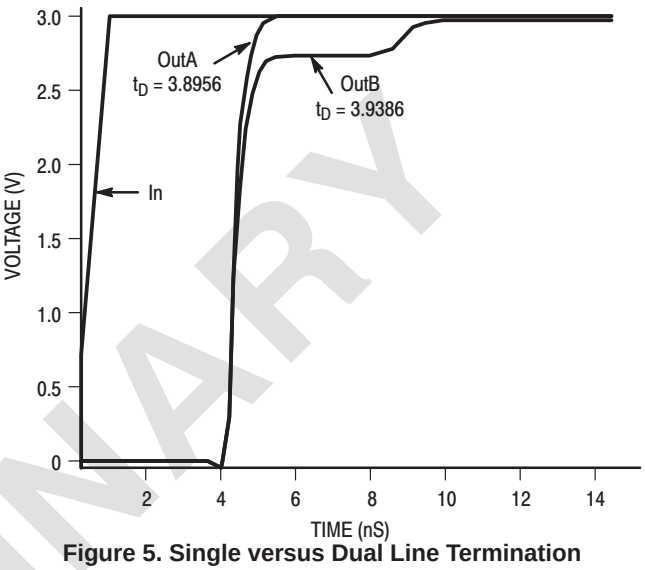



**Figure 5. Single versus Dual Line Termination Waveforms**

$V_L = V_S ( Z_0 \div (R_S + R_0 + Z_0))$

$Z_0 = 50\Omega \parallel 50\Omega$

$R_S = 22\Omega \parallel 22\Omega$

$R_0 = 14\Omega$

$V_L = 3.0 ( 25 \div (11 + 14 + 25) = 1.25V$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0 ns). Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

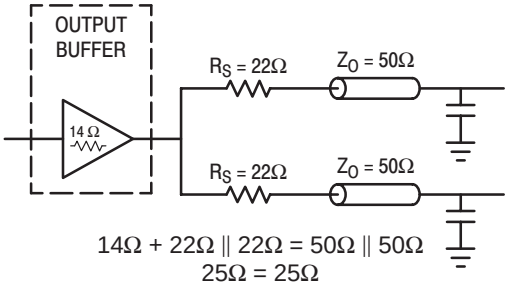



**Figure 6. Optimized Dual Line Termination**



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**Order Number: MPC9448/D**
**Rev 0, 11/2001**

*Product Preview*

# 3.3V/2.5V LVCMOS 1:12 Clock Fanout Buffer

**MPC9448**

**LOW VOLTAGE**
**3.3V/2.5V LVCMOS 1:12**
**CLOCK FANOUT BUFFER**

**FA SUFFIX**
32–LEAD LQFP PACKAGE
CASE 873A

The MPC9448 is a 3.3V or 2.5V compatible, 1:12 clock fanout buffer targeted for high performance clock tree applications. With output frequencies up to 275[1] MHz and output skews less than 150 ps[1], the device meets the needs of most demanding clock applications.

- 12 LVCMOS compatible clock outputs
- Selectable LVCMOS and differential LVPECL compatible clock inputs
- Maximum clock frequency of 275[1] MHz
- Maximum clock skew of 150 ps[1]
- Synchronous output stop in logic low state eliminates output runt pulses
- High–impedance output control
- 3.3V or 2.5V power supply
- Drives up to 24 series terminated clock lines
- Ambient temperature range –40°C to +85°C
- 32–Lead LQFP packaging
- Supports clock distribution in networking, telecommunication and computing applications
- Pin and function compatible to MPC948

5

**Functional Description**

The MPC9448 is specifically designed to distribute LVCMOS compatible clock signals up to a frequency of 275[1] MHz. Each output provides a precise copy of the input signal with a near zero skew. The outputs buffers support driving of 50Ω terminated transmission lines on the incident edge: each output is capable of driving either one parallel terminated or two series terminated transmission lines.

Two selectable, independent clock inputs are available, providing support of LVCMOS and differential LVPECL clock distribution systems. The MPC9448 CLK_STOP control is synchronous to the falling edge of the input clock. It allows the start and stop of the output clock signal only in a logic low state, thus eliminating potential output runt pulses. Applying the OE control will force the outputs into high–impedance mode.

All inputs have an internal pull–up or pull–down resistor preventing unused and open inputs from floating. The device supports a 2.5V or 3.3V power supply and an ambient temperature range of –40°C to +85°C. The MPC9448 is pin and function compatible but performance–enhanced to the MPC948.



1. Final specification of this parameter is pending characterization.


**Rev 0**

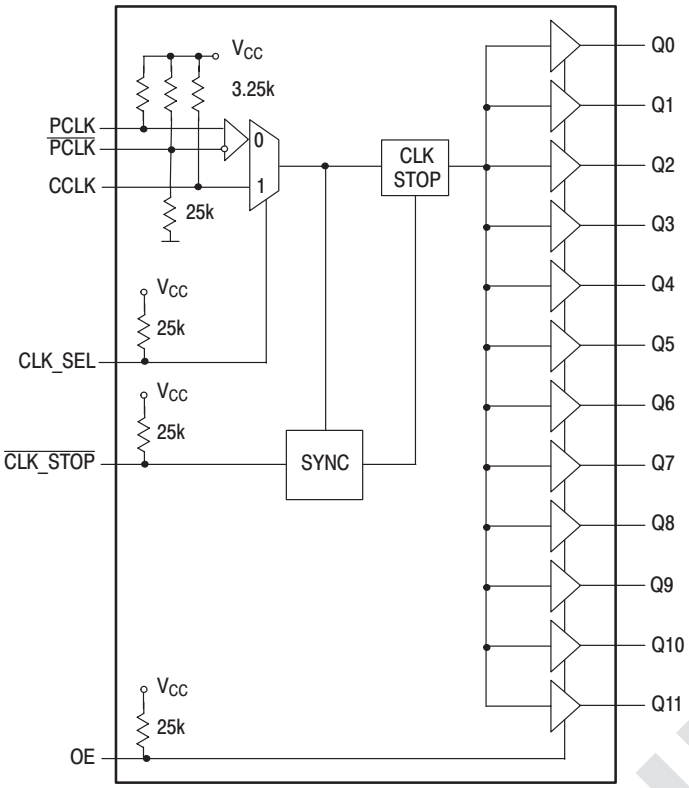


**Figure 1. Logic Diagram**

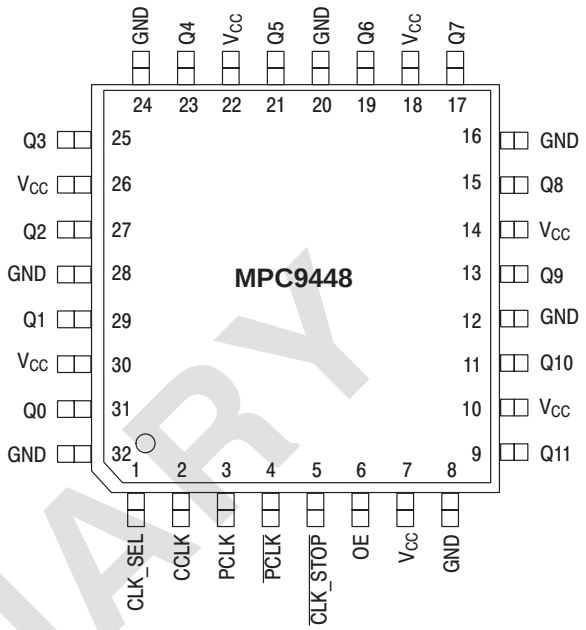


**Figure 2. 32–Lead Package Pinout**
(Top View)



**TABLE 1: FUNCTION TABLE**

| Control | Default | 0 | 1 |
|---|---|---|---|
| CLK_SEL | 1 | PECL differential input selected | CCLK input selected |
| OE | 1 | Outputs disabled (high-impedance state)[1] | Outputs enabled |
| $\overline{\text{CLK\_STOP}}$ | 1 | Outputs synchronously stopped in logic low state | Outputs active |

1. OE=0 will high-impedance tristate all outputs independent on $\overline{\text{CLK\_STOP}}$.

**TABLE 2: PIN CONFIGURATION**

| Pin | I/O | Type | Function |
|---|---|---|---|
| PCLK, $\overline{\text{PCLK}}$ | Input | LVCMOS | Clock signal input |
| CCLK | Input | LVCMOS | Alternative clock signal input |
| CLK_SEL | Input | LVCMOS | Clock input select |
| $\overline{\text{CLK\_STOP}}$ | Input | LVCMOS | Clock output enable/disable |
| OE | Input | LVCMOS | Output enable/disable (high–impedance tristate) |
| Q0–11 | Output | LVCMOS | Clock outputs |
| GND | Supply | Ground | Negative power supply (GND) |
| $V_{CC}$ | Supply | $V_{CC}$ | Positive power supply for I/O and core. All $V_{CC}$ pins must be connected to the positive power supply for correct operation |

**TABLE 3: GENERAL SPECIFICATIONS**

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output Termination Voltage | | $V_{CC} \div 2$ | | V | |
| MM | ESD Protection (Machine Model) | 200 | | | V | |
| HBM | ESD Protection (Human Body Model) | 2000 | | | V | |
| LU | Latch–up Immunity | 200 | | | mA | |
| $C_{pd}$ | Power Dissipation Capacitance | | 10 | | pF | Per Output |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | Inputs |

**TABLE 4: ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 3.6 | V |
| $V_{IN}$ | DC Input Voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $V_{OUT}$ | DC Output Voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | DC Input Current | | ±20 | mA |
| $I_{OUT}$ | DC Output Current | | ±50 | mA |
| $T_{Stor}$ | Storage Temperature Range | –65 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

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**TABLE 5: DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ±5%, $T_A$ = –40°C to +85°C)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | LVCMOS |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | $I_{OH}$ = –24mA[1] |
| $V_{PP}$ | Peak–to–Peak Input Voltage PCLK, $\overline{PCLK}$ | 250 | | | mV | LVPECL |
| $V_{CMR}$[2] | Common Mode Range PCLK, $\overline{PCLK}$ | 1.0 | | $V_{CC}$ – 0.6 | V | LVPECL |
| $V_{OL}$ | Output LOW Voltage | | | 0.55<br>0.30 | V<br>V | $I_{OL}$ = 24mA<br>$I_{OL}$ = 12mA |
| $Z_{OUT}$ | Output Impedance | | 14 – 17 | | Ω | |
| $I_{IN}$ | Input Current[3] | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | 1.0 | mA | All $V_{CC}$ Pins |

1. The MPC9448 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.
2. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (DC) specification.
3. Inputs have pull–down or pull–up resistors affecting the input current.

**TABLE 6: AC CHARACTERISTICS** ($V_{CC}$ = 3.3V ±5%, $T_A$ = –40°C to +85°C)[1, 2]

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{PP}$ | Peak–to–Peak Input Voltage | PCLK, $\overline{PCLK}$ | 500 | | 1000 | mV | LVPECL |
| $V_{CMR}$[3] | Common Mode Range | PCLK, $\overline{PCLK}$ | 1.2 | | $V_{CC}$ – 0.9 | V | LVPECL |
| $f_{max}$ | Maximum Output Frequency | | 0 | | 275 | MHz | |
| $f_{ref}$ | Maximum Input Frequency | | 0 | | 275 | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | 50 | 60 | % | |
| $t_r$, $t_f$ | CCLK Input Rise/Fall Time | | | | 1.0 | ns | 0.8V to 2.0V |
| $t_{sk(O)}$ | Output–to–Output Skew | | | | 150 | ps | |
| $t_{sk(PP)}$ | Device–to–Device Skew | | | | TBD | ps | |
| $DC_Q$ | Output Duty Cycle | | 45 | 50 | 55 | % | $DC_{REF}$ = 50% |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay | CCLK to any Q<br>PCLK to any Q | | | TBD | ns | |
| $t_{PLZ}$,$t_{PHZ}$ | Output Disable Time | OE to any Q | | | 11 | ns | |
| $t_{PZL}$,$t_{PLZ}$ | Output Enable Time | OE to any Q | | | 11 | ns | |
| $t_S$ | Setup Time | CLK_STOP to CCLK[4]<br>CLK_STOP to PCLK[4] | TBD<br>TBD | | | ns<br>ns | |
| $t_H$ | Hold Time | CLK_STOP to CCLK[4]<br>CLK_STOP to PCLK[4] | TBD<br>TBD | | | ns<br>ns | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.55V to 2.4V |
| $t_{JIT(CC)}$ | Cycle–to–Cycle Jitter | RMS (1 σ) | | TBD | | ps | |

1. All AC characteristics are design targets and subject to change upon device characterization.
2. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
3. $V_{CMR}$ (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ or $V_{PP}$ impacts static phase offset $t_{(\varnothing)}$.
4. Setup and Hold times are referenced to the falling edge of the selected clock signal input.

**TABLE 7: DC CHARACTERISTICS** ($V_{CC}$ = 2.5V ±5%, $T_A$ = –40°C to +85°C)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input LOW Voltage | | –0.3 | | 0.7 | V | LVCMOS |
| $V_{PP}$ | Peak–to–Peak Input Voltage | PCLK, $\overline{PCLK}$ | 250 | | | mV | LVPECL |
| $V_{CMR}$[1] | Common Mode Range | PCLK, $\overline{PCLK}$ | 1.0 | | $V_{CC}$ – 0.6 | V | LVPECL |
| $V_{OH}$ | Output HIGH Voltage | | 1.8 | | | V | $I_{OH}$ = –15mA[2] |
| $V_{OL}$ | Output LOW Voltage | | | | 0.6 | V | $I_{OL}$ = 15mA |
| $Z_{OUT}$ | Output Impedance | | | 17 – 20 | | Ω | |
| $I_{IN}$ | Input Current[3] | | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | | 1.0 | mA | All $V_{CC}$ Pins |

1. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (DC) specification.
2. The MPC9448 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.
3. Inputs have pull–down or pull–up resistors affecting the input current.



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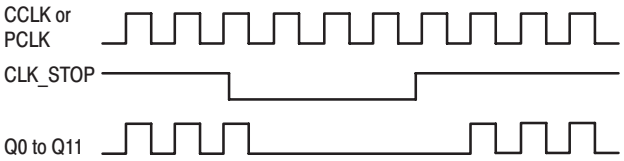
**TABLE 8: AC CHARACTERISTICS** ($V_{CC}$ = 2.5V ±5%, $T_A$ = –40°C to +85°C)[1, 2]

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{PP}$ | Peak–to–Peak Input Voltage | PCLK, $\overline{PCLK}$ | 500 | | 1000 | mV | LVPECL |
| $V_{CMR}$[3] | Common Mode Range | PCLK, $\overline{PCLK}$ | 1.2 | | $V_{CC}$ – 0.6 | V | LVPECL |
| $f_{max}$ | Maximum Output Frequency | | 0 | | 275 | MHz | |
| $f_{ref}$ | Maximum Input Frequency | | 0 | | 275 | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | | 60 | % | |
| $t_r$, $t_f$ | CCLK Input Rise/Fall Time | | | | 1.0 | ns | 0.7V to 1.7V |
| $t_{sk(O)}$ | Output–to–Output Skew[4] | | | | 150 | ps | |
| $t_{sk(PP)}$ | Device–to–Device Skew | | | | TBD | ps | |
| $DC_Q$ | Output Duty Cycle | | 45 | 50 | 55 | % | $DC_{REF}$ = 50% |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay | CCLK to any Q<br>PCLK to any Q | | | TBD | ns | |
| $t_{PLZ}$,$t_{PHZ}$ | Output Disable Time | OE to any Q | | | 11 | ns | |
| $t_{PZL}$,$t_{PLZ}$ | Output Enable Time | OE to any Q | | | 11 | ns | |
| $t_S$ | Setup Time | CLK_STOP to CCLK[5]<br>CLK_STOP to PCLK[5] | TBD<br>TBD | | | ns<br>ns | |
| $t_H$ | Hold Time | CLK_STOP to CCLK[5]<br>CLK_STOP to PCLK[5] | TBD<br>TBD | | | ns<br>ns | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.6V to 1.8V |
| $t_{JIT(CC)}$ | Cycle–to–Cycle Jitter | RMS (1 σ) | | TBD | | ps | |

1. All AC characteristics are design targets and subject to change upon device characterization.
2. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
3. $V_{CMR}$ (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ or $V_{PP}$ impacts static phase offset $t_{(\varnothing)}$.
4. See application section for part–to–part skew calculation.
5. Setup and Hold times are referenced to the falling edge of the selected clock signal input.

## APPLICATIONS INFORMATION

**Figure 3. Output Clock Stop (CLK_STOP) Timing Diagram**




### Driving Transmission Lines

The MPC9448 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of 14Ω ($V_{CC}$=3.3V) or 18Ω ($V_{CC}$=2.5V), the outputs can drive either parallel or series terminated transmission lines. For more information on transmission lines, the reader is referred to Motorola application note AN1091. In most high performance clock networks, point–to–point distribution of signals is the method of choice. In a point–to–point scheme, either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}$÷2.

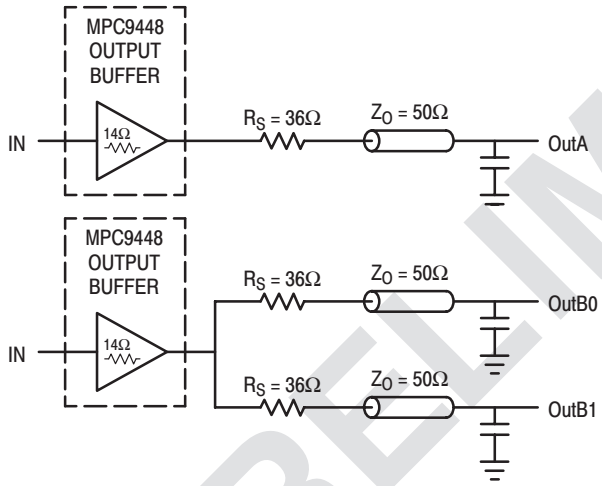



**Figure 4. Single versus Dual Transmission Lines**

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9448 clock driver. For the series terminated case, however, there is no DC current draw; thus, the outputs can drive multiple series terminated lines. Figure 4 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme, the fanout of the MPC9448 clock driver is effectively doubled due to its capability to drive multiple lines.

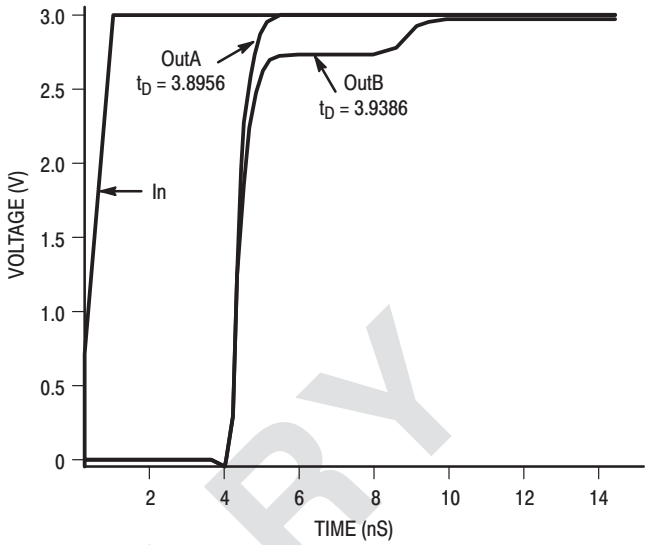


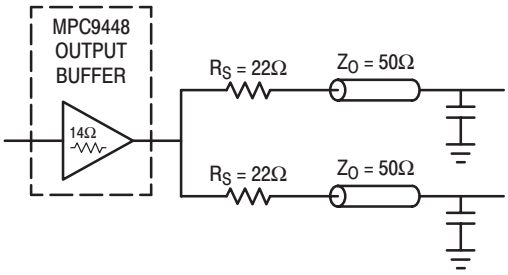

**Figure 5. Single versus Dual Line Termination Waveforms**

The waveform plots in Figure 5 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases, the drive capability of the MPC9448 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC9448. The output waveform in Figure 5 “Single versus Dual Line Termination Waveforms” shows a step in the waveform; this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S ( Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\Omega \,||\, 50\Omega$$
$$R_S = 22\Omega \,||\, 22\Omega$$
$$R_0 = 14\Omega$$
$$V_L = 3.0 ( 25 \div (18+14+25)$$
$$= 1.25V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

Since this step is well above the threshold region it will not cause any false clock triggering; however, designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines, the situation in Figure 6 “Optimized Dual Line Termination” should be used. In this case, the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




14Ω + 22Ω || 22Ω = 50Ω || 50Ω
25Ω = 25Ω

**Figure 6. Optimized Dual Line Termination**



5

**The Following Figures Illustrate the Measurement Reference for the MPC9448 Clock Driver Circuit**

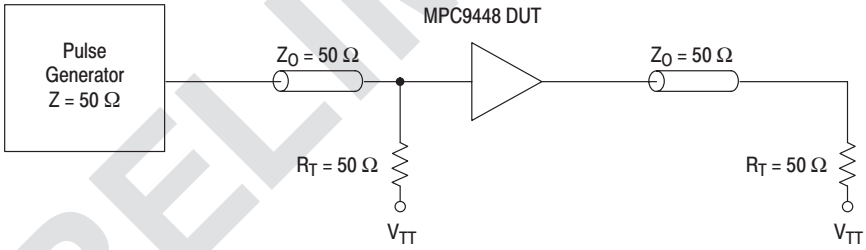



**Figure 7. CCLK MPC9448 AC Test Reference for $V_{cc}$ = 3.3V and $V_{cc}$ = 2.5V**

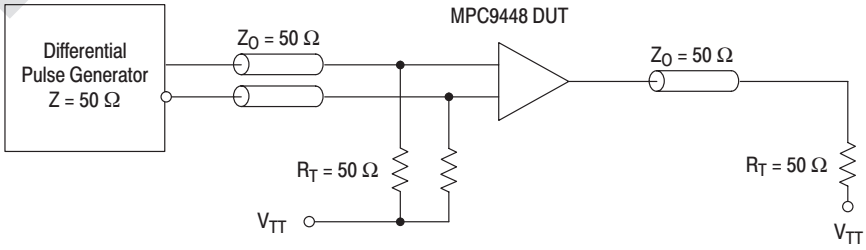
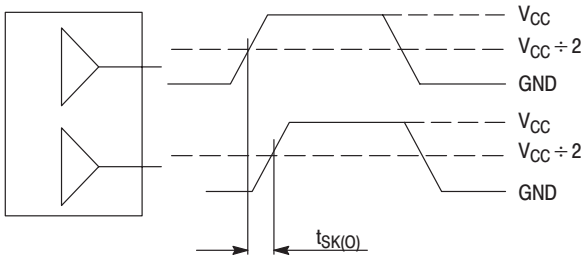



**Figure 8. PCLK MPC9448 AC Test Reference**




The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 9. Output–to–Output Skew $t_{SK(O)}$**

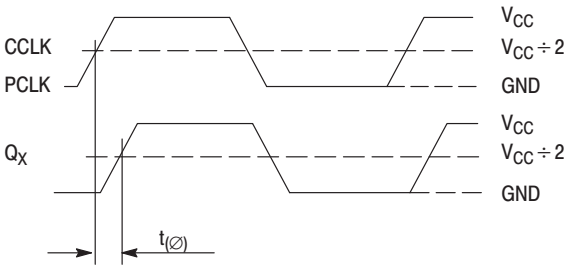
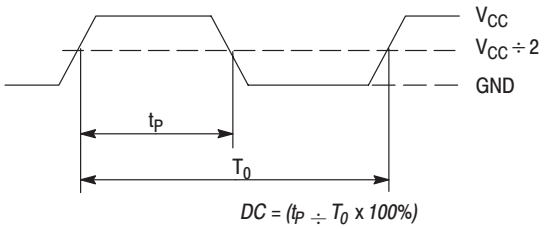



**Figure 10. Propagation Delay ($t_{PD}$) Test Reference**




The time from the output controlled edge to the non–controlled edge, divided by the time between output controlled edges, expressed as a percentage

**Figure 11. Output Duty Cycle (DC)**

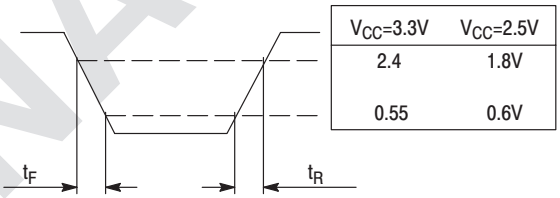
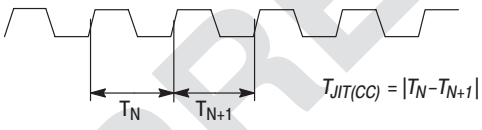



**Figure 12. Output Transition Time Test Reference**




The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

**Figure 13. Cycle–to–Cycle Jitter**

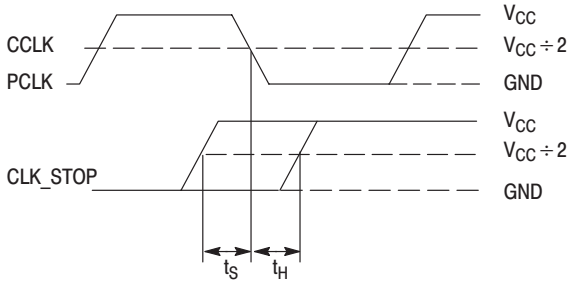



**Figure 14. Setup and Hold Time ($t_S$, $t_H$) Test Reference**



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**Order Number: MPC9449/D**
**Rev 0, 11/2001**

*Product Preview*

# 3.3V/2.5V 1:15 PECL/LVCMOS Clock Fanout Buffer

**MPC9449**

**3.3V/2.5V 1:15**
**PECL/LVCMOS**
**CLOCK FANOUT BUFFER**

**FA SUFFIX**
52 LEAD LQFP PACKAGE
CASE 848D

The MPC9449 is a 3.3V or 2.5V compatible, 1:15 clock fanout buffer targeted for high performance clock tree applications. With output frequencies up to 200[1] MHz and output skews less than 200 ps[1] the device meets the needs of the most demanding clock applications.

**Features**

- 15 LVCMOS compatible clock outputs
- Two selectable LVCMOS and one differential LVPECL compatible clock inputs
- Selectable output frequency divider (divide-by-one and divide-by-two)
- Maximum clock frequency of 200[1] MHz
- Maximum clock skew of 200 ps[1]
- High-impedance output control
- 3.3V or 2.5V power supply
- Drives up to 30 series terminated clock lines
- Ambient temperature range –40°C to +85°C
- 52 lead LQFP packaging
- Supports clock distribution in networking, telecommunication and computing applications
- Pin and function compatible to MPC949

**Functional Description**

The MPC9449 is specifically designed to distribute LVCMOS compatible clock signals up to a frequency of 200[1] MHz. The device has 15 identical outputs, organized in 4 output banks. Each output bank provides a retimed or frequency divided copy of the input signal with a near zero skew. The outputs buffers support driving of 50Ω terminated transmission lines on the incident edge: each output is capable of driving either one parallel terminated or two series terminated transmission lines.

Two selectable LVCMOS compatible clock inputs are available. This feature supports redundant differential clock sources. In addition, the MPC9449 accepts one differential PECL clock signal. The DSELx pins choose between division of the input reference frequency by one or two. The frequency divider can be set individually for each of the four output bank. Applying the OE control will force the outputs into high-impedance mode.

All inputs have an internal pull-up or pull-down resistor preventing unused and open inputs from floating. The device supports a 2.5V or 3.3V power supply and an ambient temperature range of –40°C to +85°C. The MPC9449 is pin and function compatible but performance-enhanced to the MPC949. The device is packaged in a 52-lead LQFP package.



1. Final specification of this parameter is pending characterization.



**Rev 0**

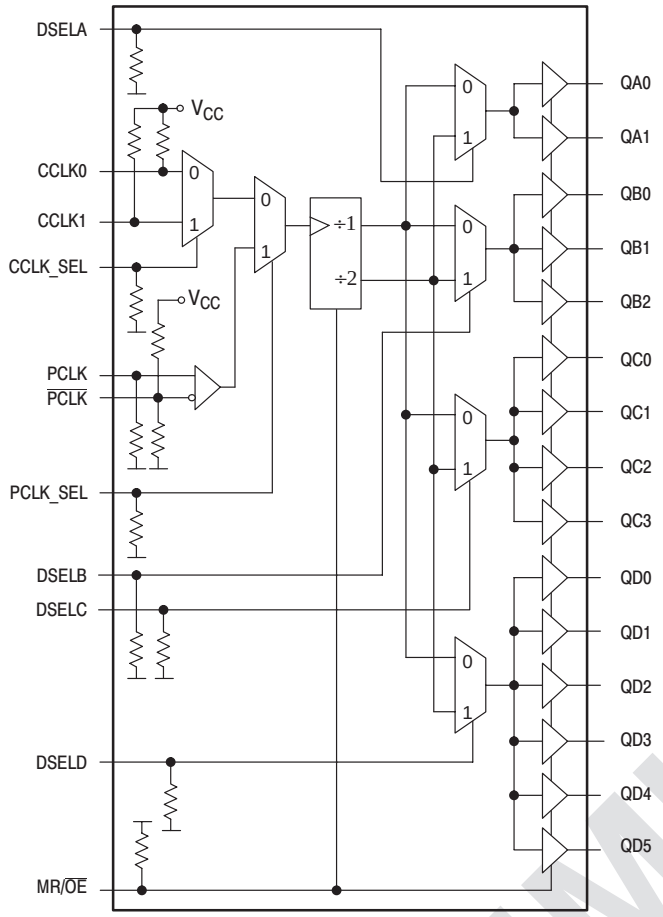


**Figure 1. MPC9449 Logic Diagram**

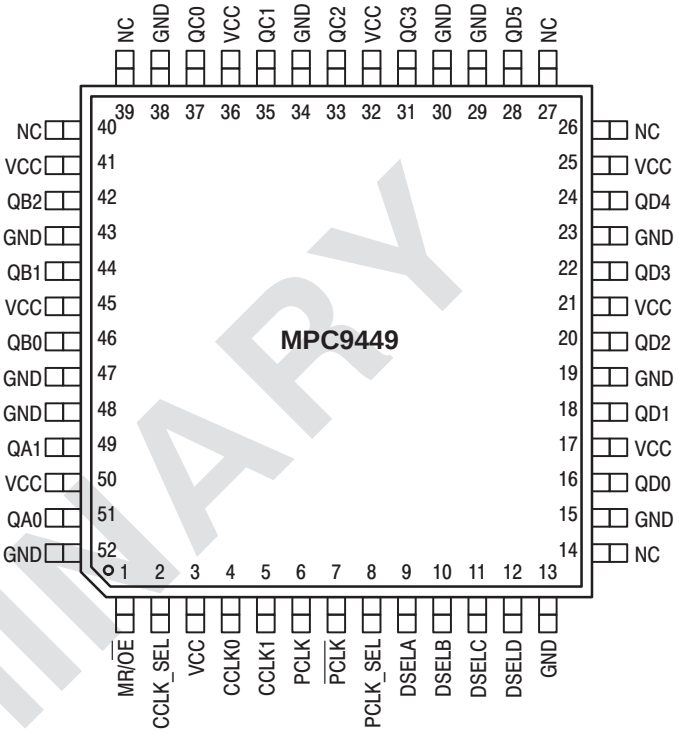


**Figure 2. MPC9449 52–Lead Package Pinout** (Top View)



**Table 1: FUNCTION TABLE**

| Control | Default | 0 | 1 |
|---|---|---|---|
| PCLK_SEL | 0 | LVCMOS clock input selected (CCLK0 or CCLK1) | PCLK differential inputs selected |
| CCLK_SEL | 0 | CCLK0 selected | CCLK1 selected |
| DSELA, DSELB, DSELC, DSELD | 0 0<br>0 0 | ÷1 | ÷2 |
| $\overline{OE}$/MR | 1 | Outputs enabled | Outputs disabled (high impedance) |

**Table 2: PIN CONFIGURATION**

| Pin | I/O | Type | Function |
|---|---|---|---|
| PCLK, $\overline{PCLK}$ | Input | LVPECL | Differential LVPECL clock input |
| CCLK0, CCLK1 | Input | LVCMOS | LVCMOS clock inputs |
| PCLK_SEL | Input | LVCMOS | LVPECL clock input select |
| CCLK_SEL | Input | LVCMOS | LVCMOS clock input select |
| DSELA, DSELB, DSELC, DSELD | Input | LVCMOS | Clock divider selection |
| $\overline{OE}$/MR | Input | LVCMOS | Output enable/disable (high-impedance tristate) |
| QA0-1, QB0-2, QC0-3, QB0-5 | Output | LVCMOS | Clock outputs |
| GND | Supply | Ground | Negative power supply (GND) |
| VCC | Supply | VCC | Positive power supply for I/O and core. All VCC pins must be connected to the positive power supply for correct operation |

**Table 3: GENERAL SPECIFICATIONS**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output Termination Voltage | | $V_{CC} \div 2$ | | V | |
| MM | ESD Protection (Machine Model) | 200 | | | V | |
| HBM | ESD Protection (Human Body Model) | 2000 | | | V | |
| LU | Latch–Up Immunity | 200 | | | mA | |
| $C_{PD}$ | Power Dissipation Capacitance | | 12 | | pF | Per output |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | Inputs |

**Table 4: ABSOLUTE MAXIMUM RATINGS[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage Temperature | -65 | 125 | °C | |

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

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**Table 5: DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40°C to 85°C)

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | | | | 0.8 | V | LVCMOS |
| $V_{OH}$ | Output High Voltage | | 2.4 | | | V | $I_{OH}$=-24 mA[a] |
| $V_{PP}$ | Peak-to-peak input voltage | PCLK, $\overline{PCLK}$ | 250 | | | mV | LVPECL |
| $V_{CMR}$[b] | Common Mode Range | PCLK, $\overline{PCLK}$ | 1.0 | | $V_{CC}$-0.6 | V | LVPECL |
| $V_{OL}$ | Output Low Voltage | | | | 0.55<br>0.30 | V<br>V | $I_{OL}$= 24 mA<br>$I_{OL}$= 12 mA |
| $Z_{OUT}$ | Output impedance | | | 14 - 17 | | Ω | |
| $I_{IN}$ | Input Current[c] | | | | ±200 | µA | $V_{IN}$=$V_{CC}$ or GND |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | | 10 | mA | All $V_{CC}$ Pins |

a The MPC9449 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

b $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (DC) specification.

c Inputs have pull-down or pull-up resistors affecting the input current.

**Table 6: AC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5%, $T_A$ = –40°C to 85°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{PP}$ | Peak-to-peak input voltage | PCLK, $\overline{PCLK}$ | 400 | | 1000 | mV | LVPECL |
| $V_{CMR}$[c] | Common Mode Range | PCLK, $\overline{PCLK}$ | 1.0 | | $V_{CC}$-0.6 | V | LVPECL |
| $f_{max}$ | Output frequency | | 0 | | 200 | MHz | |
| $f_{ref}$ | Input Frequency | | 0 | | 200 | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | 50 | 60 | % | |
| $t_r$, $t_f$ | CCLK0, CCLK1 Input Rise/Fall Time | | | | 1.0 | ns | 0.8 to 2.0V |
| $t_{sk(O)}$ | Output-to-output Skew | | | | 200 | ps | |
| $t_{sk(PP)}$ | Device-to-device Skew | | | 1.75 | | ps | |
| $DC_Q$ | Output Duty Cycle | | 45 | 50 | 55 | % | $DC_{REF}$ = 50% |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay | CCLK0 or CCLK1 to any Q<br>PCLK to any Q | | 3.0<br>3.0 | TBD<br>TBD | ns<br>ns | |
| $t_{PLZ, HZ}$ | Output Disable Time | OE to any Q | | | 11 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | OE to any Q | | | 11 | ns | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.55 to 2.4V |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ) | | TBD | | ps | |

a All AC characteristics are design targets and subject to change upon device characterization.

b AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.

c $V_{CMR}$ (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ or $V_{PP}$ impacts static phase offset $t_{(\varnothing)}$.



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**Table 7: DC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40°C to 85°C)

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | | -0.3 | | 0.7 | V | LVCMOS |
| $V_{PP}$ | Peak-to-peak input voltage | PCLK, $\overline{PCLK}$ | 250 | | | mV | LVPECL |
| $V_{CMR}$[a] | Common Mode Range | PCLK, $\overline{PCLK}$ | 1.0 | | $V_{CC}$-0.6 | V | LVPECL |
| $V_{OH}$ | Output High Voltage | | 1.8 | | | V | $I_{OH}$=-15 mA[b] |
| $V_{OL}$ | Output Low Voltage | | | | 0.6 | V | $I_{OL}$= 15 mA |
| $Z_{OUT}$ | Output impedance | | | 17 - 20 | | Ω | |
| $I_{IN}$ | Input Current[c] | | | | ±200 | µA | $V_{IN}$=$V_{CC}$ or GND |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | | 10 | mA | All $V_{CC}$ Pins |

a $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (DC) specification.

b The MPC9449 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.

c Inputs have pull-down or pull-up resistors affecting the input current.

**Table 8: AC CHARACTERISTICS** ($V_{CC}$ = 2.5V ± 5%, $T_A$ = –40°C to 85°C)[a b]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{PP}$ | Peak-to-peak input voltage | PCLK, $\overline{PCLK}$ | 400 | | 1000 | mV | LVPECL |
| $V_{CMR}$[c] | Common Mode Range | PCLK, $\overline{PCLK}$ | 1.2 | | $V_{CC}$-0.6 | V | LVPECL |
| $f_{max}$ | Output frequency | | 0 | | 200 | MHz | |
| $f_{ref}$ | Input Frequency | | 0 | | 200 | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | | 40 | | 60 | % | |
| tr, tf | CCLK Input Rise/Fall Time | | | | 1.0 | ns | 0.7 to 1.7V |
| $t_{sk(O)}$ | Output-to-output Skew[d] | | | | 200 | ps | |
| $t_{sk(PP)}$ | Device-to-device Skew | | | 1.75 | | ps | |
| $DC_Q$ | Output Duty Cycle | | 45 | 50 | 55 | % | $DC_{REF}$ = 50% |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay | CCLK0 or CCLK1 to any Q<br>PCLK to any Q | | 3.0<br>3.0 | TBD<br>TBD | ns<br>ns | |
| $t_{PLZ, HZ}$ | Output Disable Time | OE to any Q | | | 11 | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | OE to any Q | | | 11 | ns | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.6 to 1.8V |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | RMS (1 σ) | | TBD | | ps | |

a All AC characteristics are design targets and subject to change upon device characterization.

b AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.

c $V_{CMR}$ (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ or $V_{PP}$ impacts static phase offset $t_{(\varnothing)}$.

d See application section for part-to-part skew calculation.

## APPLICATIONS INFORMATION

### Driving Transmission Lines

The MPC9449 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}$÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9449 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9449 clock driver is effectively doubled due to its capability to drive multiple lines.

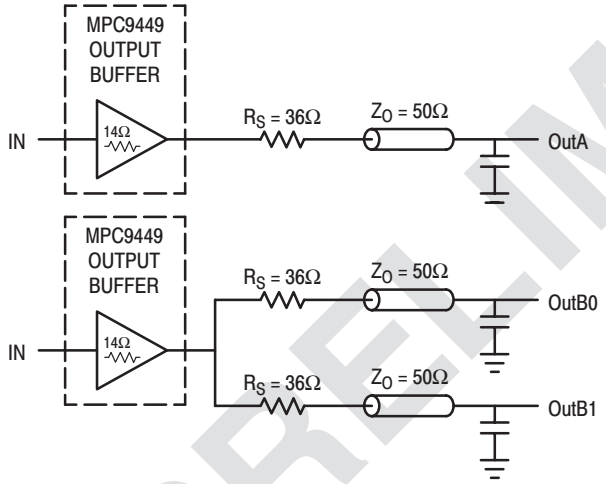



**Figure 3. Single versus Dual Transmission Lines**

The waveform plots in Figure 4 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9449 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9449. The output waveform in Figure 4 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S ( Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\Omega \parallel 50\Omega$$
$$R_S = 36\Omega \parallel 36\Omega$$
$$R_0 = 14\Omega$$
$$V_L = 3.0 ( 25 \div (18+17+25)$$
$$= 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

1. Final skew data pending specification.

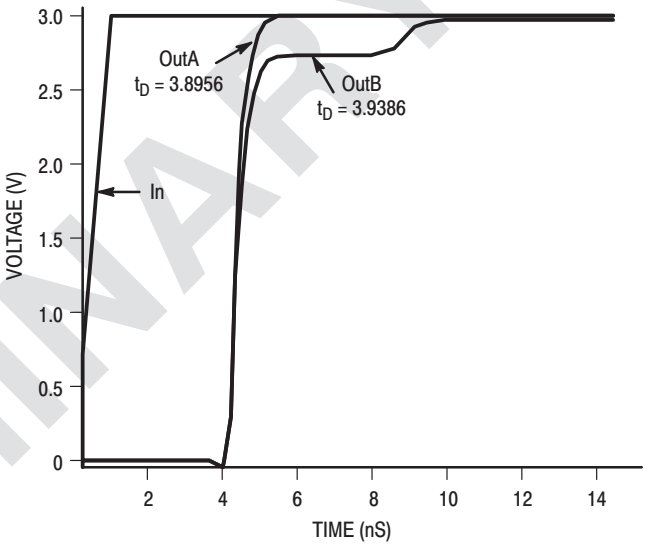
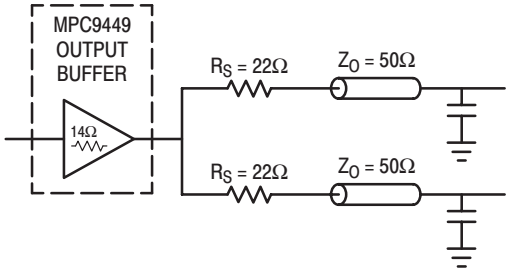



**Figure 4. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




$14\Omega + 22\Omega \parallel 22\Omega = 50\Omega \parallel 50\Omega$
$25\Omega = 25\Omega$

**Figure 5. Optimized Dual Line Termination**

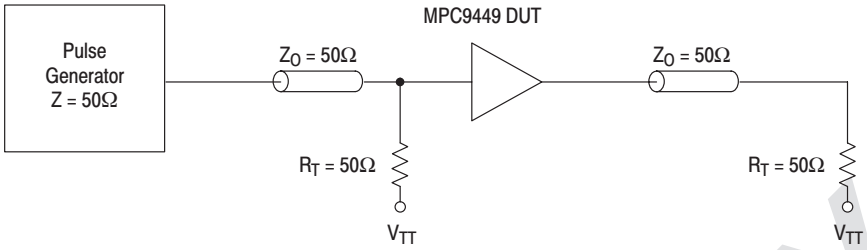



**Figure 6. CCLK MPC9449 AC test reference for $V_{cc}$ = 3.3V and $V_{cc}$ = 2.5V**

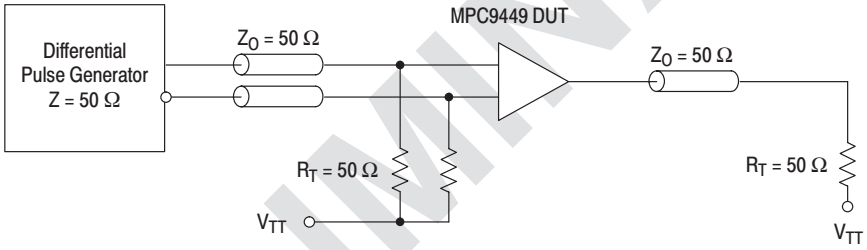
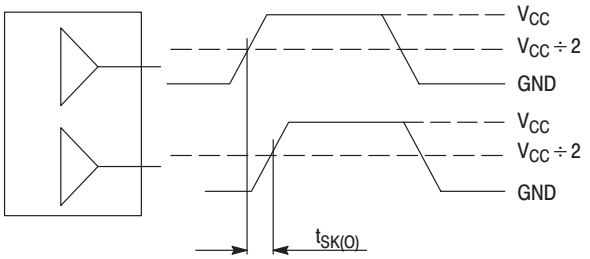



**Figure 7. PCLK MPC9449 AC test reference**




The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 8. Output–to–output Skew $t_{SK(O)}$**

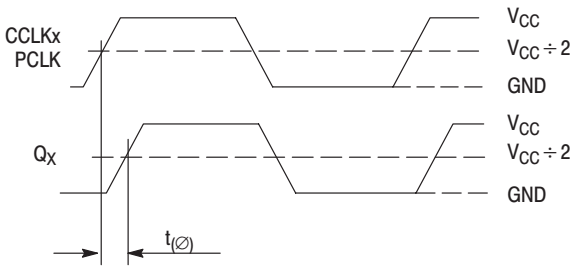
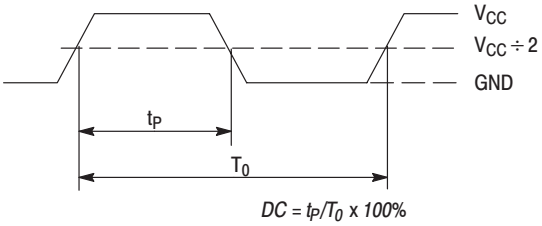



**Figure 9. Propagation delay ($t_{(\varnicothing)}$, static phase offset) test reference**




The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 10. Output Duty Cycle (DC)**

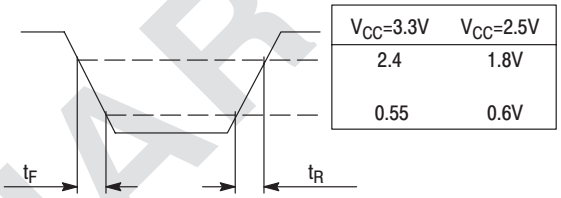
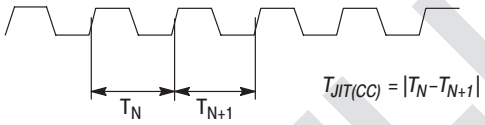



**Figure 11. Output Transition Time Test Reference**




The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

**Figure 12. Cycle–to–cycle Jitter**



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*Product Preview*

# 2.5V and 3.3V LVCMOS Clock Fanout Buffer

**MPC9456**

**LOW VOLTAGE SINGLE OR DUAL SUPPLY 2.5V AND 3.3V LVCMOS CLOCK DISTRIBUTION BUFFER**

**FA SUFFIX**
LQFP PACKAGE
CASE 873A–02

The MPC9456 is a 2.5V and 3.3V compatible 1:10 clock distribution buffer designed for low-voltage mid-range to high-performance telecom, networking and computing applications. Both 3.3V, 2.5V and dual supply voltages are supported for mixed-voltage applications. The MPC9456 offers 10 low-skew outputs and a differential LVPECL clock input. The outputs are configurable and support 1:1 and 1:2 output to input frequency ratios. The MPC9456 is specified for the extended temperature range of –40 to 85°C.

**Features**

- Configurable 10 outputs LVCMOS clock distribution buffer
- Compatible to single, dual and mixed 3.3V/2.5V voltage supply
- Wide range output clock frequency up to 250 MHz
- Designed for mid-range to high-performance telecom, networking and computer applications
- Supports high-performance differential clocking applications
- Max. output skew of 200 ps (100 ps within one bank)
- Selectable output configurations per output bank
- Tristable outputs
- 32 ld LQFP package
- Ambient operating temperature range of –40 to 85°C

**Functional Description**

The MPC9456 is a full static design supporting clock frequencies up to 250 MHz. The signals are generated and retimed on-chip to ensure minimal skew between the three output banks.

Each of the three output banks can be individually supplied by 2.5V or 3.3V supporting mixed voltage applications. The FSELx pins choose between division of the input reference frequency by one or two. The frequency divider can be set individually for each of the three output banks. The MPC9456 can be reset and the outputs are disabled by deasserting the $\overline{OE}$/MR pin (logic high state). Asserting $\overline{OE}$ will enable the outputs.

All control inputs accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. The clock input is low voltage PECL compatible for differential clock distribution support. Please consult the MPC9446 specification for a full CMOS compatible device. For series terminated transmission lines, each of the MPC9456 outputs can drive one or two traces giving the devices an effective fanout of 1:20. The device is packaged in a 7x7 $mm^2$ 32-lead LQFP package.

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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.
**Rev 0**

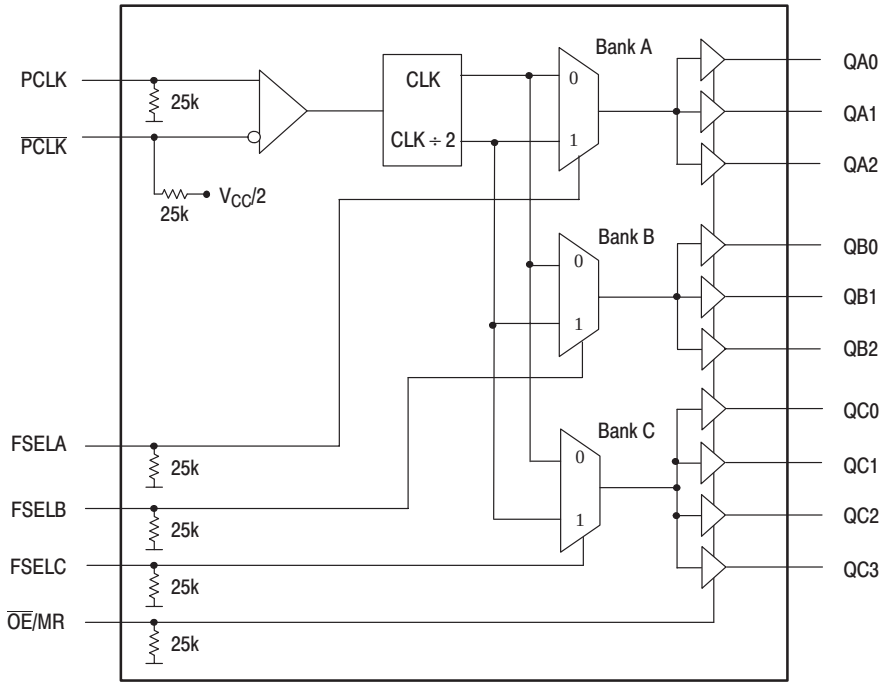


**Figure 1. MPC9456 Logic Diagram**



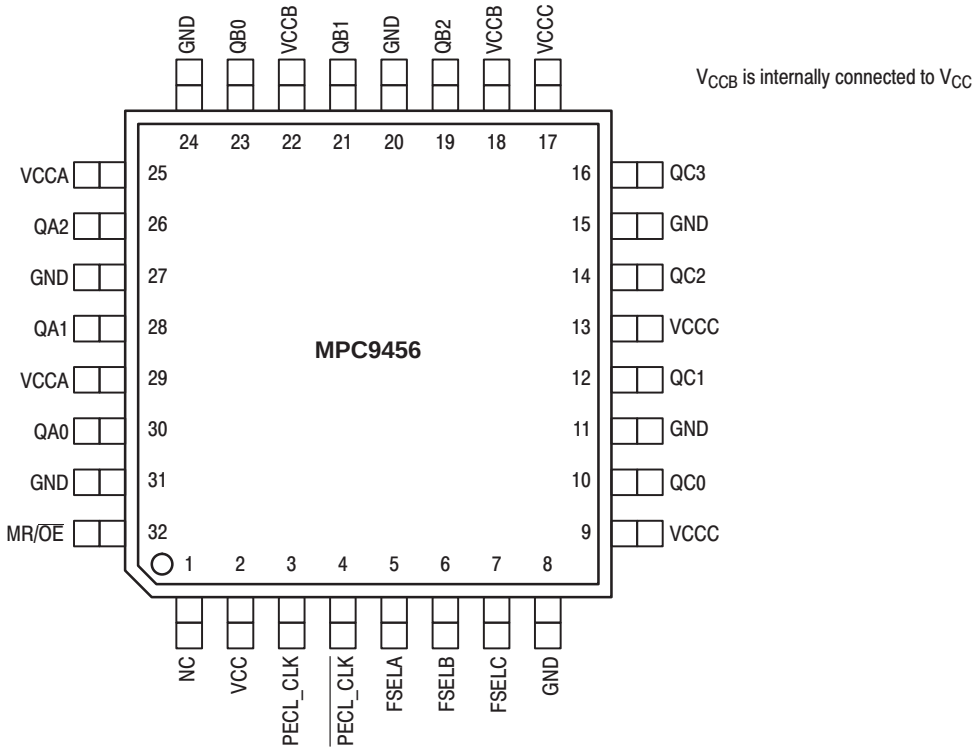


**Figure 2. Pinout: 32–Lead Package Pinout** (Top View)

**Table 1: Pin Configuration**

| Pin | I/O | Type | Function |
|---|---|---|---|
| PECL_CLK, $\overline{\text{PECL\_CLK}}$ | Input | LVPECL | Differential clock reference<br>Low voltage positive ECL input |
| $FSEL_A$, $FSEL_B$, $FSEL_C$ | Input | LVCMOS | Output bank divide select input |
| MR/$\overline{OE}$ | Input | LVCMOS | Internal reset and output tristate control |
| GND | | Supply | Negative voltage supply output bank (GND) |
| $V_{CCA}$, $V_{CCB}$*, $V_{CCC}$ | | Supply | Positive voltage supply for output banks |
| $V_{CC}$ | | Supply | Positive voltage supply core (VCC) |
| QA0 - QA2 | Output | LVCMOS | Bank A outputs |
| QB0 - QB2 | Output | LVCMOS | Bank B outputs |
| QC0 - QC3 | Output | LVCMOS | Bank C outputs |

* $V_{CCB}$ is internally connected to $V_{CC}$.

**Table 2: Supported Single and Dual Supply Configurations**

| Supply voltage configuration | $V_{CC}$[a] | $V_{CCA}$[b] | $V_{CCB}$[c] | $V_{CCC}$[d] | GND |
|---|---|---|---|---|---|
| 3.3V | 3.3V | 3.3V | 3.3V | 3.3V | 0V |
| Mixed voltage supply | 3.3V | 3.3V or 2.5V | 3.3V | 3.3V or 2.5V | 0 V |
| 2.5V | 2.5V | 2.5V | 2.5V | 2.5V | 0 V |

a. $V_{CC}$ is the positive power supply of the device core and input circuitry. $V_{CC}$ voltage defines the input threshold and levels
b. $V_{CCA}$ is the positive power supply of the bank A outputs. $V_{CCA}$ voltage defines bank A output levels
c. $V_{CCB}$ is the positive power supply of the bank B outputs. $V_{CCB}$ voltage defines bank B output levels. $V_{CCB}$ is internally connected to $V_{CC}$.
d. $V_{CCC}$ is the positive power supply of the bank C outputs. $V_{CCC}$ voltage defines bank C output levels

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**Table 3: Function Table (Controls)**

| Control | Default | 0 | 1 |
|---|---|---|---|
| CLK_SEL | 0 | TCLK0 | TCLK1 |
| FSELA | 0 | $f_{QA0:2} = f_{REF}$ | $f_{QA0:2} = f_{REF} \div 2$ |
| FSELB | 0 | $f_{QB0:2} = f_{REF}$ | $f_{QB0:2} = f_{REF} \div 2$ |
| FSELC | 0 | $f_{QC0:3} = f_{REF}$ | $f_{QC0:3} = f_{REF} \div 2$ |
| MR/$\overline{OE}$ | 0 | Outputs enabled | Internal reset<br>Outputs disabled (tristate) |

**Table 4: Absolute Maximum Ratings[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 4.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -40 | 125 | °C | |

a. Absolute maximum continuos ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

**Table 5: DC Characteristics ($V_{CC}$ = $V_{CCA}$ = $V_{CCB}$ = $V_{CCC}$ = 3.3V ± 5%, $T_A$ = –40 to +85°C)[a]**

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | | -0.3 | | 0.8 | V | LVCMOS |
| $I_{IN}$ | Input current[b] | | | | 120 | µA | |
| $V_{PP}$ | Peak-to-peak input voltage[c] | PCLK, $\overline{PCLK}$ | 500 | | 1000 | mV | LVPECL |
| $V_{CMR}$[d] | Common Mode Range[e] | PCLK, $\overline{PCLK}$ | 1.2 | | $V_{CC}$-0.8 | V | LVPECL |
| $C_{IN}$ | Input capacitance | | | 4.0 | | pF | |
| $V_{OH}$ | Output High Voltage | | 2.4 | | | V | $I_{OH}$=-24 mA[f] |
| $V_{OL}$ | Output Low Voltage | | | | 0.55<br>0.30 | V<br>V | $I_{OL}$= 24mA[f]<br>$I_{OL}$= 12mA |
| $Z_{OUT}$ | Output impedance | | | 14 - 17 | | W | |
| $C_{PD}$ | Power Dissipation Capacitance | | | 10 | | pF | Per Output |
| $I_{CC}$ | Maximum Core Supply Current | | | | | mA | $V_{CC}$ Pins |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | | 1.0 | mA | All $V_{CCx}$ Pins |
| $V_{TT}$ | Output termination voltage | | | $V_{CC}$÷2 | | V | |

a. DC specifications are design targets, final specification is pending device characterization
b. Input pull-up / pull-down resistors influence input current
c. Pending characterization
d. $V_{CMR}$ is the difference from $V_{CC}$ and the crosspoint of the differential input signal. Normal operation is obtained when the “high” input is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ specification.
e. Pending characterization
f. The MPC9456 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

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**Table 6: AC Characteristics ($V_{CC}$ = $V_{CCA}$ = $V_{CCB}$ = $V_{CCC}$ = 3.3V ± 5%, $T_A$ = –40 to +85°C)[a] [b]**

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency | | 0 | 250 | | MHz | |
| $f_{MAX}$ | Maximum Output Frequency | ÷1 output<br>÷2 output | 0<br>0 | 250<br>125 | | MHz<br>MHz | FSELx=0<br>FSELx=1 |
| $f_{refDC}$ | Reference Input Duty Cycle | | 25 | 50 | 75 | % | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay | PCLK to any Q | | | | ns | |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | | ns | |
| $t_{sk(O)}$ | Output-to-output Skew | Within one bank<br>Any output | | | 100[b]<br>200[b] | ps<br>ps | |
| $t_{sk(PP)}$ | Device-to-device Skew | | | | | ps<br>ps | |
| $DC_O$ | Output Duty Cycle | ÷1 output<br>÷2 output | 45<br>48 | 50<br>50 | 55<br>52 | %<br>% | $DC_{REF}$ = 50%<br>$DC_{REF}$ = 25%-75% |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.55 to 2.4V |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$
b. AC specifications are design targets, final specification is pending device characterization

**Table 7: DC Characteristics ($V_{CC}$ = $V_{CCA}$ = $V_{CCB}$ = $V_{CCC}$ = 2.5V ± 5%, $T_A$ = –40 to +85°C)[a]**

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input low voltage | | -0.3 | | 0.7 | V | LVCMOS |
| $V_{OH}$ | Output High Voltage | | 1.8 | | | V | $I_{OH}$=-15 mA[b] |
| $V_{OL}$ | Output Low Voltage | | | | 0.6 | V | $I_{OL}$= 15 mA |
| $V_{PP}$ | Peak-to-peak input voltage | PCLK, $\overline{PCLK}$ | 500 | | 1000 | mV | LVPECL |
| $V_{CMR}$[c] | Common Mode Range | PCLK, $\overline{PCLK}$ | 1.1 | | $V_{CC}$-0.7 | V | LVPECL |
| $Z_{OUT}$ | Output impedance | | | 17 - 20 | | W | |
| $I_{IN}$ | Input Current | | | | | µA | |
| $C_{IN}$ | Input capacitance | | | 4 | | pF | |
| $C_{PD}$ | Power Dissipation Capacitance | | | 10 | | pF | Per Output |
| $I_{CC}$ | Maximum Core Supply Current | | | | | mA | $V_{CC}$ Pins |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | | 1.0 | mA | All $V_{CCx}$ Pins |
| $V_{TT}$ | Output termination voltage | | | $V_{CC}$÷2 | | V | |

a. DC specifications are design targets, final specification is pending device characterization
b. The MPC9456 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.
c. $V_{CMR}$ is the difference from $V_{CC}$ and crosspoint of the differential input signal. Normal operation is obtained when the “high” input is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ specification.

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**Table 8: AC Characteristics ($V_{CC}$ = $V_{CCA}$ = $V_{CCB}$ = $V_{CCC}$ = 2.5 ± 5%, $T_A$ = –40 to +85°C)[a] [b]**

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency | | 0 | 250 | | MHz | |
| $f_{MAX}$ | Maximum Output Frequency | ÷1 output<br>÷2 output | 0<br>0 | 250<br>125 | | MHz<br>MHz | FSELx=0<br>FSELx=1 |
| $f_{refDC}$ | Reference Input Duty Cycle | | 25 | | 75 | % | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay | CLK to any Q<br>CLK to any Q | | | | ns | |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | | ns | |
| $t_{PZL, LZ}$ | Output Enable Time | | | | | ns | |
| $t_{sk(O)}$ | Output-to-output Skew | Within one bank<br>Any output | | 100[b]<br>200[b] | | ps<br>ps | |
| $t_{sk(PP)}$ | Device-to-device Skew | | | | | ps<br>ps | |
| $DC_O$ | Output Duty Cycle | ÷1 output<br>÷2 output | 45<br>48 | 50<br>50 | 55<br>52 | %<br>% | $DC_{REF}$ = 50%<br>$DC_{REF}$ = 25%-75% |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.6 to 1.8V |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$
b. AC specifications are design targets, final specification is pending device characterization

**Table 9: AC Characteristics ($V_{CC}$ = 3.3V ± 5%, any $V_{CCA,B,C,D}$ = 2.5V ± 5% or 3.3V ± 5% (mixed), $T_A$ = –40 to +85°C)[a] [b] [c]**

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $t_{sk(O)}$ | Output-to-output Skew | Within one bank<br>Any output | | | 100[b]<br>250[b] | ps<br>ps | |
| $t_{sk(PP)}$ | Device-to-device Skew | | | | | ps<br>ps | |
| $DC_O$ | Output Duty Cycle | ÷1 output<br>÷2 output | 45<br>48 | 50<br>50 | 55<br>52 | %<br>% | $DC_{REF}$ = 50%<br>$DC_{REF}$ = 25%-75% |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$
b. AC specifications are design targets, final specification is pending device characterization
c. For all other AC specifications, refer to 2.5V or 3.3V tables according to the supply voltage of the output bank

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## APPLICATIONS INFORMATION

### Driving Transmission Lines

The MPC9456 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}$÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9456 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3“Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9456 clock driver is effectively doubled due to its capability to drive multiple lines.



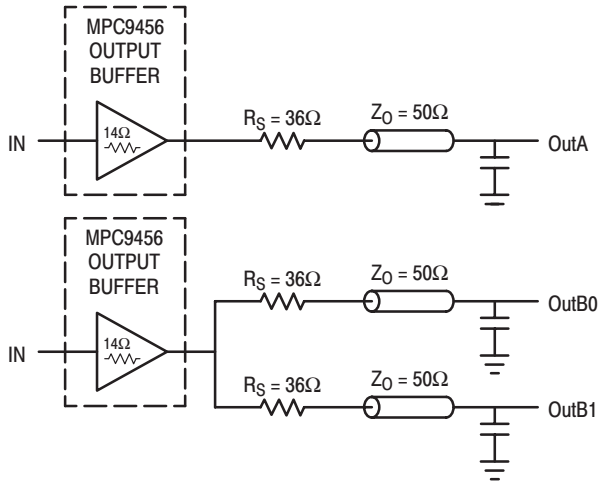



**Figure 3. Single versus Dual Transmission Lines**

The waveform plots in Figure 4“Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9456 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9456. The output waveform in Figure 4“Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S ( Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\Omega \parallel 50\Omega$$
$$R_S = 36\Omega \parallel 36\Omega$$
$$R_0 = 17\Omega$$
$$V_L = 3.0 ( 25 \div (18+17+25)$$
$$= 1.25V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

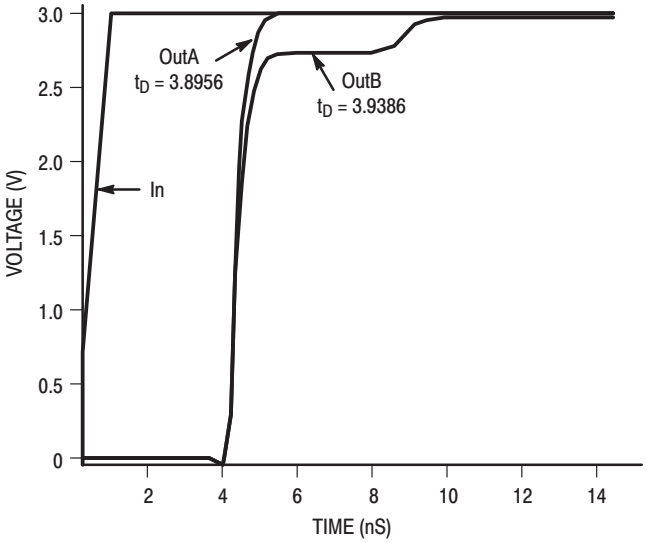
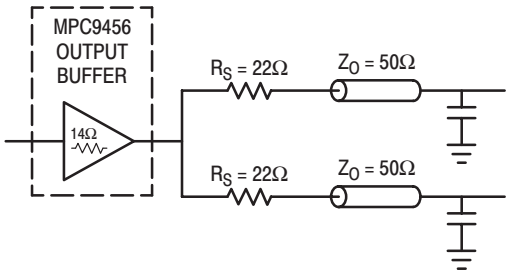



**Figure 4. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5“Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




$14\Omega + 22\Omega \parallel 22\Omega = 50\Omega \parallel 50\Omega$
$25\Omega = 25\Omega$

**Figure 5. Optimized Dual Line Termination**

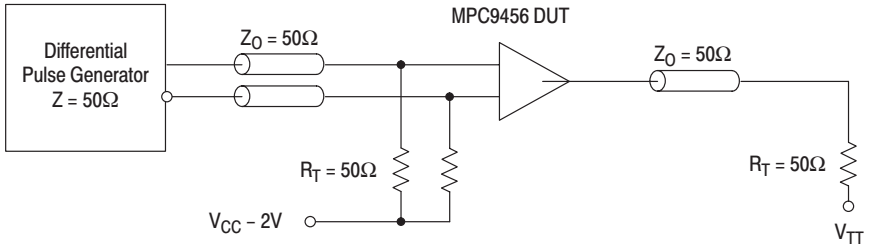



**Figure 6. PECL_CLK MPC9456 AC test reference for $V_{cc}$ = 3.3V and $V_{cc}$ = 2.5V**

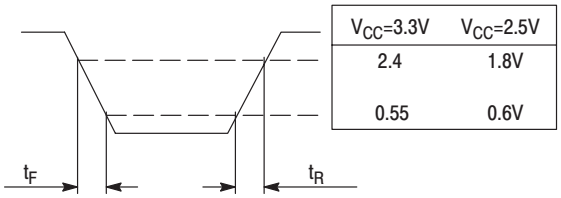



**Figure 7. Output Transition Time Test Reference**

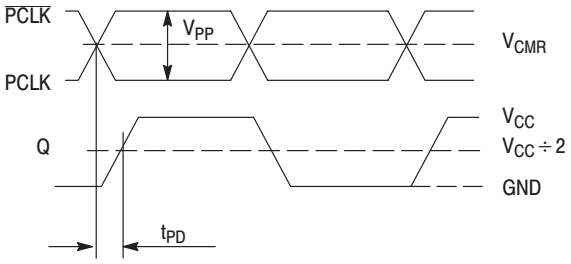
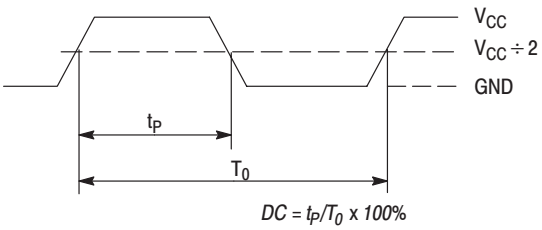
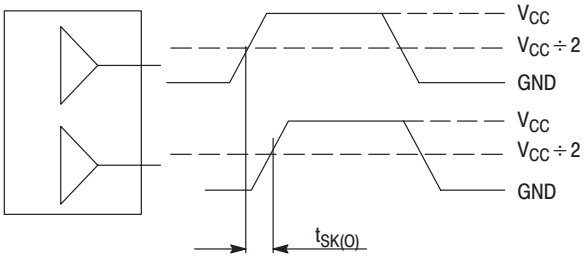



**Figure 8. Propagation delay ($t_{PD}$) test reference**




The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 9. Output Duty Cycle (DC)**




The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 10. Output–to–output Skew $t_{SK(O)}$**

5

# Low Voltage 1:10 CMOS Clock Driver

**MPC946**

**See Upgrade Product – MPC9446**

**LOW VOLTAGE 1:10 CMOS CLOCK DRIVER**

The MPC946 is a low voltage CMOS, 1:10 clock buffer. The 10 outputs can be configured into a standard fanout buffer or into 1X and 1/2X combinations. The ten outputs were designed and optimized to drive 50Ω series or parallel terminated transmission lines. With output to output skews of 350ps the MPC946 is an ideal clock distribution chip for synchronous systems which need a tight level of skew from a large number of outputs. For a similar product with more outputs consult the MPC949 data sheet.

- 2 Selectable LVCMOS/LVTTL Clock Inputs
- 350ps Output to Output Skew
- Drives up to 20 Series Terminated Independent Clock Lines
- Maximum Input/Output Frequency of 150MHz
- Tristatable Outputs
- 32–Lead LQFP Packaging
- 3.3V VCC Supply

**FA SUFFIX**
LQFP PACKAGE
CASE 873A–02

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With an output impedance of approximately 7Ω, in both the HIGH and the LOW logic states, the output buffers of the MPC946 are ideal for driving series terminated transmission lines. More specifically each of the 10 MPC946 outputs can drive two series terminated transmission lines. With this capability, the MPC946 has an effective fanout of 1:20 in applications using point–to–point distribution schemes.

The MPC946 has the capability of generating 1X and 1/2X signals from a 1X source. The design is fully static, the signals are generated and retimed inside the chip to ensure minimal skew between the 1X and 1/2X signals. The device features selectability to allow the user to select the ratio of 1X outputs to 1/2X outputs.

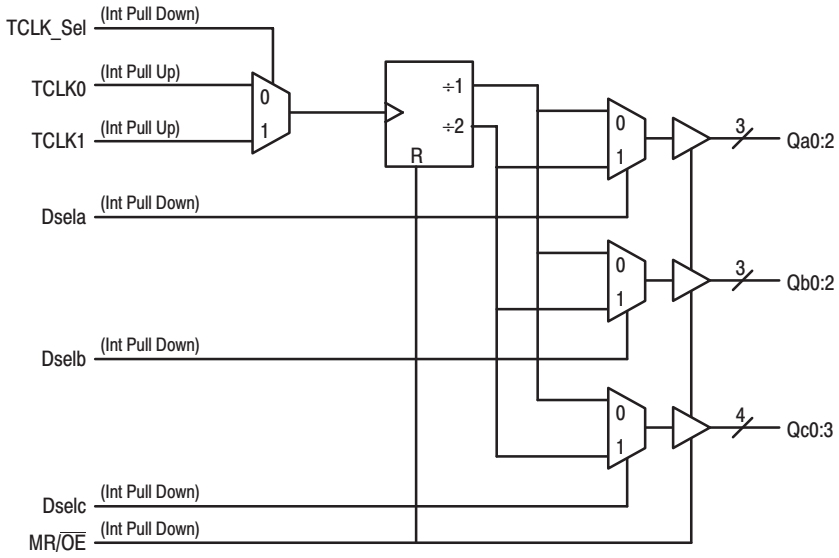
Two independent LVCMOS/LVTTL compatible clock inputs are available. Designers can take advantage of this feature to provide redundant clock sources or the addition of a test clock into the system design. With the TCLK_Sel input pulled HIGH the TCLK1 input is selected.

All of the control inputs are LVCMOS/LVTTL compatible. The Dsel pins choose between 1X and 1/2X outputs. A LOW on the Dsel pins will select the 1X output. The MR/Tristate input will reset the internal flip flops and tristate the outputs when it is forced HIGH.

The MPC946 is fully 3.3V compatible. The 32–lead LQFP package was chosen to optimize performance, board space and cost of the device. The 32–lead LQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

**Rev 2**

## LOGIC DIAGRAM

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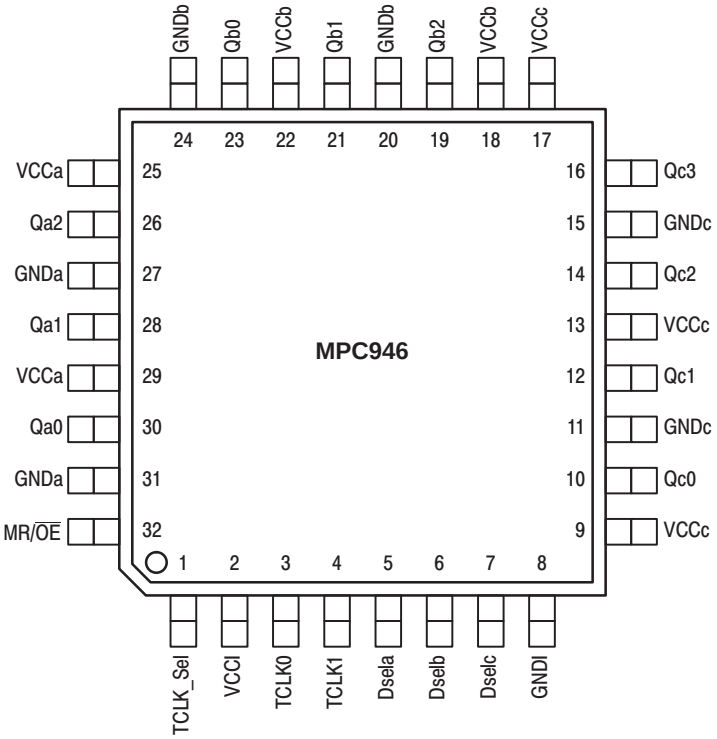
**Pinout: 32–Lead TQFP** (Top View)




### FUNCTION TABLES

| TCLK_Sel | Input |
|---|---|
| 0<br>1 | TCLK0<br>TCLK1 |
| **Dselx** | **Outputs** |
| 0<br>1 | 1x<br>1/2x |
| **MR/$\overline{OE}$** | **Outputs** |
| 0<br>1 | Enabled<br>Hi–Z |

**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 4.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_{IN}$ | Input Current (CMOS Inputs) | | ±20 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±0.3V)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | 3.6 | V | |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | |
| $V_{OH}$ | Output HIGH Voltage | 2.5 | | | V | $I_{OH}$ = –20mA[1] |
| $V_{OL}$ | Output LOW Voltage | | | 0.4 | V | $I_{OL}$ = 20mA[1] |
| $I_{IN}$ | Input Current | | | ±120 | µA | Note 2. |
| $I_{CC}$ | Maximum Quiescent Supply Current | | 70 | 85 | mA | |
| $C_{IN}$ | Input Capacitance | | | 4 | pF | |
| $C_{pd}$ | Power Dissipation Capacitance | | 25 | | pF | Per Output |

1. The MPC946 can drive 50Ω transmission lines on the incident edge. Each output can drive one 50Ω parallel terminated transmission line to the termination voltage of $V_{TT} = V_{CC}/2$. Alternately, the device drives up to two 50Ω series terminated transmission lines.
2. $I_{IN}$ current is a result of internal pull–up/pull–down resistors.

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±0.3V)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $F_{max}$ | Maximum Input Frequency | 150 | | | MHz | Note 1. |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay TCLK to Q | 5.0<br>4.5 | 8.0<br>7.5 | 12.0<br>11.5 | ns | Note 1., 3. |
| $t_{sk(o)}$ | Output–to–Output Skew<br>Same Frequency Outputs<br>Different Frequency Outputs<br>Same Frequency Outputs<br>Different Frequency Outputs | | | <br>350<br>350<br>350<br>450 | ps | Note 1., 3.<br>$F_{max}$ < 100MHz<br>$F_{max}$ < 100MHz<br>$F_{max}$ > 100MHz<br>$F_{max}$ > 100MHz |
| $t_{sk(pp)}$ | Part–to–Part Skew | | 2.0 | 4.5 | ns | Note 2. |
| $t_{PZL}$, $t_{PZH}$ | Output Enable Time | | 3 | 11 | ns | Note 3. |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time | | 3 | 11 | ns | Note 3. |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.1 | 0.5 | 1.0 | ns | 0.8V to 2.0V, Note 3. |

1. Driving 50Ω transmission lines.
2. Part–to–part skew at a given temperature and voltage.
3. Termination is 50Ω to $V_{CC}/2$.

## APPLICATIONS INFORMATION

### Driving Transmission Lines

The MPC946 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC946 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 1 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC946 clock driver is effectively doubled due to its capability to drive multiple lines.

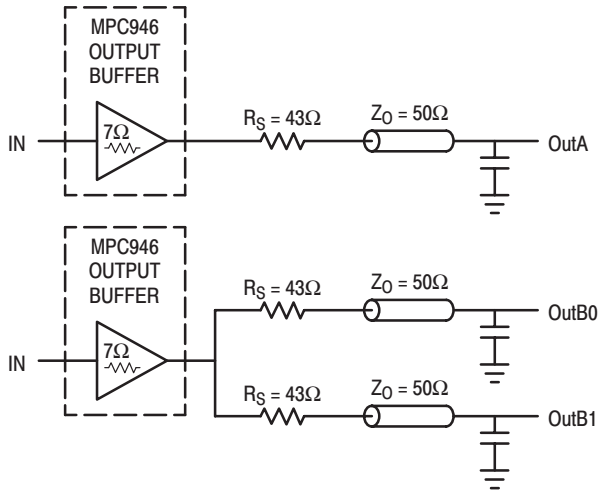



**Figure 1. Single versus Dual Transmission Lines**

The waveform plots of Figure 2 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC946 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC946. The output waveform in Figure 2 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

VL = VS ( Zo / Rs + Ro +Zo) = 3.0 (25/53.5) = 1.40V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

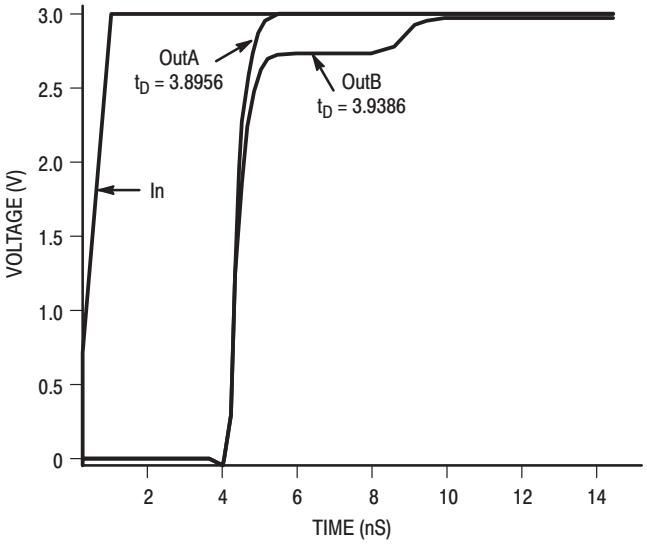
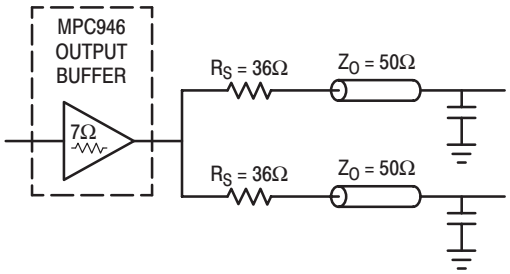



**Figure 2. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 3 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




7Ω + 36Ω || 36Ω = 50Ω || 50Ω
25Ω = 25Ω

**Figure 3. Optimized Dual Line Termination**

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

# Low Voltage 1:9 Clock Distribution Chip

**MPC947**

**See Upgrade Product – MPC9447**

**LOW VOLTAGE 1:9 CLOCK DISTRIBUTION CHIP**

The MPC947 is a 1:9 low voltage clock distribution chip. The device features the capability to select between two LVTTL compatible inputs and fans the signal out to 9 LVCMOS or LVTTL compatible outputs. These 9 outputs were designed and optimized to drive 50Ω series terminated transmission lines. With output–to–output skews of 500ps, the MPC947 is ideal as a clock distribution chip for synchronous systems which need a tight level of skew at a relatively low cost. For a similar product targeted at a higher price/performance point, consult the MPC948 data sheet.

- 2 Selectable LVCMOS/LVTTL Clock Inputs
- 500ps Maximum Output–to–Output Skew
- Drives Up to 18 Independent Clock Lines
- Maximum Output Frequency of 110MHz
- Synchronous Output Enable
- Tristatable Outputs
- 32–Lead LQFP Packaging
- 3.3V $V_{CC}$ Supply Voltage

5

**FA SUFFIX**
32–LEAD LQFP PACKAGE
CASE 873A–02

With an output impedance of approximately 7Ω, in both the HIGH and LOW logic states, the output buffers of the MPC947 are ideal for driving series terminated transmission lines. More specifically, each of the 9 MPC947 outputs can drive two series terminated 50Ω transmission lines. With this capability, the MPC947 has an effective fanout of 1:18 in applications using point–to–point distribution schemes. With this level of fanout, the MPC947 provides enough copies of low skew clocks for high performance synchronous systems, including use as a clock distribution chip for the L2 cache of a **PowerPC** 620 based system.

Two independent LVCMOS/LVTTL compatible clock inputs are available. Designers can take advantage of this feature to provide redundant clock sources or the addition of a test clock into the system design. With the select input pulled HIGH, the TTL_CLK1 input will be selected.

All of the control inputs are LVCMOS/LVTTL compatible. The MPC947 provides a synchronous output enable control to allow for starting and stopping of the output clocks. A logic high on the Sync_OE pin will enable all of the outputs. Because this control is synchronized to the input clock, potential output glitching or runt pulse generation is eliminated. In addition, for board level test, the outputs can be tristated via the tristate control pin. A logic LOW applied to the $\overline{\text{Tristate}}$ input will force all of the outputs into high impedance. Note that all of the MPC947 inputs have internal pullup resistors.

The MPC947 is fully 3.3V compatible. The 32–lead LQFP package was chosen to optimize performance, board space and cost of the device. The 32–lead LQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

**Rev 4**

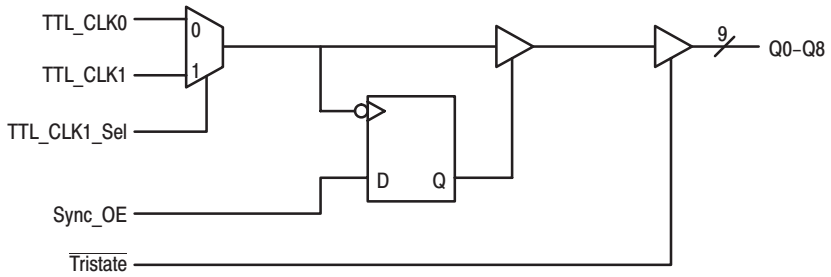



**Figure 1. Logic Diagram**

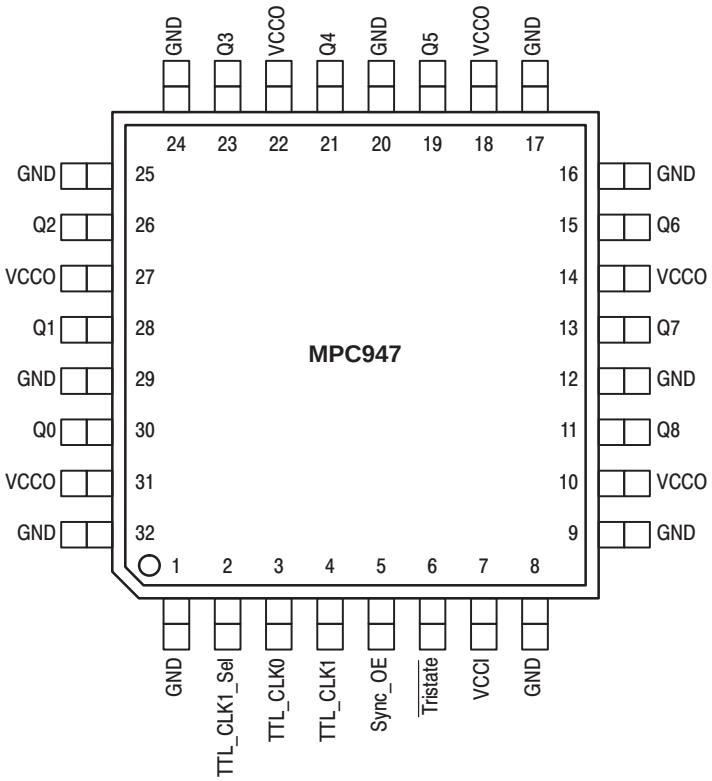



**Figure 2. 32–Lead Pinout** (Top View)

**FUNCTION TABLES**

| **TTL_CLK1_Sel** | **Input** |
|---|---|
| 0 | TTL_CLK0 |
| 1 | TTL_CLK1 |
| **Sync_OE** | **Outputs** |
| 0 | Disabled |
| 1 | Enabled |
| **$\overline{\text{Tristate}}$** | **Outputs** |
| 0 | Tristate |
| 1 | Enabled |

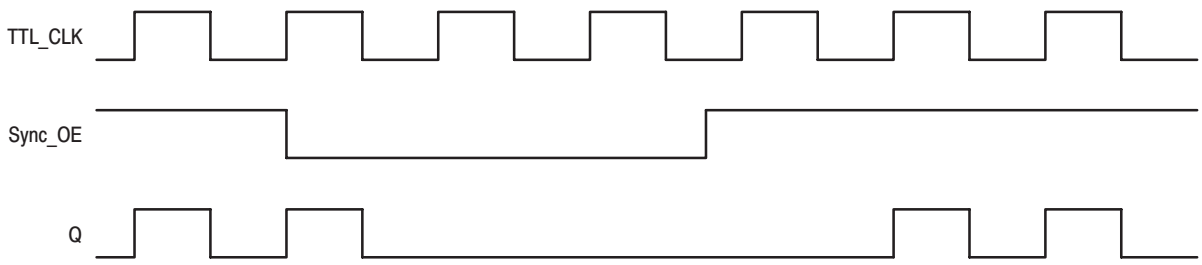



**Figure 3. Sync_OE Timing Diagram**

**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 4.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_{IN}$ | Input Current (CMOS Inputs) | | ±20 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±0.3V)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | 3.6 | V | |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | |
| $V_{OH}$ | Output HIGH Voltage | 2.5 | | | V | $I_{OH}$ = –20mA (Note 1.) |
| $V_{OL}$ | Output LOW Voltage | | | 0.4 | V | $I_{OL}$ = 20mA (Note 1.) |
| $I_{IN}$ | Input Current | | | –100 | µA | Note 2. |
| $I_{CC}$ | Maximum Quiescent Supply Current | | 21 | 28 | mA | |
| $C_{IN}$ | Input Capacitance | | | 4 | pF | |
| $C_{pd}$ | Power Dissipation Capacitance | | 25 | | pF | Per Output |

1. The MPC947 can drive 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to $V_{TT} = V_{CC}/2$. Alternately, the device drives up to two 50Ω series terminated transmission lines per output.
2. $I_{IN}$ current is a result of internal pull–up resistors.

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±0.3V)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $F_{max}$ | Maximum Input Frequency | 110 | | | MHz | Note 3. |
| $t_{pd}$ | Propagation Delay TCLK to Q | 4.75 | | 9.25 | ns | Note 3. |
| $t_{sk(o)}$ | Output–to–Output Skew | | | 500 | ps | Note 3. |
| $t_{sk(pr)}$ | Part–to–Part Skew | | | 2.0 | ns | Notes 3., 4. |
| $t_{pwo}$ | Output Pulse Width | $t_{CYCLE}/2$ – 800 | | $t_{CYCLE}/2$ + 800 | ps | Note 3., Measured at $V_{CC}/2$ |
| $t_s$ | Setup Time Sync_OE to Input Clk | 0.0 | | | ns | Notes 3., 5. |
| $t_h$ | Hold Time Input Clk to Sync_OE | 1.0 | | | ns | Notes 3., 5. |
| $t_{PZL}$, $t_{PZH}$ | Output Enable Time | | | 11 | ns | |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time | | | 11 | ns | |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.2 | | 1.0 | ns | 0.8V to 2.0V |

3. Driving 50Ω terminated to $V_{CC}/2$.
4. Part–to–part skew at a given temperature and voltage.
5. Setup and Hold times are relative to the falling edge of the input clock.

## APPLICATIONS INFORMATION

### Driving Transmission Lines

The MPC947 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC947 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC947 clock driver is effectively doubled due to its capability to drive multiple lines.

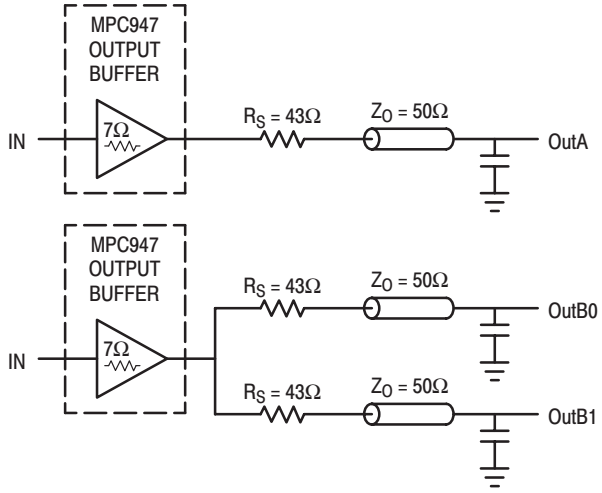



**Figure 4. Single versus Dual Transmission Lines**

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC947 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC947. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

VL = VS ( Zo / Rs + Ro +Zo) = 3.0 (25/53.5) = 1.40V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

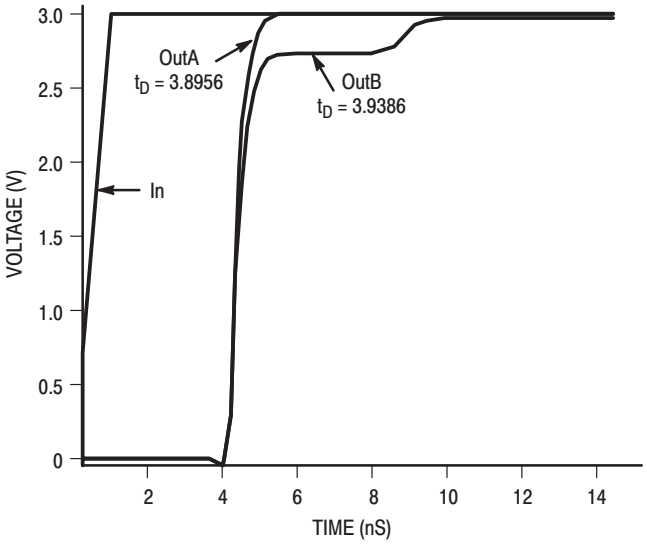
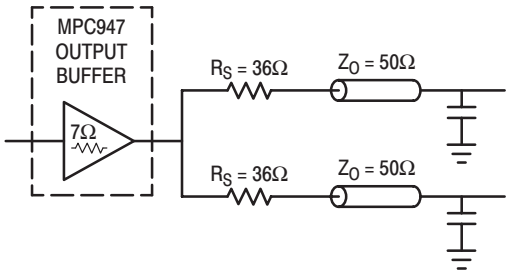



**Figure 5. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




7Ω + 36Ω || 36Ω = 50Ω || 50Ω
25Ω = 25Ω

**Figure 6. Optimized Dual Line Termination**

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

# Low Voltage 1:12 Clock Distribution Chip

**MPC948**

**See Upgrade Product – MPC9448**

**LOW VOLTAGE 1:12 CLOCK DISTRIBUTION CHIP**

The MPC948 is a 1:12 low voltage clock distribution chip. The device features the capability to select either a differential LVPECL or a LVTTL compatible input. The 12 outputs are LVCMOS or LVTTL compatible and feature the drive strength to drive 50Ω series terminated transmission lines. With output–to–output skews of 350ps, the MPC948 is ideal as a clock distribution chip for the most demanding of synchronous systems. For a similar product targeted at a lower price/performance point, please consult the MPC947 data sheet.

- Clock Distribution for **PowerPC**™ 620 L2 Cache
- LVPECL or LVCMOS/LVTTL Clock Input
- 350ps Maximum Output–to–Output Skew
- Drives Up to 24 Independent Clock Lines
- Maximum Output Frequency of 150MHz
- Synchronous Output Enable
- Tristatable Outputs
- 32–Lead LQFP Packaging
- 3.3V $V_{CC}$ Supply Voltage



**FA SUFFIX**
32–LEAD LQFP PACKAGE
CASE 873A–02

With an output impedance of approximately 7Ω, in both the HIGH and LOW logic states, the output buffers of the MPC948 are ideal for driving series terminated transmission lines. More specifically, each of the 12 MPC948 outputs can drive two series terminated 50Ω transmission lines. With this capability, the MPC948 has an effective fanout of 1:24 in applications where each line drives a single load. With this level of fanout, the MPC948 provides enough copies of low skew clocks for high performance synchronous systems, including use as a clock distribution chip for the L2 cache of a **PowerPC** 620 based system.

The differential LVPECL inputs of the MPC948 allow the device to interface directly with a LVPECL fanout buffer like the MC100LVE111 to build very wide clock fanout trees or to couple to a high frequency clock source. The LVCMOS/LVTTL input provides a more standard interface for applications requiring only a single clock distribution chip at relatively low frequencies. In addition, the two clock sources can be used to provide for a test clock interface as well as the primary system clock. A logic HIGH on the TTL_CLK_Sel pin will select the TTL level clock input.

All of the control inputs are LVCMOS/LVTTL compatible. The MPC948 provides a synchronous output enable control to allow for starting and stopping of the output clocks. A logic high on the Sync_OE pin will enable all of the outputs. Because this control is synchronized to the input clock, potential output glitching or runt pulse generation is eliminated. In addition, for board level test, the outputs can be tristated via the tristate control pin. A logic LOW applied to the $\overline{\text{Tristate}}$ input will force all of the outputs into high impedance. Note that all of the MPC948 inputs have internal pullup resistors.

The MPC948 is fully 3.3V compatible. The 32–lead LQFP package was chosen to optimize performance, board space and cost of the device. The 32–lead LQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.



**Rev 4**

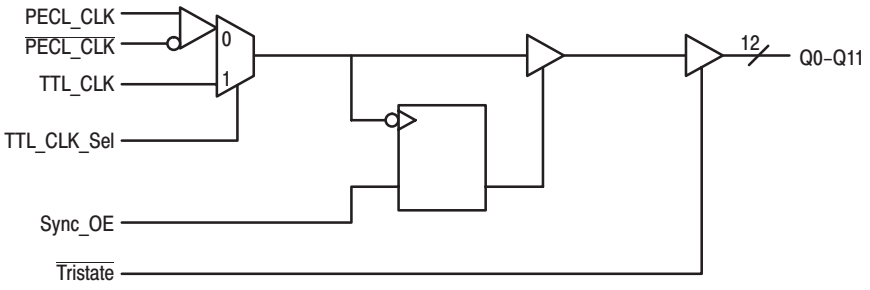



**Figure 1. Logic Diagram**

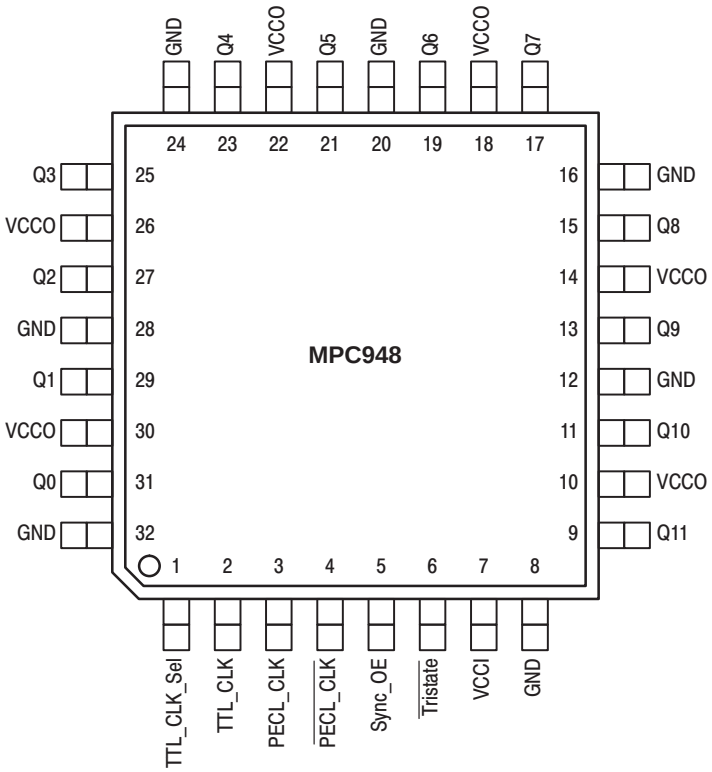



**Figure 2. 32–Lead Pinout** (Top View)

**FUNCTION TABLES**

| **TTL_CLK_Sel** | **Input** |
|---|---|
| 0<br>1 | PECL_CLK<br>TTL_CLK |
| **Sync_OE** | **Outputs** |
| 0<br>1 | Disabled<br>Enabled |
| **$\overline{\text{Tristate}}$** | **Outputs** |
| 0<br>1 | Tristate<br>Enabled |

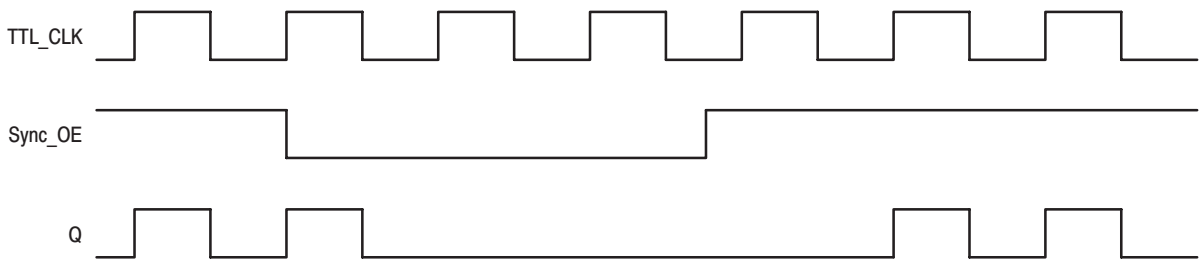



**Figure 3. Sync_OE Timing Diagram**

**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 4.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_{IN}$ | Input Current | | ±20 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±0.3V)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | PECL_CLK<br>Other | 2.135<br>2.0 | | 2.42<br>3.60 | V | Single Ended Spec |
| $V_{IL}$ | Input LOW Voltage | PECL_CLK<br>Other | 1.49 | | 1.825<br>0.8 | V | Single Ended Spec |
| $V_{PP}$ | Peak–to–Peak Input Voltage | PECL_CLK | 300 | | 1000 | mV | |
| $V_{CMR}$ | Common Mode Range | PECL_CLK | $V_{CC}$ – 2.0 | | $V_{CC}$ – 0.6 | V | Note 1. |
| $V_{OH}$ | Output HIGH Voltage | | 2.5 | | | V | $I_{OH}$ = –20mA (Note 2.) |
| $V_{OL}$ | Output LOW Voltage | | | | 0.4 | V | $I_{OL}$ = 20mA (Note 2.) |
| $I_{IN}$ | Input Current | | | | ±100 | µA | Note 3. |
| $C_{IN}$ | Input Capacitance | | | | 4 | pF | |
| $C_{pd}$ | Power Dissipation Capacitance | | | 25 | | pF | Per Output |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | 22 | 30 | mA | |

1. $V_{CMR}$ is the difference from the most positive side of the differential input signal. Normal operation is obtained when the “HIGH” input is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ specification.
2. The MPC948 can drive 50Ω transmission lines on the incident edge. Each output can drive one 50Ω parallel terminated transmission line to the termination voltage of $V_{TT} = V_{CC}/2$. Alternately, the device drives up to two 50Ω series terminated transmission lines.
3. Inputs have pull–up resistors which affect input current, $\overline{\text{PECL\_CLK}}$ has a pull–down resistor.

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±0.3V, Assumes 50% input duty cycle)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $F_{max}$ | Maximum Input Frequency | | 150 | | | MHz | Note 4. |
| $t_{pd}$ | Propagation Delay | PECL_CLK to Q<br>TTL_CLK to Q | 4.0<br>4.4 | | 8.0<br>8.9 | ns | Note 4. |
| $t_{sk(o)}$ | Output–to–Output Skew | | | | 350 | ps | Note 4. |
| $t_{sk(pr)}$ | Part–to–Part Skew | PECL_CLK to Q<br>TTL_CLK to Q | | | 1.5<br>2.0 | ns | Notes 4., 5. |
| $t_{pwo}$ | Output Pulse Width | | $t_{CYCLE}/2$ – 800 | | $t_{CYCLE}/2$ + 800 | ps | Notes 4., 6.<br>Measured at $V_{CC}/2$ |
| $t_s$ | Setup Time | Sync_OE to PECL_CLK<br>Sync_OE to TTL_CLK | 1.0<br>0.0 | | | ns | Notes 4., 7. |
| $t_h$ | Hold Time | PECL_CLK to Sync_OE<br>TTL_CLK to Sync_OE | 0.0<br>1.0 | | | ns | Notes 4., 7. |
| $t_{PZL}$,$t_{PZH}$ | Output Enable Time | | 3 | | 11 | ns | |
| $t_{PLZ}$,$t_{PHZ}$ | Output Disable Time | | 3 | | 11 | ns | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 0.20 | | 1.0 | ns | 0.8V to 2.0V |

4. Driving 50Ω transmission lines.
5. Part–to–part skew at a given temperature and voltage.
6. Assumes 50% input duty cycle.
7. Setup and Hold times are relative to the falling edge of the input clock.

## APPLICATIONS INFORMATION

### Driving Transmission Lines

The MPC948 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC948 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC948 clock driver is effectively doubled due to its capability to drive multiple lines.

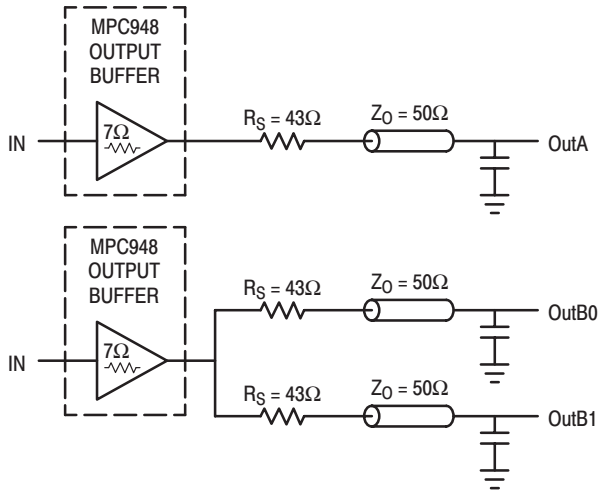



**Figure 4. Single versus Dual Transmission Lines**

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC948 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC948. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

VL = VS ( Zo / Rs + Ro +Zo) = 3.0 (25/53.5) = 1.40V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

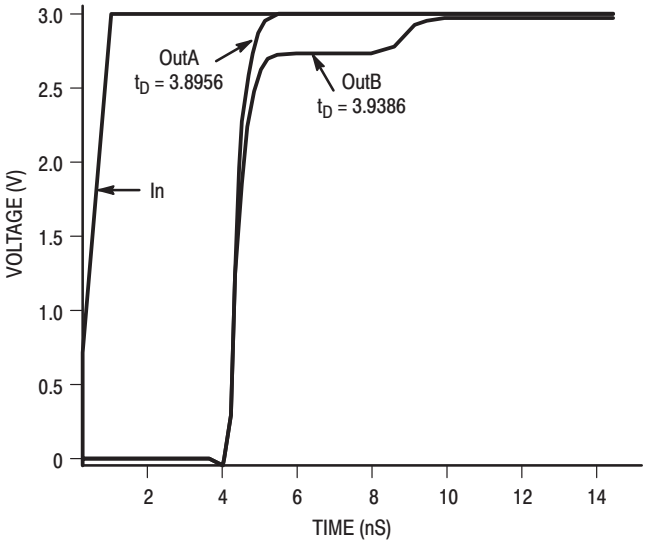
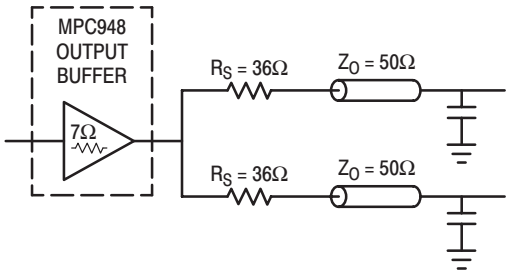



**Figure 5. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




7Ω + 36Ω || 36Ω = 50Ω || 50Ω
25Ω = 25Ω

**Figure 6. Optimized Dual Line Termination**

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

# Low Voltage 1:15 PECL to CMOS Clock Driver

**MPC949**

**See Upgrade Product – MPC9449**

**LOW VOLTAGE 1:15 PECL TO LVCMOS CLOCK DRIVER**

**FA SUFFIX**
52–LEAD LQFP PACKAGE
CASE 848D–03

The MPC949 is a low voltage CMOS, 15 output clock buffer. The 15 outputs can be configured into a standard fanout buffer or into 1X and 1/2X combinations. The device features a low voltage PECL input, in addition to its LVCMOS/LVTTL inputs, to allow it to be incorporated into larger clock trees which utilize low skew PECL devices (see the MC100EP111 data sheet) in the lower branches of the tree. The fifteen outputs were designed and optimized to drive 50Ω series or parallel terminated transmission lines. With output to output skews of 350ps the MPC949 is an ideal clock distribution chip for synchronous systems which need a tight level of skew from a large number of outputs. For a similar product with a smaller fanout and package consult the MPC946 data sheet.

- Low Voltage PECL Clock Input
- 2 Selectable LVCMOS/LVTTL Clock Inputs
- 350ps Maximum Output to Output Skew
- Drives up to 30 Independent Clock Lines
- Maximum Output Frequency of 160MHz
- High Impedance Output Enable
- 52–Lead LQFP Packaging
- 3.3V $V_{CC}$ Supply

5

With an output impedance of approximately 7Ω, in both the HIGH and the LOW logic states, the output buffers of the MPC949 are ideal for driving series terminated transmission lines. More specifically each of the 15 MPC949 outputs can drive two series terminated transmission lines. With this capability, the MPC949 has an effective fanout of 1:30 in applications using point–to–point distribution schemes.

The MPC949 has the capability of generating 1X and 1/2X signals from a 1X source. The design is fully static, the signals are generated and retimed inside the chip to ensure minimal skew between the 1X and 1/2X signals. The device features selectability to allow the user to select the ratio of 1X outputs to 1/2X outputs.

Two independent LVCMOS/LVTTL compatible clock inputs are available. Designers can take advantage of this feature to provide redundant clock sources or the addition of a test clock into the system design. With the TCLK_Sel input pulled HIGH the TCLK1 input is selected. The PCLK_Sel input will select the PECL input clock when driven HIGH.

All of the control inputs are LVCMOS/LVTTL compatible. The Dsel pins choose between 1X and 1/2X outputs. A LOW on the Dsel pins will select the 1X output. The MR/$\overline{OE}$ input will reset the internal flip flops and tristate the outputs when it is forced HIGH.

The MPC949 is fully 3.3V compatible. The 52 lead LQFP package was chosen to optimize performance, board space and cost of the device. The 52–lead LQFP has a 10x10mm body size with a 0.65mm pin spacing.

**Rev 3**

**Figure 1. Logic Diagram**

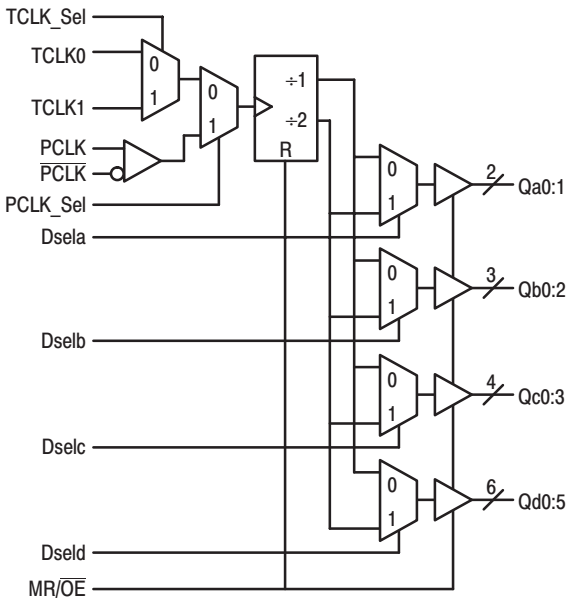
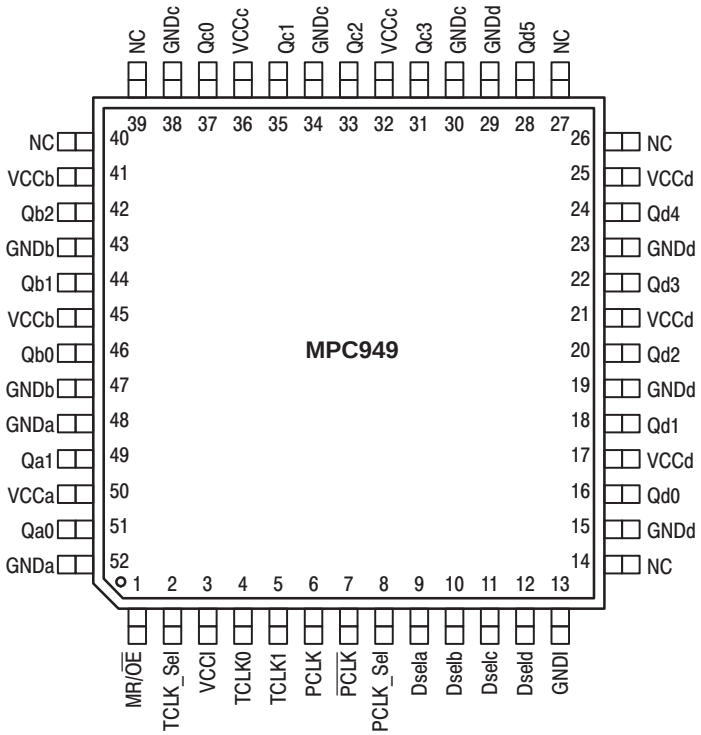



**Figure 2. 52–Lead Pinout** (Top View)

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**FUNCTION TABLE**

| Input | 0 | 1 |
|---|---|---|
| TCLK_Sel | TCLK0 | TCLK1 |
| PCLK_Sel | TCLKn | PCLK |
| Dseln | ÷1 | ÷2 |
| MR/$\overline{OE}$ | Enabled | Hi–Z |

**PIN DESCRIPTION**

| Pin Name | Function |
|---|---|
| TCLK_Sel (Int Pulldown) | Select pin to choose TCKL0 or TCLK1 |
| TCLK0:1 (Int Pullup) | LVCMOS/LVTTL clock inputs |
| PCLK (Int Pulldown) | True PECL clock input |
| $\overline{PCLK}$ (Int Pullup) | Complement PECL clock input |
| Dseln (Int Pulldown) | 1x or 1/2x input divide select pins |
| MR/$\overline{OE}$ (Int Pulldown) | Internal reset and output tristate control pin |
| PCLK_Sel (Int Pulldown) | Select Pin to choose TCLK or PCLK |

**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 4.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_{IN}$ | Input Current | TBD | TBD | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage (Except PECL_CLK) | 2.0 | | 3.60 | V | |
| $V_{IL}$ | Input LOW Voltage (Except PECL_CLK) | | | 0.8 | V | |
| $V_{PP}$ | Peak–to–Peak Input Voltage PECL_CLK | 300 | | 1000 | mV | |
| $V_{CMR}$ | Common Mode Range PECL_CLK | $V_{CC}$ – 2.0 | | $V_{CC}$ – 0.6 | V | Note 1. |
| $V_{OH}$ | Output HIGH Voltage | 2.5 | | | V | $I_{OH}$ = –20mA (Note 2.) |
| $V_{OL}$ | Output LOW Voltage | | | 0.4 | V | $I_{OL}$ = 20mA (Note 2.) |
| $I_{IN}$ | Input Current | | | ±120 | µA | Note 3. |
| $C_{IN}$ | Input Capacitance | | | 4 | pF | |
| $C_{pd}$ | Power Dissipation Capacitance | | 25 | | pF | Per Output |
| $I_{CC}$ | Maximum Quiescent Supply Current | | 70 | 85 | mA | |

1. $V_{CMR}$ is the difference from the most positive side of the differential input signal. Normal operation is obtained when the “HIGH” input is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ specification.
2. The MPC949 can drive 50Ω transmission lines on the incident edge. Each output can drive one 50Ω parallel terminated transmission line to the termination voltage of $V_{TT} = V_{CC}/2$. Alternately, the device drives up to two 50Ω series terminated transmission lines.
3. Inputs have pull–up/pull–down resistors which affect input current.

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $F_{max}$ | Maximum Input Frequency | 160 | | | MHz | Note 4. |
| $t_{PLH}$ | Propagation Delay PECL_CLK to Q<br>TTL_CLK to Q | 4.0<br>4.2 | 6.5<br>7.5 | 9.0<br>10.6 | ns | Note 4. |
| $t_{PHL}$ | Propagation Delay PECL_CLK to Q<br>TTL_CLK to Q | 3.8<br>4.0 | 6.2<br>7.2 | 8.6<br>10.5 | ns | Note 4. |
| $t_{sk(o)}$ | Output–to–Output Skew | | 300 | 350 | ps | Note 4. |
| $t_{sk(pp)}$ | Part–to–Part Skew PECL_CLK to Q<br>TTL_CLK to Q | | 1.5<br>2.0 | 2.75<br>4.0 | ns | Note 5. |
| $t_{PZL}$,$t_{PZH}$ | Output Enable Time | | 3 | 11 | ns | Note 4. |
| $t_{PLZ}$,$t_{PHZ}$ | Output Disable Time | | 3 | 11 | ns | Note 4. |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.10 | | 1.0 | ns | 0.8V to 2.0V |

4. Driving 50Ω transmission lines terminated to $V_{CC}/2$.
5. Part–to–part skew at a given temperature and voltage.

## APPLICATIONS INFORMATION

### Driving Transmission Lines

The MPC949 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC949 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC949 clock driver is effectively doubled due to its capability to drive multiple lines.

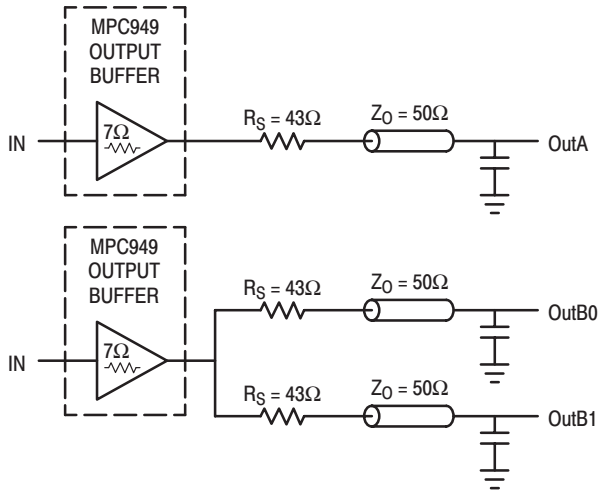



**Figure 3. Single versus Dual Transmission Lines**

The waveform plots of Figure 4 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC949 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC949. The output waveform in Figure 4 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

VL = VS ( Zo / Rs + Ro +Zo) = 3.0 (25/53.5) = 1.40V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

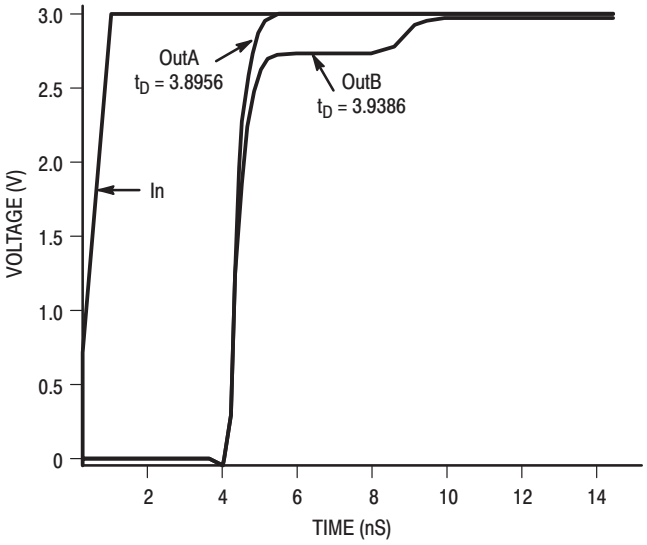
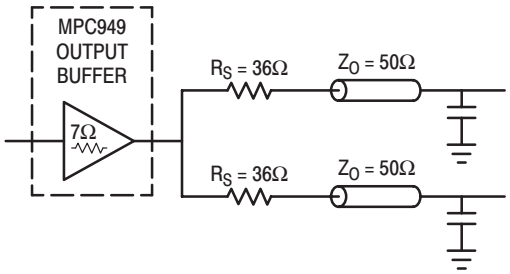



**Figure 4. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.




7Ω + 36Ω || 36Ω = 50Ω || 50Ω
25Ω = 25Ω

**Figure 5. Optimized Dual Line Termination**

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

# Chapter Six
# Differential Fanout Buffer Data Sheets

**Differential Fanout Buffer Device Index**

# Low–Voltage 1:10 Differential ECL/PECL/HSTL Clock Driver

**MC100EP111**

**See Upgrade Product – MC100ES6111**

**LOW–VOLTAGE 1:10 DIFFERENTIAL ECL/PECL/HSTL CLOCK DRIVER**

**FA SUFFIX**
32–LEAD LQFP PACKAGE
CASE 873A–02

The MC100EP111 is a low skew 1–to–10 differential driver, designed with clock distribution in mind. It accepts two clock sources into an input multiplexer. The ECL/PECL input signals can be either differential or single–ended if the $V_{BB}$ output is used. HSTL inputs can be used when the EP111 is operating under PECL conditions. The selected signal is fanned out to 10 identical differential outputs.

- 100ps Part–to–Part Skew typical
- 35ps Output–to–Output Skew typical
- Differential Design
- $V_{BB}$ Output
- Low Voltage $V_{EE}$ Range of –2.25 to –3.8V for ECL
- Low Voltage $V_{CC}$ Range of +2.25 to +3.8V for PECL and HSTL
- 75kΩ Input Pulldown Resistors
- ECL/PECL Outputs

The EP111 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate–to–gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent $t_{pd}$ distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

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To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all ten differential pairs will be used and therefore terminated. In the case where fewer than ten pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

The MC100EP111, as with most other ECL devices, can be operated from a positive $V_{CC}$ supply in PECL mode. This allows the EP111 to be used for high performance clock distribution in +3.3V or +2.5V systems. Designers can take advantage of the EP111's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on using PECL, designers should refer to Motorola Application Note AN1406/D.

The MC100EP111 may be driven single–endedly utilizing the $V_{BB}$ bias output with the $\overline{CLK0}$ input. If a single–ended signal is to be used, the $V_{BB}$ pin should be connected to the $\overline{CLK0}$ input and bypassed to ground via a 0.01 μF capacitor. The $V_{BB}$ output can only source/sink 0.2mA; therefore, it should be used as a switching reference for the MC100EP111 only. Part–to–Part Skew specifications are not guaranteed when driving the MC100EP111 single–endedly.

**Rev 1**

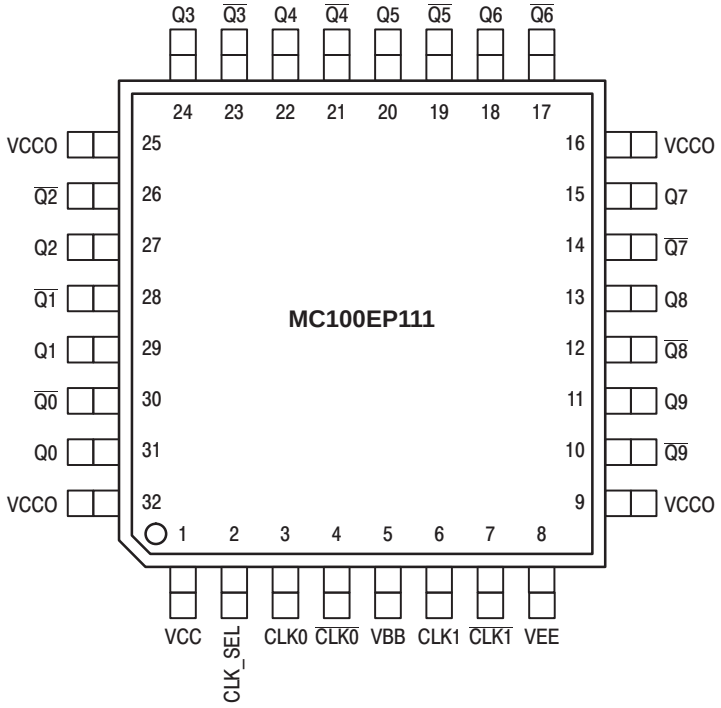


**Figure 1. 32–Lead TQFP Pinout**
(Top View)

**PIN NAMES**

| Pins | Function |
|---|---|
| CLK0, $\overline{\text{CLK0}}$ | Differential ECL/PECL Input Pair |
| CLK1, $\overline{\text{CLK1}}$ | Differential HSTL Input Pair |
| Q0:9, $\overline{\text{Q0:9}}$ | Differential PECL Outputs |
| CLK_SEL | Active Clock Select Input |
| VBB | $V_{BB}$ Output |

**FUNCTION**

| CLK_SEL | Active Input |
|---|---|
| 0 | CLK0, $\overline{\text{CLK0}}$ |
| 1 | CLK1, $\overline{\text{CLK1}}$ |

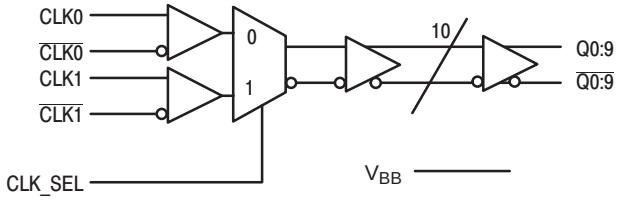


**Figure 2. Logic Symbol**

**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 4.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | Input Current | | ±20 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

**THERMAL CHARACTERISTICS**

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

## DC CHARACTERISTICS

Vsupply : VCC=VCC0 = 0.0 volts, VEE = –2.25 to –3.80 volts

| | | –40°C | | | 25°C | | | 70°C | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **typ** | **Max** | **Min** | **typ** | **Max** | **Min** | **typ** | **Max** | **Unit** | **Condition** |
| IEE | Internal supply current | 45 | | 85 | 60 | | 95 | 65 | | 105 | mA | Absolute value of current |
| ICC | Output and Internal supply current | 270 | | 360 | 290 | | 380 | 300 | | 380 | mA | All outputs terminated 50Ω to VCC–2.0V |
| IIN | Input current | | | 150 | | | 150 | | | 150 | µA | Includes pullup/ pulldown resisters |
| VBB | Internally generated bias voltage | –1.38 | | –1.26 | –1.38 | | –1.26 | –1.38 | | –1.26 | V | for VEE= –3.0 to –3.8 volts |
| VBB | Internally generated bias voltage | –1.38 | | –1.16 | –1.38 | | –1.16 | –1.38 | | –1.16 | V | for VEE= –2.25 to –2.75 volts |
| VIH | Input HIGH voltage (CLK_SEL) | –1.165 | | –0.880 | –1.165 | | –0.880 | –1.165 | | –0.880 | V | |
| VIL | Input LOW voltage (CLK_SEL) | –1.810 | | –1.475 | –1.810 | | –1.475 | –1.810 | | –1.475 | V | |
| VPP | Input amplitude (CLK0,CLK0) | 0.5 | | 1.3 | 0.5 | | 1.3 | 0.5 | | 1.3 | V | Difference of input ≈ VIH – VIL[1] |
| VCMR | Common mode voltage (CLK0,CLK0) | VEE+1.0 | | –0.3 | VEE+1.0 | | –0.3 | VEE+1.0 | | –0.3 | V | Cross point of input ≈ average (VIH,VIL) |
| VOH | Output HIGH voltage | –1.30 | | –0.95 | | | | –1.20 | | –0.90 | | IOH = –30 mA |
| VOL | Output LOW voltage | –1.85 | | –1.40 | | | | –1.90 | | –1.50 | | IOL = –5 mA |
| VOUTpp | Differential output swing | 350 | | | | | | 500 | | | mV | |

## DC CHARACTERISTICS

Vsupply : VCC=VCC0 = 2.25 to 3.80 volts, VEE = 0.0 volts

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| | | –40°C | | | 25°C | | | 70°C | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **typ** | **Max** | **Min** | **typ** | **Max** | **Min** | **typ** | **Max** | **Unit** | **Condition** |
| IEE | Internal supply current | 45 | | 85 | 60 | | 95 | 65 | | 105 | mA | Absolute value of current |
| ICC | Output and Internal supply current | 270 | | 360 | 290 | | 380 | 300 | | 380 | mA | All outputs terminated 50Ω to VCC–2.0V |
| IIN | Input current | | | 150 | | | 150 | | | 150 | µA | Includes pullup/ pulldown resisters |
| VBB | Internally generated bias voltage | VCC–1.38 | | VCC–1.26 | VCC–1.38 | | VCC–1.26 | VCC–1.38 | | VCC–1.26 | V | for VCC= 3.0 to 3.8 volts |
| VBB | Internally generated bias voltage | VCC–1.38 | | VCC–1.16 | VCC–1.38 | | VCC–1.16 | VCC–1.38 | | VCC–1.16 | V | for VCC= 2.25 to 2.75 volts |
| VIH | Input HIGH voltage (CLK_SEL) | VCC–1.165 | | VCC–0.880 | VCC–1.165 | | VCC–0.880 | VCC–1.165 | | VCC–0.880 | V | |
| VIL | Input LOW voltage (CLK_SEL) | VCC–1.810 | | VCC–1.475 | VCC–1.810 | | VCC–1.475 | VCC–1.810 | | VCC–1.475 | V | |
| VPP | Input amplitude (CLK0,CLK0) | 0.5 | | 1.3 | 0.5 | | 1.3 | 0.5 | | 1.3 | V | Difference of input ≈ VIH – VIL[1] |
| VCMR | Common mode voltage (CLK0,CLK0) | 1 | | VCC–0.3 | 1 | | VCC–0.3 | 1 | | VCC–0.3 | V | Cross point of input ≈ average (VIH,VIL) |
| Vdif | Differential input voltage (CLK1,CLK1) | 0.4 | | 1.9 | 0.4 | | 1.9 | 0.4 | | 1.9 | V | Difference of input ≈ VIH – VIL |
| Vx | Input crossover voltage (CLK1,CLK1) | 0.68 | | 0.9 | 0.68 | | 0.9 | 0.68 | | 0.9 | V | Cross point of input ≈ average (VIH,VIL) |

**DC CHARACTERISTICS**
Vsupply : VCC=VCC0 = 2.25 to 3.80 volts, VEE = 0.0 volts

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| VOH | Output HIGH voltage | VCC–1.30 | VCC–0.95 | | VCC–1.20 | VCC–0.90 | | IOH = –30 mA |
| VOL | Output LOW voltage | VCC–1.85 | VCC–1.40 | | VCC–1.90 | VCC–1.50 | | IOL = –5 mA |
| VOUTpp | Differential output swing | 350 | | | 500 | | mV | |

Note 1. VPP minimum and maximum required to maintain AC specifications. Actual device function will tolerate minimum VPP of 100 mV.

**AC CHARACTERISTICS – PECL Input**
Vsupply : VCC=VCC0 = 2.25 to 3.80 volts, VEE = 0.0 volts –OR–
VCC=VCC0 = 0.0 volts, VEE = –2.25 to –3.80 volts

| | | –40°C | | | 25°C | | | 70°C | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **typ** | **Max** | **Min** | **typ** | **Max** | **Min** | **typ** | **Max** | **Unit** | **Condition** |
| Tpd | Differential propagation delay | | | | | | | | | | | Nominal (single input condition VPP = 0.650V, VCMR = VCC–0.800V |
| | CLK0,$\overline{\text{CLK0}}$ to all Q0,$\overline{\text{Q0}}$ thru Q9,$\overline{\text{Q9}}$ | 350 | | 500 | 380 | | 530 | 450 | | 600 | ps | Note 2 |
| Tsk(part) | Part to part skew | | | 150 | | | 150 | | | 150 | ps | Note 2 |
| Tsk(output) | Output to output skew for given part | | 35 | 70 | | 30 | 65 | | 30 | 60 | ps | Note 2 |
| Tpd | Differential propagation delay CLK0,$\overline{\text{CLK0}}$ to all Q0,$\overline{\text{Q0}}$ thru Q9,$\overline{\text{Q9}}$ | 280 | | 600 | 300 | | 620 | 370 | | 700 | ps | Note 2 |
| Tsk(part) | Part to part skew | | | 320 | | | 320 | | | 330 | ps | Note 2 |
| Tsk(output) | Output to output skew for given part | | 35 | 70 | | 30 | 65 | | 30 | 60 | ps | Note 2 |
| Fmax | Maximum frequency | | | 1500 | | | 1500 | | | 1500 | MHz | Functional to 1.5 GHz Timing specifications apply up to 1.0 GHz |
| Tr / Tf | Output rise and fall times (20%, 80%) | 100 | | 300 | 100 | | 300 | 100 | | 300 | ps | All outputs terminated 500Ω to VCC–2.0V |

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**AC CHARACTERISTICS – HSTL Input**

Vsupply : VCC=VCC0 = 2.25 to 3.8 volts, VEE = 0.0 volts

| Symbol | Characteristic | –40°C Min | –40°C typ | –40°C Max | 25°C Min | 25°C typ | 25°C Max | 70°C Min | 70°C typ | 70°C Max | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Tpd | Differential propagation delay | | | | | | | | | | | Nominal (single input condition Vdif = 1.000V, Vx = VEE+0.750V |
| | CLK1,$\overline{\text{CLK1}}$ to all Q0,$\overline{\text{Q0}}$ thru Q9,$\overline{\text{Q9}}$ | 380 | | 530 | 420 | | 570 | 500 | | 650 | ps | Note 2 |
| Tsk(part) | Part to part skew | | | 150 | | | 150 | | | 150 | ps | Note 2 |
| Tsk(output) | Output to output skew for given part | | 35 | 70 | | 30 | 65 | | 30 | 60 | ps | Note 2 |
| Tpd | Differential propagation delay | | | | | | | | | | | All input conditions (full input range) |
| | CLK1,$\overline{\text{CLK1}}$ to all Q0,$\overline{\text{Q0}}$ thru Q9,$\overline{\text{Q9}}$ | 300 | | 600 | 350 | | 650 | 430 | | 750 | ps | Note 2 |
| Tsk(part) | Part to part skew | | | 300 | | | 300 | | | 320 | ps | Note 2 |
| Tsk(output) | Output to output skew for given part | | 35 | 70 | | 30 | 65 | | 30 | 60 | ps | Note 2 |
| Fmax | Maximum frequency | | | 250 | | | 250 | | | 250 | MHz | Functional to 250 MHz Timing specifications apply up to 250 MHz |
| Tr / Tf | Output rise and fall times (20%, 80%) | 100 | | 300 | 100 | | 300 | 100 | | 300 | ps | All outputs terminated 500Ω to VCC–2.0V |

Note 2. For operation with 2.5 volt supply, the output termination is 50Ω to VEE. For operation at 3.3 volt supply, the output termination is 50Ω to VCC–2v.

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# Low–Voltage 1:5 Dual Differential ECL/PECL Clock Driver

**MC100EP210**

**See Upgrade Product – MC100ES6210**

**LOW–VOLTAGE 1:5 DUAL DIFFERENTIAL ECL/PECL CLOCK DRIVER**

The MC100EP210 is a low skew 1–to–5 dual differential driver, designed with clock distribution in mind. The input signals can be either differential or single–ended if the $V_{BB}$ output is used. The signal is fanned out to 5 identical differential outputs.

- 150ps Part–to–Part Skew typical
- 35ps Output–to–Output Skew typical
- Differential Design
- $V_{BB}$ Output
- Voltage and Temperature Compensated Outputs
- Low Voltage $V_{EE}$ Range of –2.25 to –3.8V
- 75kΩ Input Pulldown Resistors

**FA SUFFIX**
32–LEAD LQFP PACKAGE
CASE 873A–02

The EP210 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate–to–gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent $t_{pd}$ distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all ten differential pairs will be used and therefore terminated. In the case where fewer than ten pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

6

The MC100EP210, as with most other ECL devices, can be operated from a positive $V_{CC}$ supply in PECL mode. This allows the EP210 to be used for high performance clock distribution in +3.3V or +2.5V systems. Designers can take advantage of the EP210's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on using PECL, designers should refer to Motorola Application Note AN1406/D.

The MC100EP210 may be driven single–endedly utilizing the $V_{BB}$ bias output with the $\overline{CLKA}$ or $\overline{CLKB}$ input. If a single–ended signal is to be used, the $V_{BB}$ pin should be connected to the $\overline{CLKA}$ or $\overline{CLKB}$ input and bypassed to ground via a 0.01 µF capacitor. The $V_{BB}$ output can only source/sink 0.3mA; therefore, it should be used as a switching reference for the MC100EP210 only. Part–to–Part Skew specifications are not guaranteed when driving the MC100EP210 single–endedly.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.
**Rev 2**

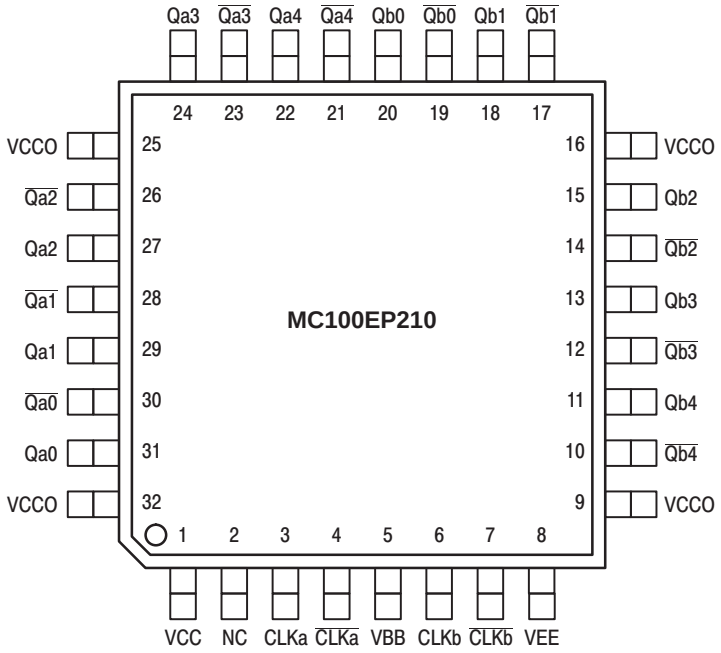


**Figure 1. 32–Lead TQFP Pinout**
(Top View)

**PIN NAMES**

| Pins | Function |
|---|---|
| CLKn, $\overline{\text{CLKn}}$<br>Qn0:4, $\overline{\text{Qn0:4}}$<br>VBB | Differential Input Pairs<br>Differential Outputs<br>$V_{BB}$ Output |

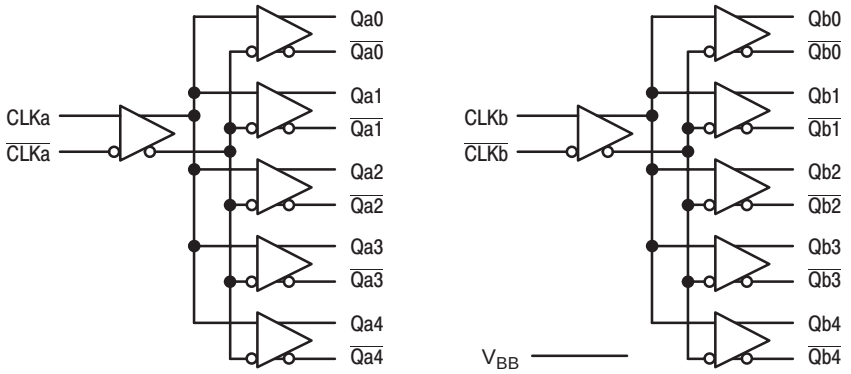


**Figure 2. Logic Symbol**

**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 4.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | Input Current | | ±20 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

**THERMAL CHARACTERISTICS**

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

## DC CHARACTERISTICS

Vsupply : VCC=VCC0 = 0.0 volts, VEE = –2.25 to –3.80 volts

| | | –40°C | | | 25°C | | | 70°C | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **typ** | **Max** | **Min** | **typ** | **Max** | **Min** | **typ** | **Max** | **Unit** | **Condition** |
| IEE | Internal supply current | 20 | | 75 | 20 | | 75 | 30 | | 85 | mA | Absolute value of current |
| ICC | Output and Internal supply current | 270 | | 360 | 270 | | 360 | 270 | | 380 | mA | All outputs terminated 50Ω to VCC–2.0V |
| IIN | Input current | | | 150 | | | 150 | | | 150 | µA | Includes pullup/ pulldown resisters |
| VBB | Internally generated bias voltage | –1.38 | | –1.26 | –1.38 | | –1.26 | –1.38 | | –1.26 | V | for VEE= –3.0 to –3.8 volts |
| VBB | Internally generated bias voltage | –1.38 | | –1.16 | –1.38 | | –1.16 | –1.38 | | –1.16 | V | for VEE= –2.25 to –2.75 volts |
| VPP | Input amplitude | 0.5 | | 1.3 | 0.5 | | 1.3 | 0.5 | | 1.3 | V | Difference of input ≈ VIH – VIL[1] |
| VCMR | Common mode voltage | VEE+1.0 | | –0.3 | VEE+1.0 | | –0.3 | VEE+1.0 | | –0.3 | V | Cross point of input ≈ average (VIH,VIL) |
| VOH | Output HIGH voltage | –1.30 | | –0.95 | | | | –1.20 | | –0.90 | | IOH = –30 mA |
| VOL | Output LOW voltage | –1.85 | | –1.40 | | | | –1.90 | | –1.50 | | IOL = –5 mA |
| VOUTpp | Differential output swing | 350 | | | | | | 500 | | | mV | |

## DC CHARACTERISTICS

Vsupply : VCC=VCC0 = 2.25 to 3.80 volts, VEE = 0.0 volts

| | | –40°C | | | 25°C | | | 70°C | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **typ** | **Max** | **Min** | **typ** | **Max** | **Min** | **typ** | **Max** | **Unit** | **Condition** |
| IEE | Internal supply current | 20 | | 75 | 20 | | 75 | 30 | | 85 | mA | Absolute value of current |
| ICC | Output and Internal supply current | 270 | | 360 | 270 | | 360 | 270 | | 380 | mA | All outputs terminated 50Ω to VCC–2.0V |
| IIN | Input current | | | 150 | | | 150 | | | 150 | µA | Includes pullup/ pulldown resisters |
| VBB | Internally generated bias voltage | VCC–1.38 | | VCC–1.26 | VCC–1.38 | | VCC–1.26 | VCC–1.38 | | VCC–1.26 | V | for VCC= 3.0 to 3.8 volts |
| VBB | Internally generated bias voltage | VCC–1.38 | | VCC–1.16 | VCC–1.38 | | VCC–1.16 | VCC–1.38 | | VCC–1.16 | V | for VCC= 2.25 to 2.75 volts |
| VPP | Input amplitude | 0.5 | | 1.3 | 0.5 | | 1.3 | 0.5 | | 1.3 | V | Difference of input ≈ VIH – VIL[1] |
| VCMR | Common mode voltage | 1 | | VCC–0.3 | 1 | | VCC–0.3 | 1 | | VCC–0.3 | V | Cross point of input ≈ average (VIH,VIL) |
| VOH | Output HIGH voltage | VCC–1.30 | | VCC–0.95 | | | | VCC–1.20 | | VCC–0.90 | | IOH = –30 mA |
| VOL | Output LOW voltage | VCC–1.85 | | VCC–1.40 | | | | VCC–1.90 | | VCC–1.50 | | IOL = –5 mA |
| VOUTpp | Differential output swing | 350 | | | | | | 500 | | | mV | |

Note 1. VPP minimum and maximum required to maintain AC specifications. Actual device function will tolerate minimum VPP of 100 mV.

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## AC CHARACTERISTICS

Vsupply : VCC=VCC0 = 2.25 to 3.80 volts, VEE = 0.0 volts – OR – VCC=VCC0 = 0.0 volts, VEE = –2.25 to –3.80 volts

| | | –40°C | | | 25°C | | | 70°C | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **typ** | **Max** | **Min** | **typ** | **Max** | **Min** | **typ** | **Max** | **Unit** | **Condition** |
| Tpd | Differential propagation delay | | | | | | | | | | | Nominal (single input condition VPP = 0.650V, VCMR = VCC–0.800V |
| | CLK,$\overline{\text{CLK}}$ to all Q0,$\overline{\text{Q0}}$ thru Q4,$\overline{\text{Q4}}$ | 270 | | 420 | 300 | | 450 | 380 | | 530 | ps | Applies to 500 MHz reference. Note 2 |
| Tsk(part) | Part to part skew | | | 150 | | | 150 | | | 150 | ps | At single frequency. Note 2 |
| Tsk(output) | Output to output skew for given part | | 15 | 50 | | 15 | 50 | | 15 | 50 | ps | Note 2 |
| Tpd | Differential propagation delay | | | | | | | | | | | All input conditions |
| | CLK,$\overline{\text{CLK}}$ to all Q0,$\overline{\text{Q0}}$ thru Q4,$\overline{\text{Q4}}$ | 220 | | 520 | 250 | | 550 | 320 | | 620 | ps | Note 2 |
| Tsk(part) | Part to part skew | | | 300 | | | 300 | | | 300 | ps | Note 2 |
| Tsk(output) | Output to output skew for given part | | 15 | 50 | | 15 | 50 | | 15 | 50 | ps | Note 2 |
| Fmax | Maximum frequency | | | 1500 | | | 1500 | | | 1500 | MHz | Functional to 1.5 GHz Timing specifications apply up to 1.0 GHz |
| Tr / Tf | Output rise and fall times (20%, 80%) | 100 | | 300 | 100 | | 300 | 100 | | 300 | ps | Note 2 |

Note 2. For operation with 2.5 volt supply, the output termination is 50Ω to VEE. For operation at 3.3 volt supply, the output termination is 50Ω to VCC–2v.

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**Order this document by MC100EP220/D**

# Low-Voltage Dual 1:10 Differential ECL/PECL Clock Driver

**MC100EP220**

**See Upgrade Product – MC100ES6220**

**LOW–VOLTAGE DUAL 1:10 DIFFERENTIAL ECL/PECL CLOCK DRIVER**

**TB SUFFIX**
52–LEAD LQFP PACKAGE
EXPOSED PAD
CASE 1336

The MC100EP220 is a dual low skew 1–to–10 differential driver, designed with clock distribution in mind. The $V_{BB}$ output provides a DC threshold bias for single ended sources. The $V_{BB}$ can be connected to the true input or the complementary input, the latter will produce an inverted output. If used, the $V_{BB}$ output should be bypassed to ground.

- 225ps Max. Part–to–Part Skew
- 60ps Output–to–Output Skew
- Differential Design
- $V_{BB}$ Output
- Voltage and Temperature Compensated Outputs
- Low Voltage $V_{EE}$ Range of –2.375 to –3.8V
- 65kΩ Input Pulldown Resistors

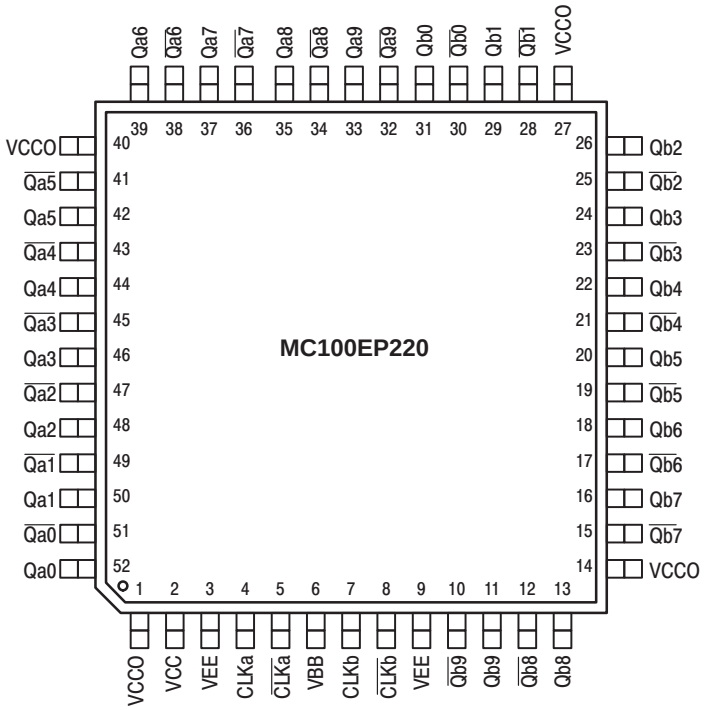
The EP220 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate–to–gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent $t_{pd}$ distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met it is necessary that both pairs of the differential outputs are terminated into 50Ω, even if only one side is being used. In applications which do not use all of the outputs, it is best to leave unused pairs open to minimize power consumption in the device.

The MC100EP220, as with most other ECL devices, can be operated from a positive $V_{CC}$ supply in PECL mode. This allows the EP220 to be used for high performance clock distribution in +3.3V or +2.5V systems. Designers can take advantage of the EP220's performance to distribute low skew clocks across the backplane. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on using PECL, designers should refer to Motorola Application Note AN1406/D.



**Rev 1**




**Pinout: 52–Lead LQFP**
(Top View)

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**LOGIC SYMBOL**

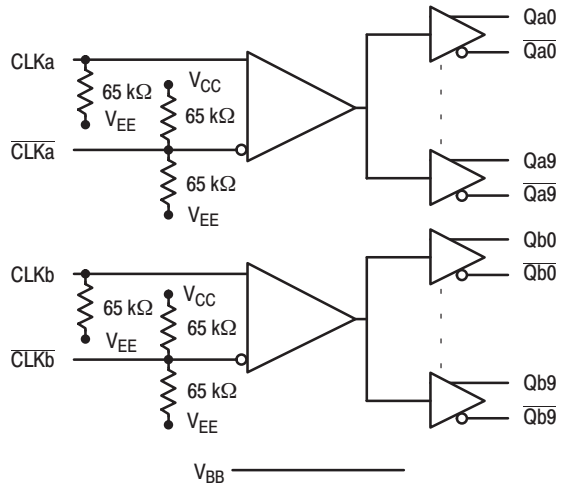

**Table 1: PIN CONFIGURATION**

| Pin | I/O | Type | Function |
|---|---|---|---|
| CLKA, $\overline{\text{CLKA}}$ | Input | ECL/LVPECL | Differential reference clock signal input for fanout buffer A |
| CLKB, $\overline{\text{CLKB}}$ | Input | ECL/LVPECL | Differential reference clock signal input for fanout buffer B |
| Q[0-19], $\overline{\text{Q[0-19]}}$ | Output | LVPECL | Differential clock outputs |
| VEE[a] | Supply | | Negative power supply |
| $V_{CC}$, $V_{CCO}$ | Supply | | Positive power supply. All $V_{CC}$ and $V_{CCO}$ pins must be connected to the positive power supply for correct DC and AC operation |
| $V_{BB}$ | Output | | DC bias output for single ended input operation |

a. In ECL mode (negative power supply mode), VEE is either -3.3V or -2.5V and VCC is connected to GND (0V). In PECL mode (positive power supply mode), VEE is connected to GND (0V) and VCC is either +3.3V or +2.5V. In both modes, the input and output levels are referrenced to the most positive supply (VCC).

**Table 2: ABSOLUTE MAXIMUM RATINGS[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 4.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -65 | 125 | °C | |

a. Absolute maximum continuos ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 3: GENERAL SPECIFICATIONS**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output termination voltage | | $V_{CC}$ - 2[a] | | V | |
| MM | ESD Protection (Machine model) | 75 | | | V | |
| HBM | ESD Protection (Human body model) | 1500 | | | V | |
| CDM | ESD Protection (Charged device model) | 500 | | | V | |
| LU | Latch-up immunity | 200 | | | mA | |
| $C_{IN}$ | | | 4.0 | | pF | Inputs |
| $\theta_{JA}$ | Thermal resistance junction to ambient | See application information[b] | | | | |
| $\theta_{JC}$ | Thermal resistance junction to case | See application information | | | | |

a. Output termination voltage $V_{TT}$ = 0V for $V_{CC}$=2.5V operation is supported but the power consumption of the device will increase.

b. Proper thermal management is critical for reliable system operation. This especially true for high-fanout and high drive capability products. Thermal package information and exposed pad land pattern design recommendations are available in the applications section of this datasheet. In addition, the means of calculating die power consumption, the corresponding die temperature and the relationship to long-term reliability is addressed in the Motorola application note AN1545. Thermal modeling is recommended for the MC100EP220.

**Table 4: PECL DC Characteristics** ($V_{CCO}$ = $V_{CC}$ = 2.375V to 3.8V, $V_{EE}$ = GND)

| Symbol | Characteristics | $T_A$ = -40°C | | $T_A$ = 25°C | | $T_A$ = 85°C | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Clock input pair CLKA, $\overline{CLKA}$, CLKB, $\overline{CLKB}$ (LVPECL differential signals) | | | | | | | | | |
| $V_{PP}$ | Differential input voltage[a] $V_{CC}$=3.3V<br>$V_{CC}$=2.5V | 0.10<br>0.15 | | 0.10<br>0.15 | | 0.10<br>0.15 | | V<br>V | |
| $V_{CMR}$ | Differential cross point voltage[b] CLKA, CLKB | 1.0 | $V_{CC}$-0.4 | 1.0 | $V_{CC}$-0.4 | 1.0 | $V_{CC}$-0.4 | V | |
| All inputs (LVPECL single ended signals) | | | | | | | | | |
| $V_{IH}$ | Input high voltage | $V_{CC}$-1.14 | | $V_{CC}$-1.14 | | $V_{CC}$-1.14 | | V | |
| $V_{IL}$ | Input low voltage | | $V_{CC}$-1.46 | | $V_{CC}$-1.46 | | $V_{CC}$-1.46 | V | |
| $I_{IH}$ | Input Current | | 150 | | 150 | | 150 | µA | $V_{IN}$ = $V_{CC}$ to $V_{EE}$ |
| LVPECL clock outputs (Q0-19, $\overline{Q0\text{-}19}$) | | | | | | | | | |
| $V_{OH}$ | Output High Voltage | $V_{CC}$-1.20 | $V_{CC}$-0.82 | $V_{CC}$-1.15 | $V_{CC}$-0.82 | $V_{CC}$-1.15 | $V_{CC}$-0.82 | V | $I_{OH}$= -30mA[c] |
| $V_{OL}$ | Output Low Voltage | $V_{CC}$-1.90 | $V_{CC}$-1.40 | $V_{CC}$-1.90 | $V_{CC}$-1.40 | $V_{CC}$-1.9 | $V_{CC}$-1.40 | V | $I_{OL}$= -5mA[c] |
| Supply current and $V_{BB}$ | | | | | | | | | |
| $I_{EE}$ | Max. Supply Current | | 190 | | 190 | | 190 | mA | $V_{EE}$ pin |
| $I_{CC}$ | Max. Supply Current[d] | | 750 | | 750 | | 750 | mA | $V_{CC}$ pins |
| $V_{BB}$ | Output reference voltage[e] | $V_{CC}$-1.36 | $V_{CC}$-1.24 | $V_{CC}$-1.36 | $V_{CC}$-1.24 | $V_{CC}$-1.36 | $V_{CC}$-1.24 | V | |

a. $V_{PP}$ is the minimum differential input voltage swing required to maintain device functionality.
b. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.
c. Equivalent to an output termination of 50Ω to $V_{TT}$.
d. $I_{CC}$ includes current through the output resistors (all outputs terminated 50Ω to $V_{TT}$).
e. $V_{BB}$ output can be used to bias the complementary input when the device is used with single ended clock signals. $V_{BB}$ can sink max. 0.3 mA DC current.

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**Table 5: ECL DC Characteristics** ($V_{CC}$ = $V_{CCO}$ = GND, $V_{EE}$ = -3.8V to -2.375V)

| Symbol | Characteristics | $T_A$ = -40°C | | $T_A$ = 25°C | | $T_A$ = 85°C | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Clock input pair CLKA, $\overline{CLKA}$, CLKB, $\overline{CLKB}$ for ECL differential signals | | | | | | | | | |
| $V_{PP}$ | Differential input voltage[a] $V_{EE}$=-3.3V<br>$V_{EE}$=-2.5V | 0.10<br>0.15 | | 0.10<br>0.15 | | 0.10<br>0.15 | | V<br>V | |
| $V_{CMR}$ | Differential cross point voltage[b] | $V_{EE}$+1.0 | -0.4 | $V_{EE}$+1.0 | -0.4 | $V_{EE}$+1.0 | -0.4 | V | |
| All inputs ECL single ended signals | | | | | | | | | |
| $V_{IH}$ | Input high voltage | -1.14 | | -1.14 | | -1.14 | | V | |
| $V_{IL}$ | Input low voltage | | -1.46 | | -1.46 | | -1.46 | V | |
| $I_{IH}$ | Input Current | | 150 | | 150 | | 150 | µA | $V_{IN}$ = $V_{EE}$ to $V_{CC}$ |
| LVPECL clock outputs (Q0-19, $\overline{Q0\text{-}19}$) | | | | | | | | | |
| $V_{OH}$ | Output High Voltage | -1.20 | -0.82 | -1.15 | -0.82 | -1.15 | -0.82 | V | $I_{OH}$= -30 mA[c] |
| $V_{OL}$ | Output Low Voltage | -1.90 | -1.40 | -1.90 | -1.40 | -1.90 | -1.40 | V | $I_{OL}$= -5 mA[c] |
| Supply current and $V_{BB}$ | | | | | | | | | |
| $I_{EE}$ | Max. Supply Current | | 190 | | 190 | | 190 | mA | $V_{EE}$ pin |
| $I_{CC}$ | Max. Supply Current[d] | | 750 | | 750 | | 750 | mA | $V_{CC}$ Pins |
| $V_{BB}$ | Output reference voltage[e] | -1.36 | -1.24 | -1.36 | -1.24 | -1.36 | -1.24 | V | |

a. $V_{PP}$ is the minimum differential input voltage swing required to maintain device functionality.
b. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.
c. Equivalent to an output termination of 50Ω to $V_{TT}$.
d. $I_{CC}$ includes current through the output resistors (all outputs terminated 50Ω to $V_{TT}$).
e. $V_{BB}$ output can be used to bias the complementary input when the device is used with single ended clock signals. $V_{BB}$ can sink max. 0.3 mA DC current.

**Table 6: PECL/ECL AC Characteristics**[a] ($V_{CC}$ = $V_{CCO}$ = 2.375V to 3.8V, $V_{EE}$ = GND) or ($V_{EE}$ = -3.8V to -2.375V, $V_{CC}$ = $V_{CCO}$ = GND)

| Symbol | Characteristics | $T_A$ = -40°C | | | $T_A$ = 25°C | | | $T_A$ = 85°C | | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| Clock input pair CLKA, $\overline{\text{CLKA}}$, CLKB, $\overline{\text{CLKB}}$ for PECL differential signals | | | | | | | | | | | | |
| $V_{PP}$ | Differential input voltage[b] (peak-to-peak) | 0.4 | | 1.0 | 0.4 | | 1.0 | 0.4 | | 1.0 | V | |
| $V_{CMR}$ | Differential cross point voltage[c] | 1.0 | | $V_{CC}$-0.4 | 1.0 | | $V_{CC}$-0.4 | 1.0 | | $V_{CC}$-0.4 | V | |
| $f_{CLK}$ | Input Frequency (PECL) | 0 | | 1.0 | 0 | | 1.0 | 0 | | 1.0 | GHz | |
| Clock input pair CLKA, $\overline{\text{CLKA}}$, CLKB, $\overline{\text{CLKB}}$ for ECL differential signals | | | | | | | | | | | | |
| $V_{PP}$ | Differential input voltage (peak-to-peak) | 0.4 | | 1.0 | 0.4 | | 1.0 | 0.4 | | 1.0 | V | |
| $V_{CMR}$ | Differential cross point voltage | $V_{EE}$+1.0 | | -0.4 | $V_{EE}$+1.0 | | -0.4 | $V_{EE}$+1.0 | | -0.4 | V | |
| $f_{CLK}$ | Input Frequency (ECL) | 0 | | 1.0 | 0 | | 1.0 | 0 | | 1.0 | GHz | |
| PECL/ECL clock outputs (Q0-19, $\overline{\text{Q0-19}}$) | | | | | | | | | | | | |
| $t_{PD}$ | Propagation Delay CLKA or CLKB to Qx | 300 | 400 | 500 | 350 | 450 | 550 | 425 | 535 | 650 | ps | |
| $V_{O(P-P)}$ | Differential output voltage (peak-to-peak) | 450 | 700 | | 500 | 700 | | 500 | 700 | | mV | |
| $t_{sk(O)}$ | Output-to-output skew (within device) | | 35 | 60 | | 35 | 60 | | 35 | 60 | ps | Diff. |
| $t_{sk(PP)}$ | Output-to-output skew (part-to-part) | | | 200 | | | 200 | | | 225 | ps | Diff. |
| $t_{JIT(CC)}$ | Output cycle-to-cycle jitter (RMS) | | | TBD | | | TBD | | | TBD | ps | |
| $DC_O$ | Positive output pulse width | $t_p$ – 50 | $t_p$ | $t_p$ + 50 | $t_p$ – 50 | $t_p$ | $t_p$ + 50 | $t_p$ – 50 | $t_p$ | $t_p$ + 50 | ps | $t_p$ input positive pulse width |
| $t_r$, $t_f$ | Output Rise/Fall Time | 100 | | 500 | 100 | | 500 | 100 | | 500 | ps | 20% to 80% |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
b. $V_{PP}$ (AC) is the minimum differential input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
c. $V_{CMR}$ (AC) is the crosspoint of the differential input signal. AC operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ (AC) or $V_{PP}$ (AC) impacts the device propagation delay and part-to-part skew.

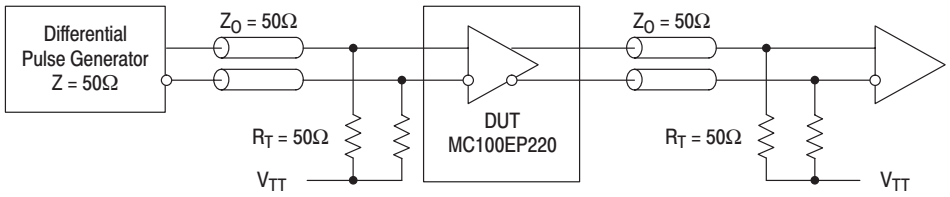



**Figure 1. MC100EP220 AC test reference**

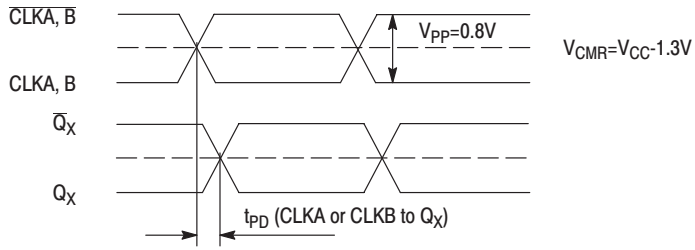



**Figure 2. MC100EP220 AC reference measurement waveform**

## APPLICATIONS INFORMATION

### Using the thermally enhanced package of the MC100EP220

The MC100EP220 uses a thermally enhanced exposed pad (EP) 52 lead LQFP package. The package is molded so that the leadframe is exposed at the surface of the package bottom side. The exposed metal pad will provide the low thermal impedance that supports the power consumption of the MC100EP220 high-speed bipolar integrated circuit and eases the power management task for the system design. A thermal land pattern on the printed circuit board and thermal vias are recommended in order to take advantage of the enhanced thermal capabilities of the MC100EP220. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal path. In multilayer board designs, thermal vias thermally connect the exposed pad to internal copper planes. Number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package. A nine thermal via array, arranged in a 3 x 3 array and using a 1.2 mm pitch in the center of the thermal land is the absolute minimum requirement for MC100EP220 applications on multi-layer boards. The recommended thermal land design comprises a 5 x 5 thermal via array as shown in Figure 3 “Recommended thermal land pattern”, providing an efficient heat removal path.

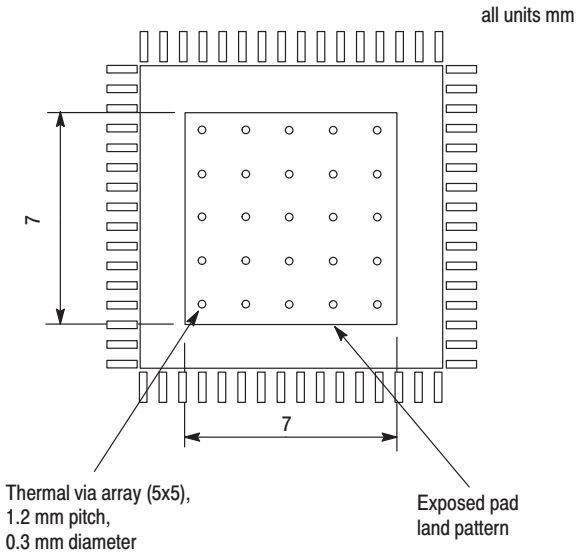



**Figure 3. Recommended thermal land pattern**

The via diameter is should be approx. 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via resulting in voids during the solder process must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for exposed pad package is equivalent to standard surface mount packages. Figure 4 “Recommended solder mask openings” shows a recommend solder mask opening with respect to the recommended 5 x 5 thermal via array. Because a large solder mask opening may result in a poor release, the opening should be subdivided as shown in Figure 4 For the nominal package standoff 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

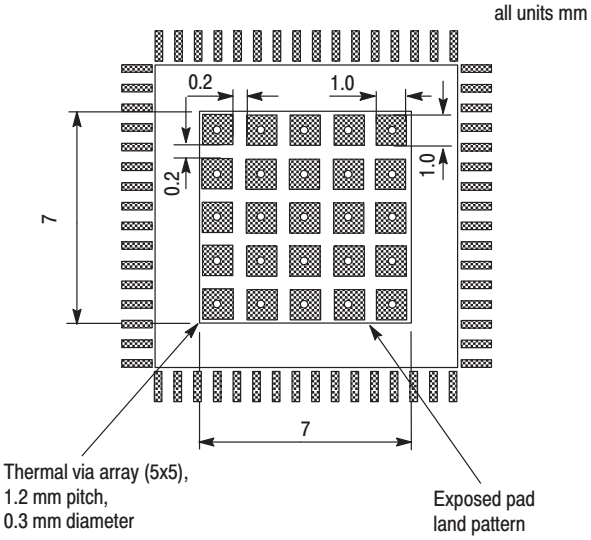



**Figure 4. Recommended solder mask openings**

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided. For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

**Table 7: Thermal Resistance[a]**

| Convection-LFPM | $R_{THJA}$[b] °C/W | $R_{THJA}$[c] °C/W | $R_{THJC}$[d] °C/W | $R_{THJB}$[e] °C/W |
|---|---|---|---|---|
| Natural | 57.1 | 24.9 | 15.8 | 9.7 |
| 100 | 50.0 | 21.3 | | |
| 200 | 46.9 | 20.0 | | |
| 400 | 43.4 | 18.7 | | |
| 800 | 38.6 | 16.9 | | |

a. Thermal data pattern with a 3 x 3 thermal via array on 2S2P boards (based on empirical results)
b. Junction to ambient, single layer test board, per JESD51-6
c. Junction to ambient, four conductor layer test board (2S2P), per JES51-6
d. Junction to case, per MIL-SPEC 883E, method 1012.1
e. Junction to board, four conductor layer test board (2S2P) per JESD 51-8

It is recommended that users employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100EP220 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals. The thermal land should be connected to GND through connection of internal board layers.

**Order this document by MC100EP221/D**

# Low-Voltage 1:20 Differential ECL/PECL Clock Driver

**MC100EP221**

**See Upgrade Product – MC100ES6221**

**LOW–VOLTAGE 1:20 DIFFERENTIAL ECL/PECL CLOCK DRIVER**

**TB SUFFIX**
52–LEAD LQFP PACKAGE
EXPOSED PAD
CASE 1336

The MC100EP221 is a low skew 1–to–20 differential driver, designed with clock distribution in mind. It accepts two clock sources into an input multiplexer. The input signals can be either differential or single–ended if the $V_{BB}$ output is used. The selected signal is fanned out to 20 identical differential outputs.

- 270ps max. Part–to–Part Skew
- 50ps max. Output–to–Output Skew
- Differential Design
- $V_{BB}$ Output
- Voltage and Temperature Compensated Outputs
- Supports 3.3V and 2.5V, ECL and PECL Operation
- Supports HSTL and PECL Clock Systems

The EP221 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate–to–gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent $t_{pd}$ distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

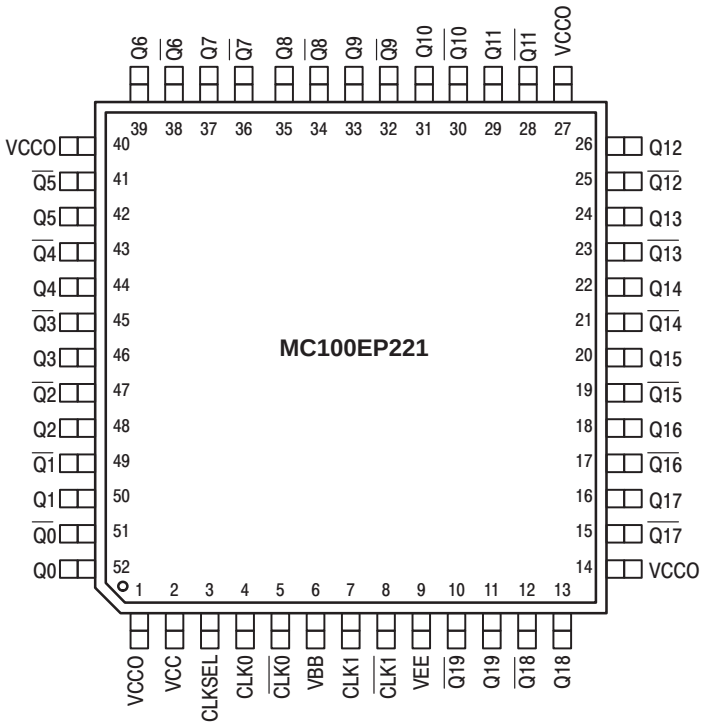
To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all ten differential pairs will be used and therefore terminated. In the case where fewer than ten pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

The MC100EP221, as with most other ECL devices, can be operated from a positive $V_{CC}$ supply in PECL mode. This allows the EP221 to be used for high performance clock distribution in +3.3V or +2.5V systems. Designers can take advantage of the EP221's performance to distribute low skew clocks across the backplane. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies.



**Rev 1**

**Pinout: 52–Lead LQFP**
(Top View)




**FUNCTION**

| CLK_SEL | Active Input |
|---|---|
| 0 | CLK0, $\overline{CLK0}$ |
| 1 | CLK1, $\overline{CLK1}$ |

**LOGIC SYMBOL**

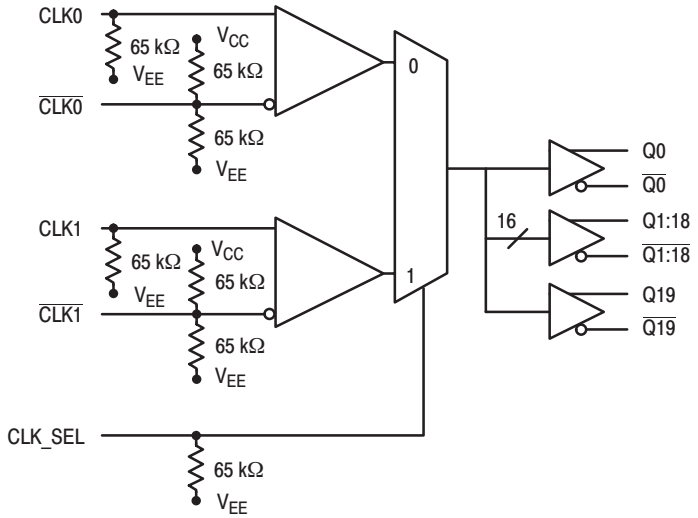


**Table 1: PIN CONFIGURATION**

| Pin | I/O | Type | Function |
|---|---|---|---|
| CLK0, $\overline{CLK0}$ | Input | ECL/LVPECL | Differential reference clock signal input |
| CLK1, $\overline{CLK1}$ | Input | ECL/LVPECL or HSTL | Alternative differential reference clock signal input |
| CLK_SEL | Input | LVPECL | Output frequency divider select |
| Q[0-19], $\overline{Q[0\text{-}19]}$ | Output | LVPECL | Differential clock outputs |
| VEE[a] | Supply | | Negative power supply |
| $V_{CC}$, $V_{CCO}$ | Supply | | Positive power supply. All $V_{CC}$ and $V_{CCO}$ pins must be connected to the positive power supply for correct DC and AC operation |
| VBB | Output | | DC bias output for single ended input operation |

a. In ECL mode (negative power supply mode), VEE is either -3.3V or -2.5V and VCC is connected to GND (0V).
In PECL mode (positive power supply mode), VEE is connected to GND (0V) and VCC is either +3.3V or +2.5V.
In both modes, the input and output levels are referrenced to the most positive supply (VCC).

**Table 2: ABSOLUTE MAXIMUM RATINGS[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 4.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -65 | 125 | °C | |

a. Absolute maximum continuos ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 3: GENERAL SPECIFICATIONS**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output termination voltage | | $V_{CC}$ - 2[a] | | V | |
| MM | ESD Protection (Machine model) | 75 | | | V | |
| HBM | ESD Protection (Human body model) | 1500 | | | V | |
| CDM | ESD Protection (Charged device model) | 500 | | | V | |
| LU | Latch-up immunity | 200 | | | mA | |
| $C_{IN}$ | | | 4.0 | | pF | Inputs |
| $\theta_{JA}$ | Thermal resistance junction to ambient | See application information[b] | | | | |
| $\theta_{JC}$ | Thermal resistance junction to case | See application information | | | | |

a. Output termination voltage $V_{TT}$ = 0V for $V_{CC}$=2.5V operation is supported but the power consumption of the device will increase.
b. Proper thermal management is critical for reliable system operation. This especially true for high-fanout and high drive capability products. Thermal package information and exposed pad land pattern design recommendations are available in the applications section of this datasheet. In addition, the means of calculating die power consumption, the corresponding die temperature and the relationsship to long-term reliability is addressed in the Motorola application note AN1545. Thermal modeling is recommended for the MC100EP221.

**Table 4: PECL and HSTL DC Characteristics** ($V_{CCO}$ = $V_{CC}$ = 2.375V to 3.8V, $V_{EE}$ = GND)

| Symbol | Characteristics | $T_A$ = -40°C | | $T_A$ = 25°C | | $T_A$ = 85°C | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Clock input pair CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$[a] (LVPECL differential signals) | | | | | | | | | |
| $V_{PP}$ | Differential input voltage[b] $V_{CC}$=3.3V<br>$V_{CC}$=2.5V | 0.10<br>0.15 | | 0.10<br>0.15 | | 0.10<br>0.15 | | V<br>V | |
| $V_{CMR}$ | Differential cross point voltage[c] CLK0<br>CLK1 | 1.0<br>0.1 | $V_{CC}$-0.4<br>$V_{CC}$-1.0 | 1.0<br>0.1 | $V_{CC}$-0.4<br>$V_{CC}$-1.0 | 1.0<br>0.1 | $V_{CC}$-0.4<br>$V_{CC}$-1.0 | V<br>V | |
| Clock input pair CLK1, $\overline{CLK1}$[d] (HSTL differential signals) | | | | | | | | | |
| $V_{DIF}$ | Differential input voltage[e] $V_{CC}$=3.3V<br>$V_{CC}$=2.5V | 0.4<br>0.4 | 1.0<br>1.0 | 0.4<br>0.4 | 1.0<br>1.0 | 0.4<br>0.4 | 1.0<br>1.0 | V<br>V | |
| $V_X$ | Differential cross point voltage[f] | 0.68 | 0.9 | 0.68 | 0.9 | 0.68 | 0.9 | V | |
| $V_{IH}$ | Input high voltage | $V_X$+0.2 | $V_X$+0.5 | $V_X$+0.2 | $V_X$+0.5 | $V_X$+0.2 | $V_X$+0.5 | V | |
| $V_{IL}$ | Input low voltage | $V_X$-0.5 | $V_X$-0.2 | $V_X$-0.5 | $V_X$-0.2 | $V_X$-0.5 | $V_X$-0.2 | V | |
| All inputs (LVPECL single ended signals) | | | | | | | | | |
| $V_{IH}$ | Input high voltage | $V_{CC}$-1.165 | $V_{CC}$-0.880 | $V_{CC}$-1.165 | $V_{CC}$-0.880 | $V_{CC}$-1.165 | $V_{CC}$-0.880 | V | |
| $V_{IL}$ | Input low voltage | $V_{CC}$-1.810 | $V_{CC}$-1.480 | $V_{CC}$-1.810 | $V_{CC}$-1.480 | $V_{CC}$-1.810 | $V_{CC}$-1.480 | V | |
| $I_{IH}$ | Input Current | | 150 | | 150 | | 150 | µA | $V_{IN}$ = $V_{CC}$ to $V_{EE}$ |
| LVPECL clock outputs (Q0-19, $\overline{Q0\text{-}19}$) | | | | | | | | | |
| $V_{OH}$ | Output High Voltage | $V_{CC}$-1.20 | $V_{CC}$-0.82 | $V_{CC}$-1.15 | $V_{CC}$-0.82 | $V_{CC}$-1.15 | $V_{CC}$-0.82 | V | $I_{OH}$= -30mA[g] |
| $V_{OL}$ | Output Low Voltage | $V_{CC}$-1.90 | $V_{CC}$-1.40 | $V_{CC}$-1.90 | $V_{CC}$-1.40 | $V_{CC}$-1.9 | $V_{CC}$-1.40 | V | $I_{OL}$= -5mA[g] |
| Supply current and $V_{BB}$ | | | | | | | | | |
| $I_{EE}$ | Max. Supply Current | | 190 | | 190 | | 190 | mA | $V_{EE}$ pin |
| $I_{CC}$ | Max. Supply Current[h] | | 750 | | 750 | | 750 | mA | $V_{CC}$ pins |
| $V_{BB}$ | Output reference voltage[i] $V_{CC}$=3.3V<br>$V_{CC}$=2.5V | $V_{CC}$-1.35<br>$V_{CC}$-1.35 | $V_{CC}$-1.24<br>$V_{CC}$-1.24 | $V_{CC}$-1.35<br>$V_{CC}$-1.35 | $V_{CC}$-1.24<br>$V_{CC}$-1.22 | $V_{CC}$-1.35<br>$V_{CC}$-1.35 | $V_{CC}$-1.24<br>$V_{CC}$-1.22 | V<br>V | |

a. The input pairs CLK0, CLK1 are compatible to differential signaling standards. CLK0 is compatible to LVPECL signals and CLK1 meets both HSTL and LVPECL differential signal specifications. The difference between CLK0 and CLK1 is the differential input threshold voltage ($V_{CMR}$).
b. $V_{PP}$ is the minimum differential input voltage swing required to maintain device functionality.
c. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.
d. Clock inputs driven by differential HSTL compatible signals. Only applicable to CLK1, $\overline{CLK1}$.
e. $V_{DIF}$ (DC) is the minimum differential HSTL input voltage swing required for device functionality. Only applicable to CLK1, $\overline{CLK1}$.
f. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.
g. Equivalent to an output termination of 50Ω to $V_{TT}$.
h. $I_{CC}$ includes current through the output resistors (all outputs terminated 50Ω to $V_{TT}$).
i. $V_{BB}$ output can be used to bias the complementary input when the device is used with single ended clock signals. $V_{BB}$ can sink max. 0.3 mA DC current.

**Table 5: ECL DC Characteristics** ($V_{CC}$ = $V_{CCO}$ = GND, $V_{EE}$ = -3.8V to -2.375V)

| Symbol | Characteristics | $T_A$ = -40°C | | $T_A$ = 25°C | | $T_A$ = 85°C | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Clock input pair CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$[a] for ECL differential signals | | | | | | | | | |
| $V_{PP}$ | Differential input voltage[b] | | | | | | | | |
| | $V_{EE}$=-3.3V | 0.10 | | 0.10 | | 0.10 | | V | |
| | $V_{EE}$=-2.5V | 0.15 | | 0.15 | | 0.15 | | V | |
| $V_{CMR}$ | Differential cross point voltage[c] | | | | | | | | |
| | CLK0 | $V_{EE}$+1.0 | -0.4 | $V_{EE}$+1.0 | -0.4 | $V_{EE}$+1.0 | -0.4 | V | |
| | CLK1 | $V_{EE}$+0.1 | –1.0 | $V_{EE}$+0.1 | –1.0 | $V_{EE}$+0.1 | –1.0 | V | |
| All inputs ECL single ended signals | | | | | | | | | |
| $V_{IH}$ | Input high voltage | -1.165 | -0.880 | -1.165 | -0.880 | -1.165 | -0.880 | V | |
| $V_{IL}$ | Input low voltage | -1.810 | -1.480 | -1.810 | -1.480 | -1.810 | -1.480 | V | |
| $I_{IH}$ | Input Current | | 150 | | 150 | | 150 | µA | $V_{IN}$ = $V_{EE}$ to $V_{CC}$ |
| LVPECL clock outputs (Q0-19, $\overline{Q0\text{-}19}$) | | | | | | | | | |
| $V_{OH}$ | Output High Voltage | -1.20 | -0.82 | -1.20 | -0.82 | -1.20 | -0.82 | V | $I_{OH}$= -30 mA[d] |
| $V_{OL}$ | Output Low Voltage | -1.90 | -1.40 | -1.90 | -1.40 | -1.90 | -1.40 | V | $I_{OL}$= -5 mA[d] |
| Supply current and $V_{BB}$ | | | | | | | | | |
| $I_{EE}$ | Max. Supply Current | | 190 | | 190 | | 190 | mA | $V_{EE}$ pin |
| $I_{CC}$ | Max. Supply Current[e] | | 750 | | 750 | | 750 | mA | $V_{CC}$ Pins |
| $V_{BB}$ | Output reference voltage[f] | | | | | | | | |
| | $V_{EE}$=-3.3V | -1.35 | -1.24 | -1.35 | -1.24 | -1.35 | -1.24 | V | |
| | $V_{EE}$=-2.5V | -1.35 | -1.24 | -1.35 | -1.22 | -1.35 | -1.22 | V | |

a. The input pairs CLK0, CLK1 are compatible to differential signaling standards such as ECL. The difference between CLK0 and CLK1 is the differential input threshold voltage ($V_{CMR}$).
b. $V_{PP}$ is the minimum differential input voltage swing required to maintain device functionality.
c. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.
d. Equivalent to an output termination of 50Ω to $V_{TT}$.
e. $I_{CC}$ includes current through the output resistors (all outputs terminated 50Ω to $V_{TT}$).
f. $V_{BB}$ output can be used to bias the complementary input when the device is used with single ended clock signals. $V_{BB}$ can sink max. 0.3 mA DC current.

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**Table 6: PECL/ECL/HSTL AC Characteristics**[a] ($V_{CC}$ = $V_{CCO}$ = 2.375V to 3.8V, $V_{EE}$ = GND) or ($V_{EE}$ = -3.8V to -2.375V, $V_{CC}$ = $V_{CCO}$ = GND)

| Symbol | Characteristics | $T_A$ = -40°C | | | $T_A$ = 25°C | | | $T_A$ = 85°C | | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| Clock input pair CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$[b] for PECL differential signals | | | | | | | | | | | | |
| $V_{PP}$ | Differential input voltage[c] (peak-to-peak) | 0.5 | | 1.0 | 0.5 | | 1.0 | 0.5 | | 1.0 | V | |
| $V_{CMR}$ | Differential cross point voltage[d] CLK0<br>CLK1 | 1.0<br>0.3 | | $V_{CC}$-0.4<br>$V_{CC}$-1.3 | 1.0<br>0.3 | | $V_{CC}$-0.4<br>$V_{CC}$-1.3 | 1.0<br>0.3 | | $V_{CC}$-0.4<br>$V_{CC}$-1.3 | V<br>V | |
| $f_{CLK}$ | Input Frequency (PECL) | 0 | | 1.0 | | | 1.0 | | | 1.0 | GHz | |
| Clock input pair CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$ for ECL differential signals | | | | | | | | | | | | |
| $V_{PP}$ | Differential input voltage (peak-to-peak) | 0.5 | | 1.0 | 0.5 | | 1.0 | 0.5 | | 1.0 | V | |
| $V_{CMR}$ | Differential cross point voltage CLK0<br>CLK1 | $V_{EE}$+1.0<br>$V_{EE}$+0.3 | | -0.4<br>-1.3 | $V_{EE}$+1.0<br>$V_{EE}$+0.3 | | -0.4<br>–1.3 | $V_{EE}$+1.0<br>$V_{EE}$+0.3 | | -0.4<br>-1.3 | V<br>V | |
| $f_{CLK}$ | Input Frequency (ECL) | 0 | | 1.0 | | | 1.0 | | | 1.0 | GHz | |
| Clock input pair CLK1, $\overline{CLK1}$ for HSTL differential signals | | | | | | | | | | | | |
| $V_{DIF}$ | Differential input voltage[e] (peak-to-peak) CLK1 | 0.4 | | 1.0 | 0.5 | | 1.0 | 0.5 | | 1.0 | V | |
| $V_X$ | Differential cross point voltage[f] CLK1 | 0.68 | | 0.9 | 0.68 | | 0.9 | 0.68 | | 0.9 | V | |
| $f_{CLK}$ | Input Frequency (HSTL) | 0 | | 1.0 | | | 1.0 | | | 1.0 | GHz | |
| PECL/ECL clock outputs (Q0-19, $\overline{Q0-19}$) | | | | | | | | | | | | |
| $t_{PD}$ | Propagation Delay $CLK_0$ to Qx<br>$CLK_1$ to Qx | 350<br>370 | 460<br>500 | 600<br>640 | 390<br>440 | 520<br>570 | 660<br>710 | 480<br>530 | 630<br>680 | 750<br>800 | ps<br>ps | Diff.<br>Diff. |
| $V_{O(P-P)}$ | Differential output voltage (peak-to-peak) $f_O$ < 50 MHz<br>$f_O$ < 0.8 GHz<br>$f_O$ < 1.0 GHz | 450<br>400<br>375 | | | 550<br>500<br>400 | | | 550<br>500<br>400 | | | mV<br>mV<br>mV | |
| $t_{sk(O)}$ | Output-to-output skew (within device) | | 30 | 50 | | 30 | 50 | | 30 | 50 | ps | Diff. |
| $t_{sk(PP)}$ | Output-to-output skew (part-to-part) | | | 270 | | | 270 | | | 270 | ps | Diff. |
| $t_{JIT(CC)}$ | Output cycle-to-cycle jitter (RMS) | | | TBD | | | TBD | | | TBD | ps | |
| $DC_O$ | Output duty cycle | 49.5 | 50 | 50.5 | 49.5 | 50 | 50.5 | 49.5 | 50 | 50.5 | % | $DC_{fref}$= 50% |
| $t_r$, $t_f$ | Output Rise/Fall Time | 100 | | 500 | 100 | | 500 | 100 | | 500 | ps | 20% to 80% |

a. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
b. The input pairs CLK0, CLK1 are compatible to differential signaling standards such as ECL. The difference between CLK0 and CLK1 is the differential input threshold voltage ($V_{CMR}$).
c. $V_{PP}$ (AC) is the minimum differential input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
d. $V_{CMR}$ (AC) is the crosspoint of the differential input signal. AC operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ (AC) or $V_{PP}$ (AC) impacts the device propagation delay and part-to-part skew.
e. $V_{DIF}$ (AC) is the minimum differential HSTL input voltage swing required to maintain AC characteristics. Only applicable to CLK1.
f. $V_X$ (AC) is the crosspoint of the differential HSTL input signal. AC operation is obtained when the crosspoint is within the $V_X$ (AC) range and the input swing lies within the $V_{DIF}$ (AC) specification. Violation of $V_X$ (AC) or $V_{DIF}$ (AC) impacts the device propagation delay and part-to-part skew.

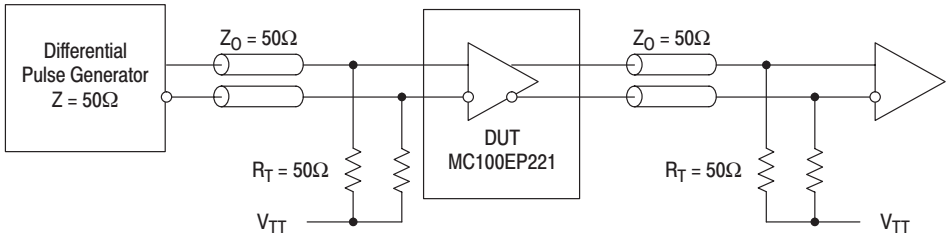


**Figure 1. MC100EP221 AC test reference**

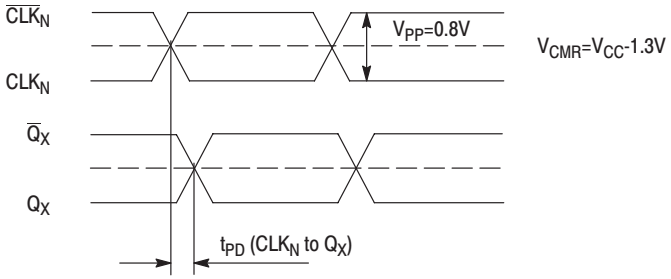


**Figure 2. MC100EP221 AC reference measurement waveform**

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## APPLICATIONS INFORMATION

### Using the thermally enhanced package of the MC100EP221

The MC100EP221 uses a thermally enhanced exposed pad (EP) 52 lead LQFP package. The package is molded so that the leadframe is exposed at the surface of the package bottom side. The exposed metal pad will provide the low thermal impedance that supports the power consumption of the MC100EP221 high-speed bipolar integrated circuit and eases the power management task for the system design. A thermal land pattern on the printed circuit board and thermal vias are recommended in order to take advantage of the enhanced thermal capabilities of the MC100EP221. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal path. In multilayer board designs, thermal vias thermally connect the exposed pad to internal copper planes. Number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package. A nine thermal via array, arranged in a 3 x 3 array and using a 1.2 mm pitch in the center of the thermal land is the absolute minimum requirement for MC100EP221 applications on multi-layer boards. The recommended thermal land design comprises a 5 x 5 thermal via array as shown in Figure 3 “Recommended thermal land pattern”, providing an efficient heat removal path.

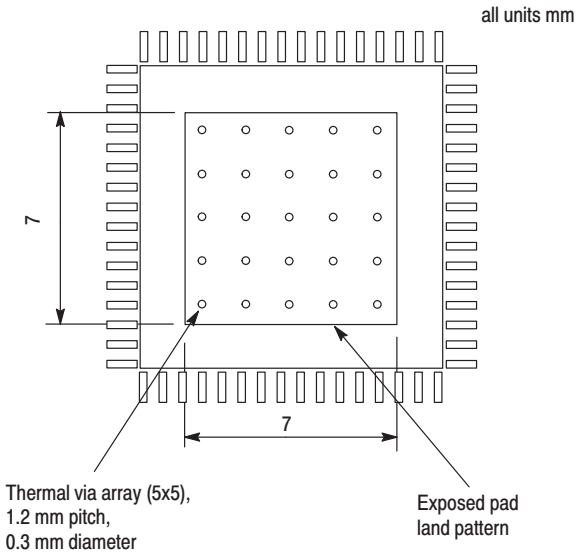


**Figure 3. Recommended thermal land pattern**

The via diameter is should be approx. 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via resulting in voids during the solder process must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for exposed pad package is equivalent to standard surface mount packages. Figure 4 “Recommended solder mask openings” shows a recommend solder mask opening with respect to the recommended 5 x 5 thermal via array. Because a large solder mask opening may result in a poor release, the opening should be subdivided as shown in Figure 4 For the nominal package standoff 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

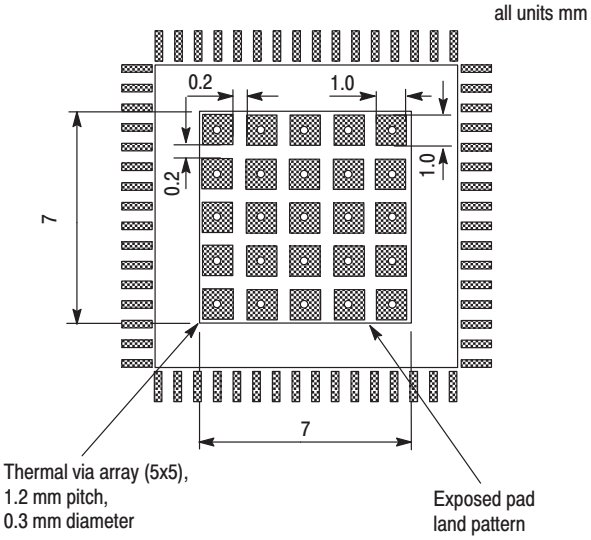


**Figure 4. Recommended solder mask openings**

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided. For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

**Table 7: Thermal Resistance[a]**

| Convection-LFPM | $R_{THJA}$[b] °C/W | $R_{THJA}$[c] °C/W | $R_{THJC}$[d] °C/W | $R_{THJB}$[e] °C/W |
|---|---|---|---|---|
| Natural | 57.1 | 24.9 | 15.8 | 9.7 |
| 100 | 50.0 | 21.3 | | |
| 200 | 46.9 | 20.0 | | |
| 400 | 43.4 | 18.7 | | |
| 800 | 38.6 | 16.9 | | |

a. Thermal data pattern with a 3 x 3 thermal via array on 2S2P boards (based on empirical results)
b. Junction to ambient, single layer test board, per JESD51-6
c. Junction to ambient, four conductor layer test board (2S2P), per JES51-6
d. Junction to case, per MIL-SPEC 883E, method 1012.1
e. Junction to board, four conductor layer test board (2S2P) per JESD 51-8

It is recommended that users employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100EP221 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals. The thermal land should be connected to GND through connection of internal board layers.

**Order Number: MC100EP222/D**
**Rev. 2, 09/2001**

# Low Voltage ECL/PECL 1:15 Clock Driver

## MC100EP222

**See Upgrade Product – MC100ES6222**

**LOW VOLTAGE 3.3 V/2.5 V 1:15 DIFFERENTIAL ECL/PECL CLOCK DRIVER**

**TB SUFFIX**
52–LEAD LQFP PACKAGE
EXPOSED PAD
CASE 1336

The MC100EP222 is a low voltage, low skew 1:15 differential ÷1 and ÷2 ECL/PECL clock distribution buffer. The MC100EP222 has been designed and optimized for 2.5 V and 3.3 V systems. Target applications for this clock driver are high performance clock distribution systems for computer, networking and telecommunication systems.

**Features:**

- 15 differential ECL outputs (4 output banks)
- 2 selectable differential ECL inputs
- Selectable 1:1 or 1:2 frequency outputs
- Operates from a -2.5, -3.3 V (ECL) or 2.5, 3.3 V (PECL) power supply
- Extended temperature operating range of -40 to +85 deg C

The MC100EP222 device characteristics allows low-skew clock distribution of differential and single-ended LVECL/LVPECL signals. Typical applications for the MC100EP222 are primary clock distribution systems on backplanes of high-performance computer, networking and telecommunication systems.

The MC100EP222 can be operated from a 3.3 V or 2.5 V positive supply (PECL mode) without the requirement of a negative supply line. Each of the four output banks of two, three, four and six differential clock output pairs may be independently configured to distribute the input frequency or ÷2 of the input frequency. The FSELA, FSELB, FSELC, FSELD and CLK_SEL are asychronous control inputs. Any changes of the control inputs require a MR pulse for resynchronization of the the ÷2 outputs. For the functionality of the MR control input, “Timing Diagram” on page 566.

Each of the CLK0, CLK1 inputs can be used differential of single-ended. For single-ended signals, connect the bypassed $V_{BB}$ output reference to the unused input of the pair.

The MC100EP222 guarantees low output-to-output skew of 40 (70) ps and device-to-device skew of max. 350 ps. To ensure low skew clock signals in the application, both sides of any differential output pair need to be terminated identically, even if only one side is used. When fewer than all fifteen pairs are used, identical termination of all output pairs on the same package side is recommended. If no outputs on a side are used, it is recommended to leave all of these outputs open and unterminated. This will maintain minimum output skew.



**Rev 2**

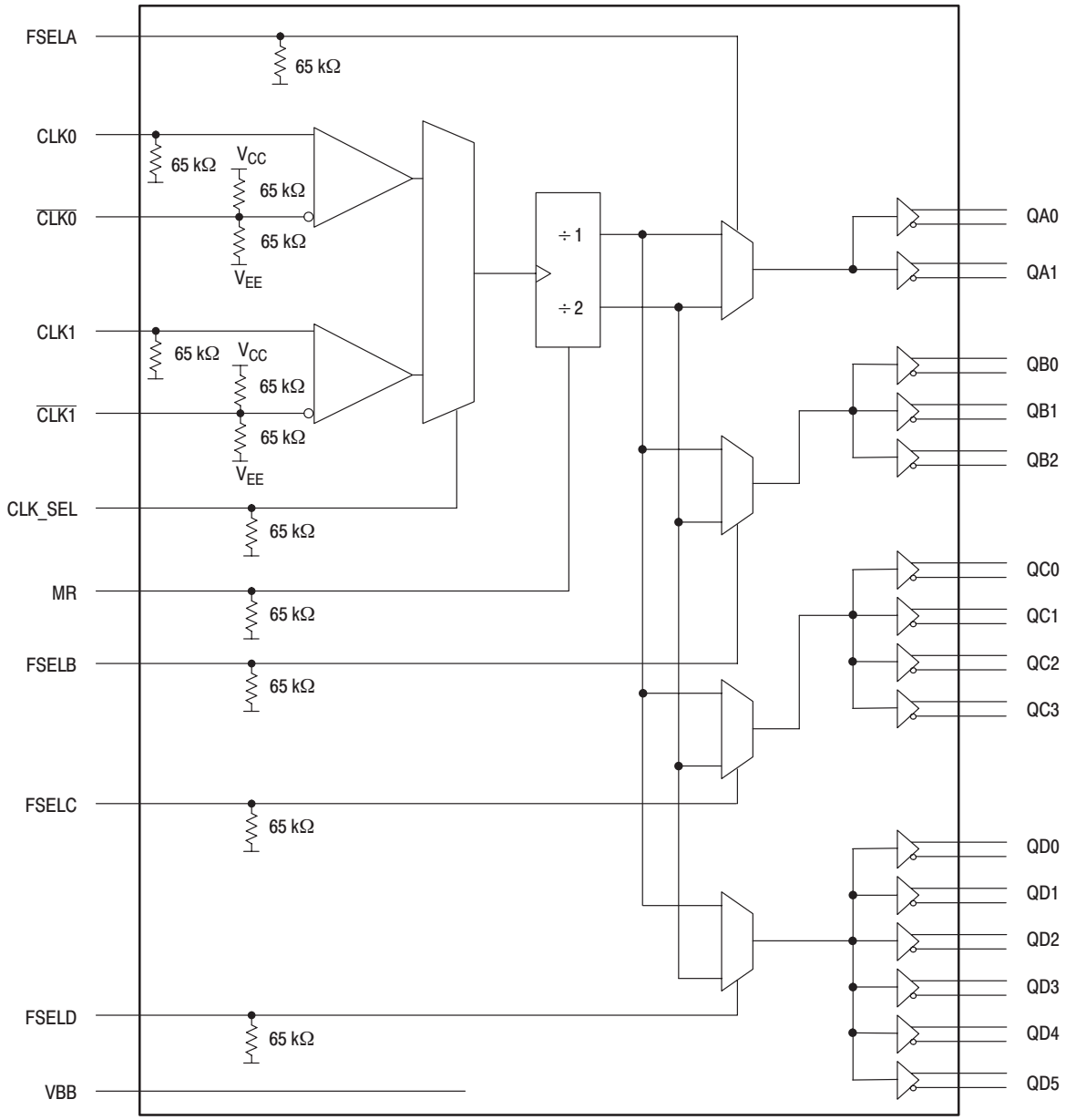


**Figure 1. MC100EP222 Logic Diagram**

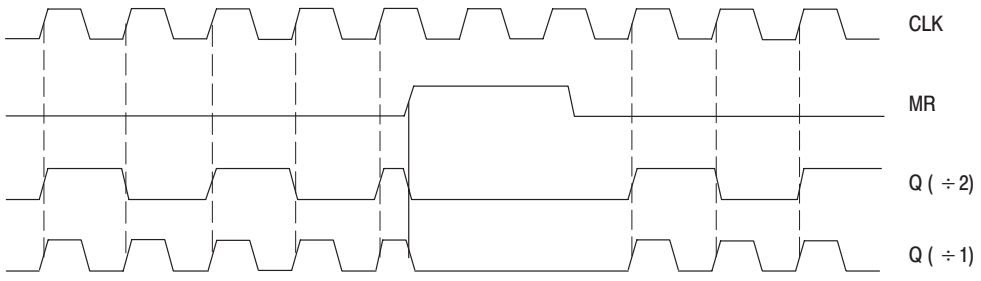


**Figure 2. MC100EP222 Function Diagram**

**Figure 3. 52 Lead Package Pinout** (Top View)

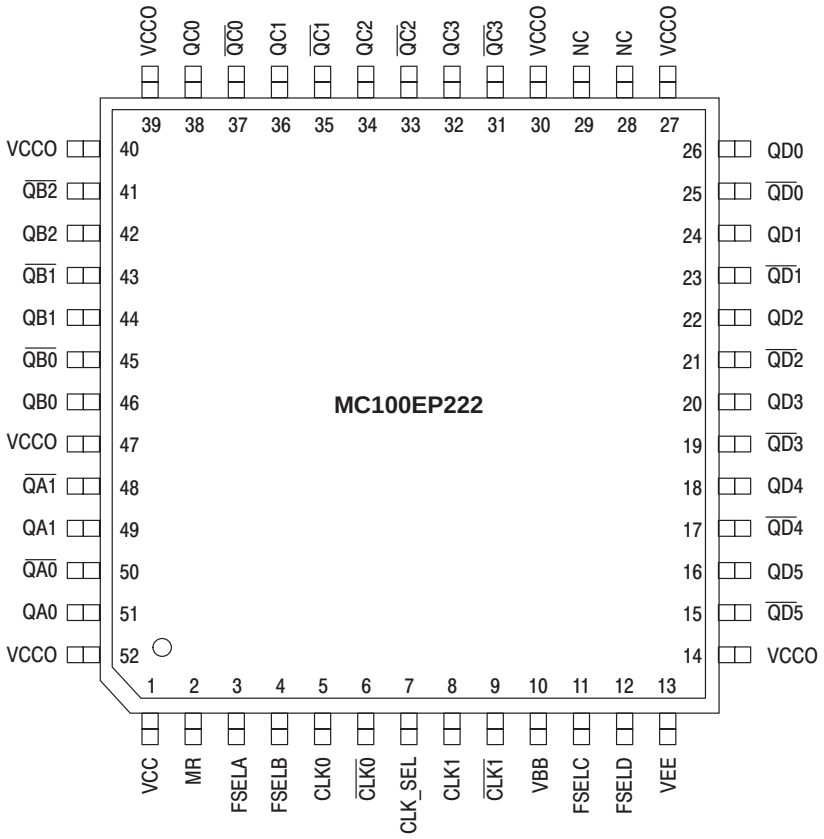


**Table 1: FUNCTION TABLE**

| Control Pin | 0 | 1 |
|---|---|---|
| FSELA (asynchronous) | ÷1 | ÷2 |
| FSELB (asynchronous) | ÷1 | ÷2 |
| FSELC (asynchronous) | ÷1 | ÷2 |
| FSELD (asynchronous) | ÷1 | ÷2 |
| CLK_SEL (asynchronous) | CLK0 | CLK1 |
| MR (asynchronous) | Active | Reset |

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**Table 2: PIN CONFIGURATION**

| Pin | I/O | Type | Description |
|---|---|---|---|
| CLK0, $\overline{CLK0}$ | Input | ECL/PECL | Differential reference clock signal input |
| CLK1, $\overline{CLK1}$ | Input | ECL/PECL | Alternative differential reference clock signal input |
| CLK_SEL | Input | ECL/PECL | Clock input select |
| QAn, $\overline{QAn}$ | Output | ECL/PECL | Bank A differential outputs |
| QBn, $\overline{QBn}$ | Output | ECL/PECL | Bank B differential outputs |
| QCn, $\overline{QCn}$ | Output | ECL/PECL | Bank C differential outputs |
| QDn, $\overline{QDn}$ | Output | ECL/PECL | Bank D differential outputs |
| FSELA | Input | ECL/PECL | Selection of bank A output frequency |
| FSELB | Input | ECL/PECL | Selection of bank B output frequency |
| FSELC | Input | ECL/PECL | Selection of bank C output frequency |
| FSELD | Input | ECL/PECL | Selection of bank D output frequency |
| MR | Input | ECL/PECL | Reset |
| VBB | Output | | DC bias output for single ended input operation |
| VEE[a] | Supply | | Negative power supply |
| $V_{CC}$, $V_{CCO}$ | Supply | | Positive power supply. All $V_{CC}$ and $V_{CCO}$ pins must be connected to the positive power supply for correct DC and AC operation |

a. In ECL mode (negative power supply mode), VEE is either -3.3V or -2.5V and VCC is connected to GND (0V).
In PECL mode (positive power supply mode), VEE is connected to GND (0V) and VCC is either +3.3V or +2.5V .
In both modes, the input and output levels are referrenced to the most positive supply.

**Table 3: ABSOLUTE MAXIMUM RATINGS[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 4.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -65 | 125 | °C | |

a. Absolute maximum continuos ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 4: GENERAL SPECIFICATIONS**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output termination voltage | | $V_{CC}$ - 2[a] | | V | |
| MM | ESD Protection (Machine model) | 75 | | | V | |
| HBM | ESD Protection (Human body model) | 1500 | | | V | |
| CDM | ESD Protection (Charged device model | 500 | | | V | |
| LU | Latch-up immunity | 200 | | | mA | |
| $C_{IN}$ | | | 4.0 | | pF | Inputs |
| $\theta_{JA}$ | Thermal resistance junction to ambient | See application information[b] | | | | |
| $\theta_{JC}$ | Thermal resistance junction to case | See application information | | | | |

a. Output termination voltage $V_{TT}$ = 0V for $V_{CC}$=2.5V operation is supported but the power consumption of the device will increase
b. Proper thermal management is critical for reliable system operation. This especially true for high-fanout and high drive capability products. Thermal package information and exposed pad land pattern design recommendations are available in the applications section of this datasheet. In addition, the means of calculating die power consumption, the corresponding die temperature and the relationsship to long-term reliability is addressed in the Motorola application note AN1545. Thermal modeling is recommended for the MC100EP222.

**Table 5: PECL DC Characteristics** ($V_{CCO}$ = $V_{CC}$ = 2.375 V to 3.8 V, $V_{EE}$ = GND)

| Symbol | Characteristics | $T_A$ = -40°C | | $T_A$ = 25°C | | $T_A$ = 85°C | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Clock input pairs CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$ (LVPECL differential signals) | | | | | | | | | |
| $V_{PP}$ | Differential input voltage[a] $V_{CC}$=3.3 V<br>$V_{CC}$=2.5 V | 0.10<br>0.15 | | 0.10<br>0.15 | | 0.10<br>0.15 | | V<br>V | |
| $V_{CMR}$ | Differential cross point voltage[b] CLK0,CLK1 | 1.0 | $V_{CC}$-0.4 | 1.0 | $V_{CC}$-0.4 | 1.0 | $V_{CC}$-0.4 | V | |
| $I_{IH}$ | Input Current | | 150 | | 150 | | 150 | µA | $V_{IN}$ = $V_{CC}$ to $V_{EE}$ |
| Control inputs (LVPECL single ended) | | | | | | | | | |
| $V_{IH}$ | Input high voltage | $V_{CC}$-1.165 | $V_{CC}$-0.880 | $V_{CC}$-1.165 | $V_{CC}$-0.880 | $V_{CC}$-1.165 | $V_{CC}$-0.880 | V | |
| $V_{IL}$ | Input low voltage | $V_{CC}$-1.810 | $V_{CC}$-1.480 | $V_{CC}$-1.810 | $V_{CC}$-1.480 | $V_{CC}$-1.810 | $V_{CC}$-1.480 | V | |
| $I_{IH}$ | Input Current | | 150 | | 150 | | 150 | µA | $V_{IN}$ = $V_{CC}$ to $V_{EE}$ |
| LVPECL clock outputs (QAn, $\overline{QAn}$, QBn, $\overline{QBn}$, QCn, $\overline{QCn}$, QDn, $\overline{QDn}$) | | | | | | | | | |
| $V_{OH}$ | Output High Voltage | $V_{CC}$-1.20 | $V_{CC}$-0.82 | $V_{CC}$-1.15 | $V_{CC}$-0.82 | $V_{CC}$-1.15 | $V_{CC}$-0.82 | V | $I_{OH}$= -30mA[c] |
| $V_{OL}$ | Output Low Voltage | $V_{CC}$-1.90 | $V_{CC}$-1.40 | $V_{CC}$-1.90 | $V_{CC}$-1.40 | $V_{CC}$-1.9 | $V_{CC}$-1.40 | V | $I_{OL}$= -5mA[c] |
| Supply current and $V_{BB}$ | | | | | | | | | |
| $I_{EE}$ | Max. Supply Current | | 190 | | 190 | | 190 | mA | $V_{EE}$ pin |
| $I_{CC}$ | Max. Supply Current[d] | | 675 | | 675 | | 675 | mA | $V_{CC}$ pins |
| $V_{BB}$ | Output reference voltage[e] $V_{CC}$=3.3 V<br>$V_{CC}$=2.5 V | $V_{CC}$-1.35<br>$V_{CC}$-1.35 | $V_{CC}$-1.24<br>$V_{CC}$-1.24 | $V_{CC}$-1.35<br>$V_{CC}$-1.35 | $V_{CC}$-1.24<br>$V_{CC}$-1.22 | $V_{CC}$-1.35<br>$V_{CC}$-1.35 | $V_{CC}$-1.24<br>$V_{CC}$-1.22 | V<br>V | |

a. $V_{PP}$ is the minimum differential input voltage swing required to maintain device functionality.
b. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.
c. Equivalent to an output termination of 50Ω to $V_{TT}$.
d. $I_{CC}$ includes current through the output resistors (all outputs terminated 50Ω to $V_{TT}$).
e. $V_{BB}$ output can be used to bias the complementary input when the device is used with single ended clock signals. $V_{BB}$ can sink max. 0.3 mA DC current.

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**Table 6: ECL DC Characteristics** ($V_{CC}$ = $V_{CCO}$ = GND, $V_{EE}$ = -3.8 V to -2.375 V)

| Symbol | Characteristics | $T_A$ = -40°C | | $T_A$ = 25°C | | $T_A$ = 85°C | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Clock input pairs CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$ (ECL differential signals) | | | | | | | | | |
| $V_{PP}$ | Differential input voltage[a] $V_{EE}$=-3.3 V<br>$V_{EE}$=-2.5 V | 0.10<br>0.15 | | 0.10<br>0.15 | | 0.10<br>0.15 | | V<br>V | |
| $V_{CMR}$ | Differential cross point voltage[b] CLK0,CLK1 | $V_{EE}$+1.0 | -0.4 | $V_{EE}$+1.0 | -0.4 | $V_{EE}$+1.0 | -0.4 | V | |
| $I_{IH}$ | Input Current | | 150 | | 150 | | 150 | µA | $V_{IN}$ = $V_{EE}$ to $V_{CC}$ |
| All inputs ECL single ended signals | | | | | | | | | |
| $V_{IH}$ | Input high voltage | -1.165 | -0.880 | -1.165 | -0.880 | -1.165 | -0.880 | V | |
| $V_{IL}$ | Input low voltage | -1.810 | -1.480 | -1.810 | -1.480 | -1.810 | -1.480 | V | |
| $I_{IH}$ | Input Current | | 150 | | 150 | | 150 | µA | $V_{IN}$ = $V_{EE}$ to $V_{CC}$ |
| LVPECL clock outputs (Q0-19, $\overline{Q0\text{-}19}$) | | | | | | | | | |
| $V_{OH}$ | Output High Voltage | -1.20 | -0.82 | -1.20 | -0.82 | -1.20 | -0.82 | V | $I_{OH}$= -30 mA[c] |
| $V_{OL}$ | Output Low Voltage | -1.90 | -1.40 | -1.90 | -1.40 | -1.90 | -1.40 | V | $I_{OL}$= -5 mA[c] |
| Supply current and $V_{BB}$ | | | | | | | | | |
| $I_{EE}$ | Max. Supply Current | | 190 | | 190 | | 190 | mA | $V_{EE}$ pin |
| $I_{CC}$ | Max. Supply Current[d] | | 750 | | 750 | | 750 | mA | $V_{CC}$ Pins |
| $V_{BB}$ | Output reference voltage[e] $V_{EE}$=-3.3 V<br>$V_{EE}$=-2.5 V | -1.35<br>-1.35 | -1.24<br>-1.24 | -1.35<br>-1.35 | -1.24<br>-1.22 | -1.35<br>-1.35 | -1.24<br>-1.22 | V<br>V | |

a. $V_{PP}$ is the minimum differential input voltage swing required to maintain device functionality.
b. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.
c. Equivalent to an output termination of 50Ω to $V_{TT}$.
d. $I_{CC}$ includes current through the output resistors (all outputs terminated 50Ω to $V_{TT}$).
e. $V_{BB}$ output can be used to bias the complementary input when the device is used with single ended clock signals. $V_{BB}$ can sink max. 0.3 mA DC current.

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**Table 7: ECL AC Characteristics**[a] ($V_{CC}$ = $V_{CCO}$ = 2.375 V to 3.8 V, $V_{EE}$ = GND) or ($V_{EE}$ = -3.8 V to -2.375 V, $V_{CC}$ = $V_{CCO}$ = GND)

| Symbol | Characteristics | $T_A$ = -40°C | | | $T_A$ = 25°C | | | $T_A$ = 85°C | | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| Clock input pair CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$ (PECL/ECL differential signals) | | | | | | | | | | | | |
| $V_{PP}$ | Differential input voltage[b] (peak-to-peak) CLK0, CLK1 | 0.5 | | 1.0 | 0.5 | | 1.0 | 0.5 | | 1.0 | V | |
| $V_{CMR}$ | Differential cross point voltage[c] | | | | | | | | | | | |
| | PECL mode CLK0, CLK1 | $V_{EE}$+1.0 | | -0.4 | $V_{EE}$+1.0 | | -0.4 | $V_{EE}$+1.0 | | -0.4 | V | |
| | ECL mode CLK0, CLK1 | 1.0 | | $V_{CC}$-0.4 | 1.0 | | $V_{CC}$-0.4 | 1.0 | | $V_{CC}$-0.4 | V | |
| $f_{CLK}$ | Input Frequency | 0 | | 1.0 | 0 | | 1.0 | 0 | | 1.0 | GHz | |
| PECL/ECL clock outputs (QAn, $\overline{QAn}$, QBn, $\overline{QBn}$, QCn, $\overline{QCn}$, QDn, $\overline{QDn}$) | | | | | | | | | | | | |
| $t_{PD}$ | Propagation Delay $CLK_N$ to Qx | 560 | 730 | 910 | 640 | 790 | 940 | 740 | 890 | 1040 | ps | Diff. |
| | MR to Qx | | | TBD | | | TBD | | | TBD | ps | |
| $V_{O(P-P)}$ | Differential output voltage | | | | | | | | | | | |
| | (peak-to-peak) $f_O$ < 100 MHz | 450 | | | 550 | | | 550 | | | mV | |
| | $f_O$ < 0.5 GHz | 400 | | | 500 | | | 500 | | | mV | |
| | $f_O$ < 1.0 GHz | 375 | | | 400 | | | 400 | | | mV | |
| $t_{sk(O)}$ | Output-to-output skew within | | | | | | | | | | | Diff. |
| | - QA[0:1] | | | 40 | | | 40 | | | 40 | ps | |
| | - QB[0:2] | | | 40 | | | 40 | | | 40 | ps | |
| | - QC[0:3] | | | 70 | | | 70 | | | 70 | ps | |
| | - QD[0:5] | | | 40 | | | 40 | | | 40 | ps | |
| | | | | | | | | | | | ps | |
| | - $QA_N$, $QB_N$, $QD_N$ (single freq.) | | | 60 | | | 60 | | | 60 | ps | |
| | - all outputs (single freq.) | | | 120 | | | 120 | | | 120 | ps | |
| | - $QA_N$, $QB_N$, $QD_N$ (multiple freq.) | | | 130 | | | 130 | | | 130 | ps | |
| | - all outputs (multiple freq.) | | | 150 | | | 150 | | | 150 | ps | |
| $t_{sk(PP)}$ | Output-to-output skew (part-to-part) | | | 350 | | | 300 | | | 300 | ps | Diff. |
| $t_{JIT(CC)}$ | Output cycle-to-cycle jitter (RMS) | | | TBD | | | TBD | | | TBD | ps | |
| $DC_O$ | Output duty cycle | 49.5 | 50 | 50.5 | 49.5 | 50 | 50.5 | 49.5 | 50 | 50.5 | % | $DC_{fref}$= 50% |
| $t_r$, $t_f$ | Output Rise/Fall Time | 100 | | 500 | 100 | | 500 | 100 | | 500 | ps | 20% to 80% |

a. AC characteristics apply for parallel output termination of 50 Ω to $V_{TT}$.
b. $V_{PP}$ is the minimum differential input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
c. $V_{CMR}$ (AC) is the crosspoint of the differential input signal. AC operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ (AC) or $V_{PP}$ (AC) impacts the device propagation delay and part-to-part skew.

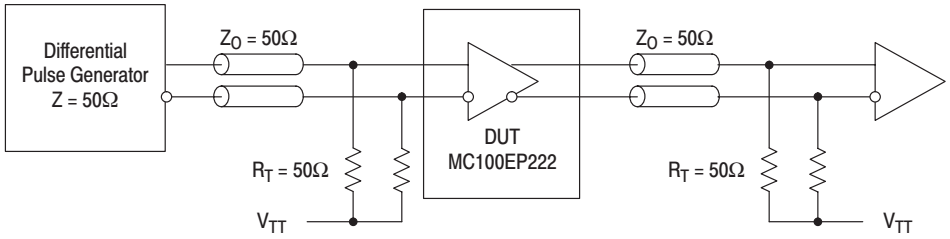


**Figure 4. MC100EP222 AC test reference**

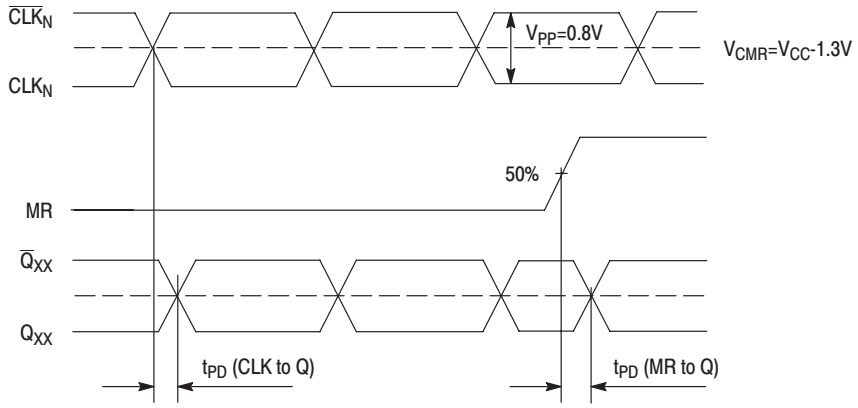


**Figure 5. MC100EP222 $t_{PD}$ / AC reference measurement waveform**

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## APPLICATIONS INFORMATION

### Using the thermally enhanced package of the MC100EP222

The MC100EP222 uses a thermally enhanced exposed pad (EP) 52 lead LQFP package. The package is molded so that the leadframe is exposed at the surface of the package bottom side. The exposed metal pad will provide the low thermal impedance that supports the power consumption of the MC100EP222 high-speed bipolar integrated circuit and eases the power management task for the system design. A thermal land pattern on the printed circuit board and thermal vias are recommended in order to take advantage of the enhanced thermal capabilities of the MC100EP222. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal path. In multilayer board designs, thermal vias thermally connect the exposed pad to internal copper planes. Number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package. A nine thermal via array, arranged in a 3 x 3 array and using a 1.2 mm pitch in the center of the thermal land is the absolute minimum requirement for MC100EP222 applications on multi-layer boards. The recommended thermal land design comprises a 5 x 5 thermal via array as shown in Figure 6 “Recommended thermal land pattern”, providing an efficient heat removal path.

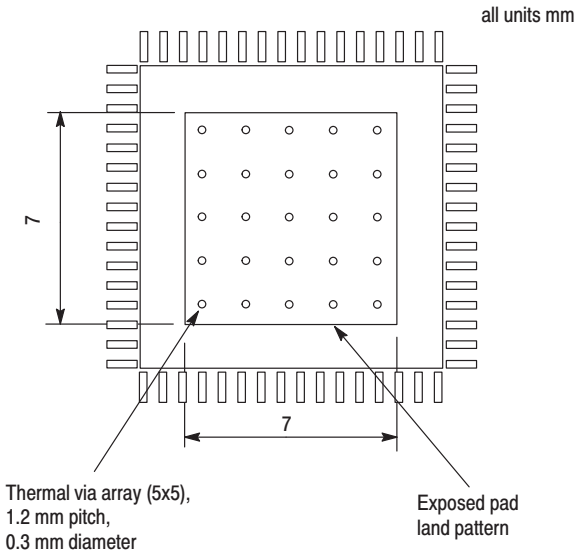



**Figure 6. Recommended thermal land pattern**

The via diameter is should be approx. 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via resulting in voids during the solder process must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for exposed pad package is equivalent to standard surface mount packages. Figure 7 “Recommended solder mask openings” shows a recommend solder mask opening with respect to the recommended 5 x 5 thermal via array. Because a large solder mask opening may result in a poor release, the opening should be subdivided as shown in Figure 7 For the nominal package standoff 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

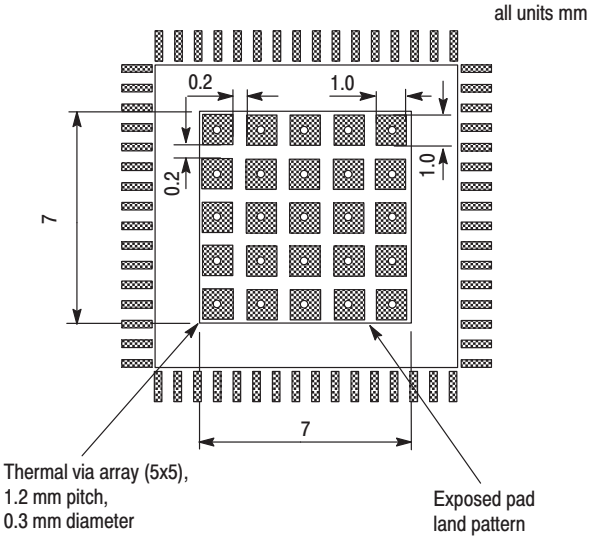



**Figure 7. Recommended solder mask openings**

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided. For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

**Table 8: Thermal Resistance[a]**

| Convection-LFPM | $R_{THJA}$[b] °C/W | $R_{THJA}$[c] °C/W | $R_{THJC}$[d] °C/W | $R_{THJB}$[e] °C/W |
|---|---|---|---|---|
| Natural | 57.1 | 24.9 | 15.8 | 9.7 |
| 100 | 50.0 | 21.3 | | |
| 200 | 46.9 | 20.0 | | |
| 400 | 43.4 | 18.7 | | |
| 800 | 38.6 | 16.9 | | |

a. Thermal data pattern with a 3 x 3 thermal via array on 2S2P boards (based on empirical results)
b. Junction to ambient, single layer test board, per JESD51-6
c. Junction to ambient, four conductor layer test board (2S2P), per JES51-6
d. Junction to case, per MIL-SPEC 883E, method 1012.1
e. Junction to board, four conductor layer test board (2S2P) per JESD 51-8

It is recommended that users employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100EP222 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals. The thermal land should be connected to GND through connection of internal board layers.

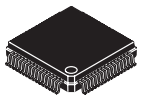
*Product Preview*

# Low-Voltage 1:22 Differential PECL/HSTL Clock Driver

**MC100EP223**

**See Upgrade Product – MC100ES6223**

**LOW–VOLTAGE**
**1:22 DIFFERENTIAL**
**PECL/HSTL CLOCK DRIVER**



**TC SUFFIX**
64–LEAD LQFP PACKAGE
CASE 840K–01

The MC100EP223 is a low skew 1–to–22 differential driver, designed with clock distribution in mind. It accepts two clock sources into an input multiplexer. The selected signal is fanned out to 22 identical differential outputs.

- 200ps Part–to–Part Skew
- 50ps Output–to–Output Skew
- Differential Design
- Open Emitter HSTL Compatible Outputs
- 3.3V $V_{CC}$
- Both PECL and HSTL Inputs
- 75kΩ Input Pulldown Resistors
- Thermally Enhanced 64 lead Exposed Pad LQFP

The EP223 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate–to–gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent $t_{pd}$ distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

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The EP223 HSTL outputs are not realized in the conventional manner. To minimize part–to–part and output–to–output skew, the HSTL compatible output levels are generated with an open emitter architecture. The outputs are pulled down with 50Ω to ground, rather than the typical 50Ω to $V_{DDQ}$ pullup of a “standard” HSTL output. Because the HSTL outputs are pulled to ground, the EP223 does not utilize the $V_{DDQ}$ supply of the HSTL standard. The output levels are derived from $V_{CC}$.

In the case of an asynchronous control, there is a chance of generating a ‘runt’ clock pulse when the device is enabled/disabled. To avoid this, the output enable (OE) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all 22 differential pairs will be used and therefore terminated. In the case where fewer than 22 pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.
**Rev 2**

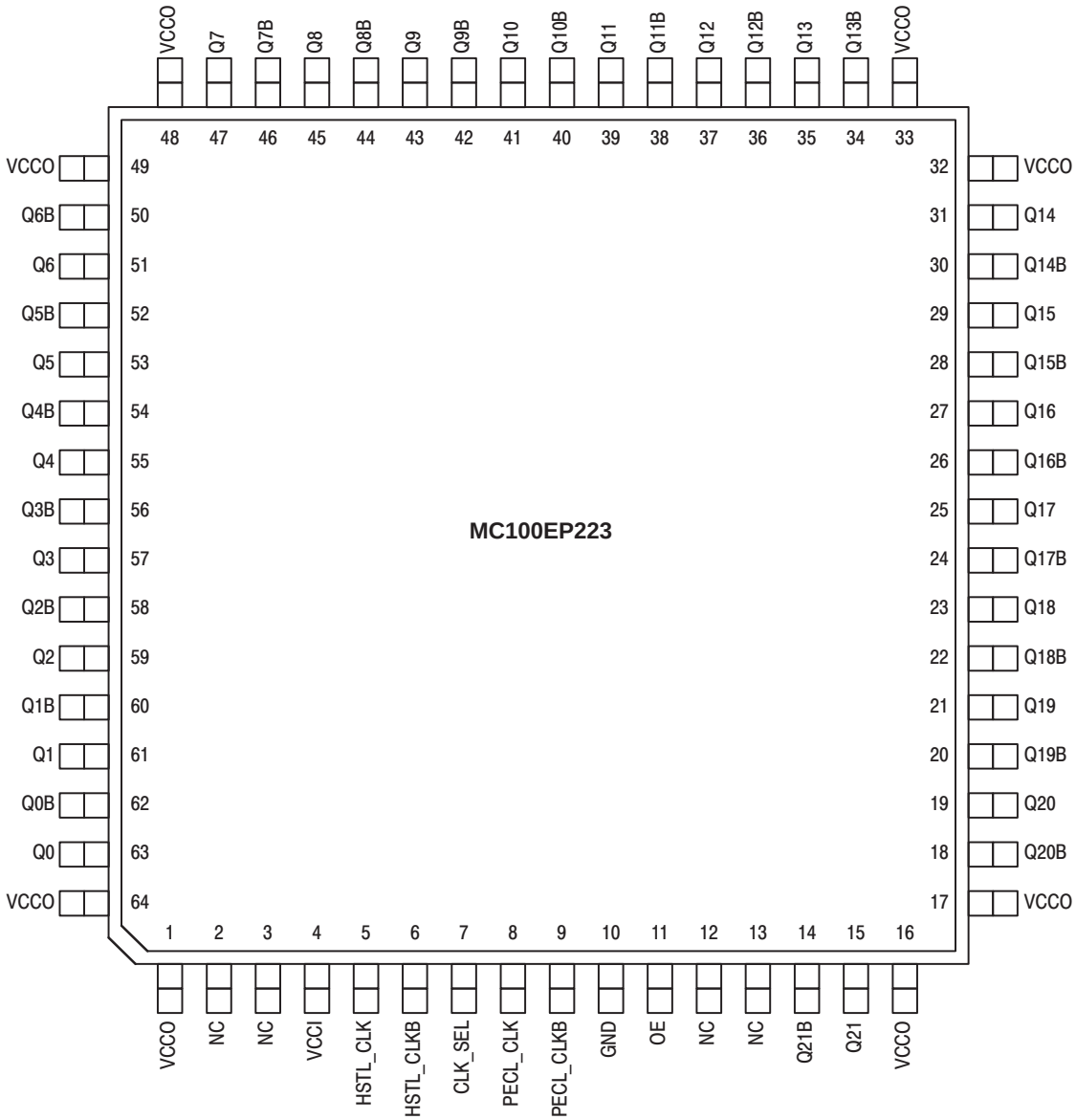


**Figure 1. 64–Lead Pinout** (Top View)



**PIN NAMES**

| Pins | Function |
|---|---|
| HSTL_CLK, HSTL_CLKB | Differential HSTL Inputs |
| PECL_CLK, PECL_CLKB | Differential PECL Inputs |
| Q0:21, Q0B:21B | Differential HSTL Outputs |
| CLK_SEL | Active Clock Select Input |
| OE | Output Enable |
| GND | Ground |
| VCCI | Core VCC |
| VCCO | I/O VCC |

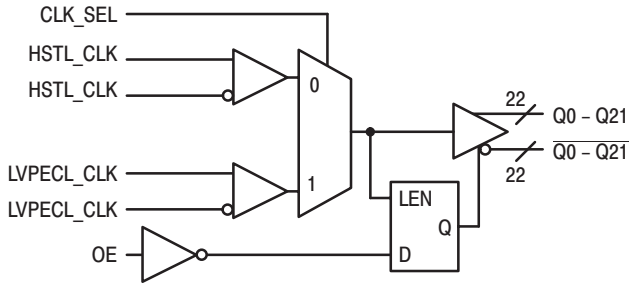


**Figure 2. Logic Symbol**

**FUNCTION**

| OE | CLK_SEL | Q0:21, Q0B:21B |
|---|---|---|
| 0 | 0 | Q = Low, QB = High |
| 0 | 1 | Q = Low, QB = High |
| 1 | 0 | HSTL_CLK, HSTL_CLKB |
| 1 | 1 | PECL_CLK, PECL_CLKB |

**SIGNAL GROUPS**

| Level | Direction | Signal |
|---|---|---|
| HSTL | Input | HSTL_CLK, HSTL_CLKB |
| HSTL | Output | Q0:21, Q0B:21B |
| LVPECL | Input | PECL_CLK, PECL_CLKB |
| LVCMOS/LVTTL | Input | CLK_SEL, OE |

### HSTL DC CHARACTERISTICS

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_{OH}$ | Output HIGH Voltage | | | | 1.0 | | | | | | V |
| $V_{OL}$ | Output LOW Voltage | | | | | | 0.4 | | | | V |
| $V_{IH}$ | Input HIGH Voltage | | | | $V_{\mathfrak{X}}$+0.1 | | 1.6 | | | | V |
| $V_{IL}$ | Input LOW Voltage | | | | –0.3 | | $V_{\mathfrak{X}}$–0.1 | | | | V |
| $V_{\mathfrak{X}}$ | Input Crossover Voltage | | | | 0.68 | | 0.9 | | | | V |

### PECL DC CHARACTERISTICS

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_{IH}$ | Input HIGH Voltage (Note 1.) | 2.135 | | 2.420 | 2.135 | | 2.420 | 2.135 | | 2.420 | V |
| $V_{IL}$ | Input LOW Voltage (Note 1.) | 1.490 | | 1.825 | 1.490 | | 1.825 | 1.490 | | 1.825 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |

1. These values are for $V_{CC}$ = 3.3V. Level specifications vary 1:1 with $V_{CC}$.

### AC CHARACTERISTICS ($V_{EE}$ = GND, $V_{CC}$ =$V_{CC(min)}$ to $V_{CC(max)}$)

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay to Output IN (Differential) | | 1.0 | | | 1.0 | | | 1.0 | | ns |
| $t_{skew}$ | Within–Device Skew<br>Part–to–Part Skew (Diff) | | | 50<br>200 | | | 50<br>200 | | | 50<br>200 | ps |
| $f_{max}$ | Maximum Input Frequency | | | 250 | | | 250 | | | 250 | MHz |
| $V_{PP}$ | Minimum Input Swing PECL_CLK | | 600 | | | 600 | | | 600 | | mV |
| $V_{CMR}$ | Common Mode Range PECL_CLK | | | | | | | | | | V |
| $t_r$, $t_f$ | Output Rise/Fall Time (20–80%) | 300 | | 600 | 300 | | 600 | 300 | | 600 | ps |

### Power Supply Characteristics

| Symbol | Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCI}$ | Core $V_{CC}$ | 3.0 | 3.3 | 3.6 | V |
| $V_{CCO}$ | I/O $V_{CC}$ | 1.6 | 1.8 | 2.0 | V |
| | | | | | |
| $I_{CC}$ | Power Supply Current | | | | mA |
| $I_{EE}$ | Power Supply Current | | | | mA |

## APPLICATIONS INFORMATION

### Using the thermally enhanced package of the MC100EP223

The MC100EP223 uses a thermally enhanced 64 lead LQFP package. This package provides the low thermal impedance that supports the power consumption of the MC100EP223 high-speed bipolar integrated circuit and eases the power management task for the system design. An exposed pad at the bottom of the package establishes thermal conductivity from the package to the printed circuit board. In order to take advantage of the enhanced thermal capabilitites of this package, it is recommended to solder the exposed pad of the package to the printed circuit board. The attachment process for exposed pad package is the same as for any standard surface mount package. Vias are recommended from the pad on the board down to an appropriate plane in the board that is capable of distributing the heat. In order to supply enough solder paste to fill those vias and not starve the solder joints, it may be required to stencil print solder paste onto the printed circuit pad. This pad should match the dimensions of the exposed pad. The dimensions of the exposed pad are shown on the package outline in this specification. For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

**Thermal Resistance**

| Convection LFPM | $R_{THJA}$[a] °C/W | $R_{THJA}$[b] °C/W | $R_{THJC}$[c] °C/W | $R_{THJB}$[d] °C/W |
|---|---|---|---|---|
| Natural | 57.1 | 24.9 | 15.8 | 9.7 |
| 100 | 50.0 | 21.3 | | |
| 200 | 46.9 | 20.0 | | |
| 400 | 43.4 | 18.7 | | |
| 800 | 38.6 | 16.9 | | |

a. Junction to ambient, single layer test board, per JESD51-6
b. Junction to ambient, four conductor layer test board (2S2P), per JES51-6
c. Junction to case, per MIL-SPEC 883E, method 1012.1
d. Junction to board, four conductor layer test board (2S2P) per JESD 51-8

It is recommended that users employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100EP223 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals.

**Order Number: MC100ES6111/D**
**Rev 0, 11/2001**

*Preliminary Information*

# Low Voltage 2.5/3.3V Differential ECL/PECL/HSTL Fanout Buffer

**MC100ES6111**

**LOW–VOLTAGE 1:10 DIFFERENTIAL ECL/PECL/HSTL CLOCK FANOUT DRIVER**

**FA SUFFIX**
32–LEAD LQFP PACKAGE
CASE 873A

The Motorola MC100ES6111 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6111 supports various applications that require to distribute precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver is high performance clock distribution in computing, networking and telecommunication systems.

- 1:10 differential clock distribution
- 35 ps maximum device skew[1]
- Fully differential architecture from input to all outputs
- SiGe technology supports near-zero output skew
- Supports DC to 3 GHz operation of clock or data signals
- ECL/PECL compatible differential clock outputs
- ECL/PECL/HSTL compatible differential clock inputs
- Single 3.3V, -3.3V, 2.5V or -2.5V supply
- Standard 32 lead LQFP package
- Industrial temperature range
- Pin and function compatible to the MC100EP111

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**Functional Description**

The MC100ES6111 is designed for low skew clock distribution systems and supports clock frequencies up to 3 GHz[1]. The device accepts two clock sources. The CLKA input can be driven by ECL or PECL compatible signals, the CLKB input accepts ECL, PECL or HSTL compatible signals. The selected input signal is distributed to 10 identical, differential ECL/PECL outputs. If VBB is connected to the CLKA or CLKB input and bypassed to GND by a 10 nF capacitor, the MC100ES6111 can be driven by single-ended ECL/PECL signals utilizing the VBB bias voltage output.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all ten outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The MC100ES6111 can be operated from a single 3.3V or 2.5V supply. As most other ECL compatible devices, the MC100ES6111 supports positive (PECL) and negative (ECL) supplies. The MC100ES6111 is pin and function compatible to the MC100EP111.



1. AC specifications are design targets and subject to change



**Rev 0**

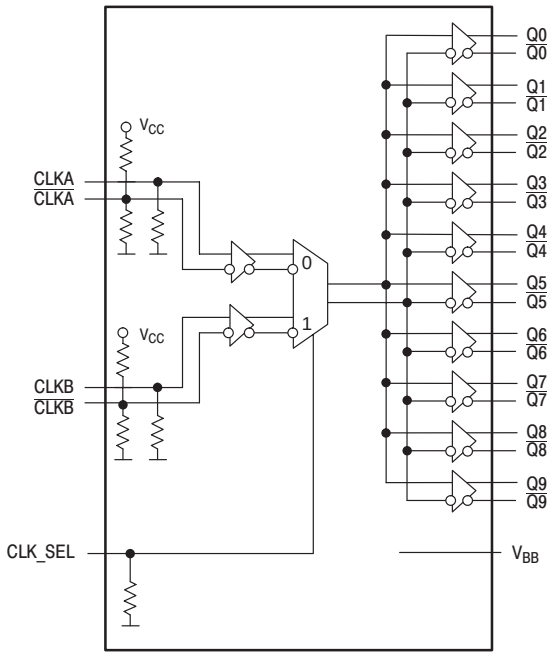


**Figure 1. MC100ES6111 Logic Diagram**

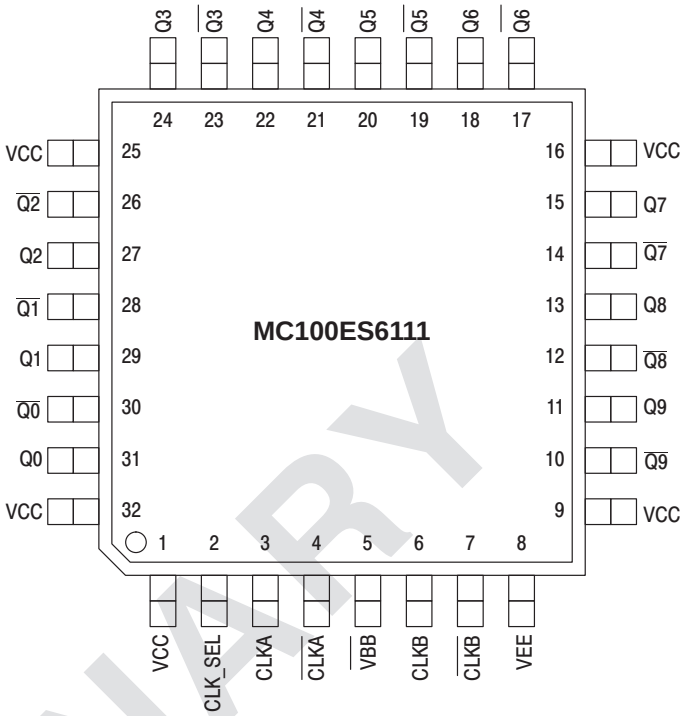


**Figure 2. 32–Lead Package Pinout** (Top View)

**Table 1. PIN CONFIGURATION**

| Pin | I/O | Type | Function |
|---|---|---|---|
| CLKA, $\overline{\text{CLKA}}$ | Input | ECL/PECL | Differential reference clock signal input |
| CLKB, $\overline{\text{CLKB}}$ | Input | ECL/PECL/HSTL | Alternative differential reference clock signal input |
| CLK_SEL | Input | ECL/PECL | Active clock input select |
| Q[0–9], $\overline{\text{Q[0–9]}}$ | Output | ECL/PECL | Differential clock outputs |
| $V_{EE}$[a] | Supply | | Negative power supply |
| $V_{CC}$ | Supply | | Positive power supply. All $V_{CC}$ pins must be connected to the positive power supply for correct DC and AC operation. |
| $V_{BB}$ | Output | DC | Reference voltage output for single ended ECL or PECL operation |

a. In ECL mode (negative power supply mode), $V_{EE}$ is either –3.3V or –2.5V and $V_{CC}$ is connected to GND (0V). In PECL mode (positive power supply mode), $V_{EE}$ is connected to GND (0V) and VCC is either +3.3V or +2.5V. In both modes, the input and output levels are referenced to the most positive supply ($V_{CC}$).

**Table 2. FUNCTION TABLE**

| Control | Default | 0 | 1 |
|---|---|---|---|
| CLK_SEL | 0 | CLKA, $\overline{\text{CLKA}}$ input pair is active. CLKa can be driven by ECL or PECL compatible signals. | CLKB, $\overline{\text{CLKB}}$ input pair is active. CLKB can be driven by either ECL, PECL, or HSTL compatible signals. |

**Table 3. Absolute Maximum Ratings[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -65 | 125 | °C | |

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 4. General Specifications**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output termination voltage | | $V_{CC}$ – 2[a] | | V | |
| MM | ESD Protection (Machine model) | TBD | | | V | |
| HBM | ESD Protection (Human body model) | TBD | | | V | |
| CDM | ESD Protection (Charged device model | TBD | | | V | |
| LU | Latch-up immunity | 200 | | | mA | |
| $C_{IN}$ | | | 4.0 | | pF | Inputs |
| $\theta_{JA}$ | Thermal resistance junction to ambient | | | | | |
| | JESD 51-3, single layer test board | | 83.1 | 86.0 | °C/W | Natural convection |
| | | | 73.3 | 75.4 | °C/W | 100 ft/min |
| | | | 68.9 | 70.9 | °C/W | 200 ft/min |
| | | | 63.8 | 65.3 | °C/W | 400 ft/min |
| | | | 57.4 | 59.6 | °C/W | 800 ft/min |
| | JESD 51-6, 2S2P multilayer test board | | 59.0 | 60.6 | °C/W | Natural convection |
| | | | 54.4 | 55.7 | °C/W | 100 ft/min |
| | | | 52.5 | 53.8 | °C/W | 200 ft/min |
| | | | 50.4 | 51.5 | °C/W | 400 ft/min |
| | | | 47.8 | 48.8 | °C/W | 800 ft/min |
| $\theta_{JC}$ | Thermal resistance junction to case | | 23.0 | 26.3 | °C/W | MIL-SPEC 883E Method 1012.1 |
| $T_J$ | Operating junction temperature[b] (continuous operation)MTBF = 9.1 years | | | 110 | °C | |

a. Output termination voltage $V_{TT}$ = 0V for $V_{CC}$ = 2.5V operation is supported but the power consumption of the device will increase

b. Operating junction temperature impacts device life time. Maximum continues operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6111 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6111 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

**Table 5. PECL/HSTL DC Characteristics** ($V_{CC}$ = 2.5V ± 5% or $V_{CC}$ = 3.3V±5%, $V_{EE}$ = GND, $T_J$ = 0°C to + 110°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Control input CLK_SEL | | | | | | |
| $V_{IL}$ | Input voltage low | $V_{CC}$ - 1.810 | | $V_{CC}$ - 1.475 | V | |
| $V_{IH}$ | Input voltage high | $V_{CC}$ - 1.165 | | $V_{CC}$ - 0.880 | V | |
| $I_{IN}$ | Input Current[a] | | | ±TBD | µA | $V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$ |
| Clock input pair CLKA, $\overline{CLKA}$, CLKB, $\overline{CLKB}$ (PECL differential signals) | | | | | | |
| $V_{PP}$ | Differential input voltage[b] | 0.1 | | 1.3 | V | Differential operation |
| $V_{CMR}$ | Differential cross point voltage[c] | 1.0 | | $V_{CC}$ - 0.3 | V | Differential operation |
| $I_{IN}$ | Input Current[a] | | | ±TBD | µA | $V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$ |
| Clock input pair CLKB, $\overline{CLKB}$ (HSTL differential signals) | | | | | | |
| $V_{DIF}$ | Differential input voltage[d]<br>$V_{CC}$ = 3.3V<br>$V_{CC}$ = 2.5V | 0.4<br>0.4 | | | V<br>V | |
| $V_X$ | Differential cross point voltage[e] | 0.68 | | 0.9 | V | |
| $I_{IN}$ | Input Current | | | ±TBD | µA | $V_{IN} = V_X \pm 0.2V$ |
| PECL clock outputs (Q0-9, $\overline{Q0\text{-}9}$) | | | | | | |
| $V_{OH}$ | Output High Voltage | TBD | $V_{CC}$ - 1.005 | TBD | V | Termination 50Ω to $V_{TT}$ |
| $V_{OL}$ | Output Low Voltage | TBD | $V_{CC}$ - 1.705 | TBD | V | Termination 50Ω to $V_{TT}$ |
| Supply current and $V_{BB}$ | | | | | | |
| $I_{EE}$ | Maximum Quiescent Supply Current without output termination current | | TBD | TBD | mA | $V_{EE}$ pin |
| $I_{CC}$ | Maximum Quiescent Supply Current, outputs terminated 50Ω to $V_{TT}$ | | TBD | TBD | mA | All $V_{CC}$ Pins |
| $V_{BB}$ | Output reference voltage | $V_{CC}$ - 1.38 | | $V_{CC}$ - 1.26 | V | $I_{BB}$ = 0.4 mA |

a. Input have internal pullup/pulldown resistors which affect the input current
b. $V_{PP}$ (DC) is the minimum differential input voltage swing required to maintain device functionality
c. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.
d. $V_{DIF}$ (DC) is the minimum differential HSTL input voltage swing required for device functionality. Only applicable to CLKB, $\overline{CLKB}$
e. $V_X$ (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the $V_X$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.

**Table 6. ECL DC Characteristics** ($V_{EE}$ = -2.5V ± 5% or $V_{EE}$ = -3.3V ± 5%, $V_{CC}$ = GND, $T_J$ = 0°C to + 110°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Control input CLK_SEL | | | | | | |
| $V_{IL}$ | Input voltage low | -1.810 | | -1.475 | V | |
| $V_{IH}$ | Input voltage high | -1.165 | | -0.880 | V | |
| $I_{IN}$ | Input Current[a] | | | ±TBD | µA | $V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$ |
| Clock input pair CLKA, $\overline{CLKA}$, CLKB, $\overline{CLKB}$ (ECL differential signals) | | | | | | |
| $V_{PP}$ | Differential input voltage[b] | 0.1 | | 1.3 | V | Differential operation |
| $V_{CMR}$ | Differential cross point voltage[c] | $V_{EE}$ + 1.0 | | -0.3 | V | Differential operation |
| $I_{IN}$ | Input Current[a] | | | ±TBD | µA | $V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$ |
| ECL clock outputs (Q0-9, $\overline{Q0\text{-}9}$) | | | | | | |
| $V_{OH}$ | Output High Voltage | TBD | -1.005 | TBD | V | Termination 50Ω to $V_{TT}$ |
| $V_{OL}$ | Output Low Voltage | TBD | -1.705 | TBD | V | Termination 50Ω to $V_{TT}$ |
| Supply current and $V_{BB}$ | | | | | | |
| $I_{EE}$ | Maximum Quiescent Supply Current without output termination current | | TBD | TBD | mA | $V_{EE}$ pin |
| $I_{CC}$ | Maximum Quiescent Supply Current, outputs terminated 50Ω to $V_{TT}$ | | TBD | TBD | mA | All $V_{CC}$ Pins |
| $V_{BB}$ | Output reference voltage | -1.38 | | -1.26 | V | $I_{BB}$ = 0.4 mA |

a. Input have internal pullup/pulldown resistors which affect the input current
b. $V_{PP}$ (DC) is the minimum differential input voltage swing required to maintain device functionality
c. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.



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**Table 7. AC Characteristics** (ECL: $V_{EE}$ = -3.3V ± 5% or $V_{EE}$ = -2.5V± 5%, $V_{CC}$ = GND) or (PECL: $V_{CC}$ = 3.3V ± 5% or $V_{CC}$ = 2.5V± 5%, $V_{EE}$ = GND, $T_J$ = 0°C to + 110°C)[a] [b]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Clock input pair CLKA, $\overline{CLKA}$, CLKB, $\overline{CLKB}$ (PECL or ECL differential signals) | | | | | | |
| $V_{PP}$ | Differential input voltage[c] (peak-to-peak) | TBD | 0.3 | 1.3 | V | |
| $V_{CMR}$ | Differential input crosspoint voltage[d]<br>PECL<br>ECL | <br>TBD<br>TBD | | <br>$V_{CC}$ - 0.3<br>-0.3 V | <br>V<br>V | |
| $f_{CLK}$ | Input Frequency | | 0-3000 | TBD | MHz | Differential |
| $t_{PD}$ | Propagation Delay CLKA or CLKB to Q0-9 | | | TBD | ps | Differential |
| Clock input pair CLKB, $\overline{CLKB}$ (HSTL differential signals) | | | | | | |
| $V_{DIF}$ | Differential input voltage[e] (peak-to-peak)[e] | 0.4 | | 1.0 | V | |
| $V_X$ | Differential input crosspoint voltage[f] | 0.68 | | 0.9 | V | |
| $f_{CLK}$ | Input Frequency | | 0 - 800 | | MHz | Differential |
| $t_{PD}$ | Propagation Delay CLKB to Q0-9 | | | TBD | ps | Differential |
| ECL clock outputs (Q0-9, $\overline{Q0\text{-}9}$) | | | | | | |
| $V_{O(P-P)}$ | Differential output voltage (peak-to-peak)<br>$f_O$ < 1.1 GHz<br>$f_O$ < 2.5 GHz<br>$f_O$ < 3.0 GHz | <br>TBD<br>TBD<br>TBD | <br>0.8<br>0.6 | | <br>V<br>V<br>V | |
| $t_{sk(O)}$ | Output-to-output skew | | | 35 | ps | Differential |
| $t_{sk(PP)}$ | Output-to-output skew (part-to-part) | | | TBD | ps | Differential |
| $t_{JIT(CC)}$ | Output cycle-to-cycle jitter | | | | | |
| $DC_O$ | Output duty cycle | TBD | 50 | TBD | % | $DC_{fref}$ = 50% |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.05 | | TBD | ns | 20% to 80% |

a. AC characteristics are design targets and pending characterization
b. AC characteristics apply for parallel output termination of 50 Ω to $V_{TT}$
c. $V_{PP}$ (AC) is the minimum differential ECL/PECL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew
d. $V_{CMR}$ (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ (AC) range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ (AC) or $V_{PP}$ (AC) impacts the device propagation delay, device and part-to-part skew
e. $V_{DIF}$ (AC) is the minimum differential HSTL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew. Only applicaple to CLKB.
f. $V_X$ (AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the $V_X$ (AC) range and the input swing lies within the $V_{DIF}$ (AC) specification. Violation of $V_X$ (AC) or $V_{DIF}$ (AC) impacts the device propagation delay, device and part-to-part skew



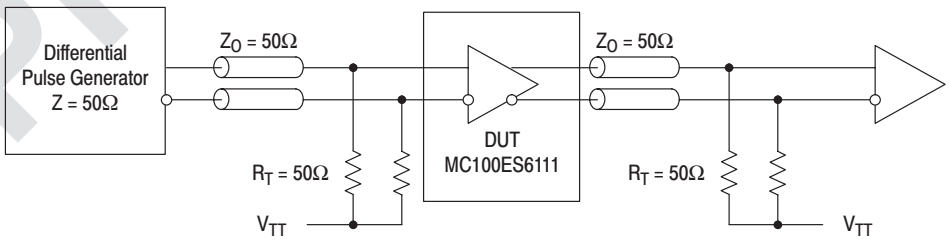


**Figure 3. MC100ES6111 AC test reference**

**Order Number: MC100ES6210/D**
**Rev 0, 11/2001**

*Product Preview*

# Low Voltage 2.5/3.3V Differential ECL/PECL/HSTL Fanout Buffer

**MC100ES6210**

**Low Voltage Dual 1:5 Differential PECL/ECL/HSTL Clock Fanout Buffer**



The Motorola MC100ES6210 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6210 supports various applications that require to distribute precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low clock skew outputs and superior digital signal characteristics. Target applications for this clock driver is high performance clock distribution in computing, networking and telecommunication systems.

**Features:**

- Dual 1:5 differential clock distribution
- 35 ps maximum device skew[1]
- Fully differential architecture from input to all outputs
- SiGe technology supports near-zero output skew
- Supports DC to 3GHz operation of clock or data signals
- ECL/PECL compatible differential clock outputs
- ECL/PECL compatible differential clock inputs
- Single 3.3V, -3.3V, 2.5V or -2.5V supply
- Standard 32 lead LQFP package
- Industrial temperature range
- Pin and function compatible to the MC100EP210

**FA SUFFIX**
32–LEAD LQFP PACKAGE
CASE 873A

6

**Functional Description**

The MC100ES6210 is designed for low skew clock distribution systems and supports clock frequencies up to 3 GHz[1]. The device consists of two independent 1:5 clock fanout buffers. The input signal of each fanout buffer is distributed to five identical, differential ECL/PECL outputs. Both CLKA and CLKB inputs can be driven by ECL/PECL compatible signals.

If VBB is connected to the CLKA or CLKB input and bypassed to GND by a 10 nF capacitor, the MC100ES6210 can be driven by single-ended ECL/PECL signals utilizing the VBB bias voltage output.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all ten outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The MC100ES6210 can be operated from a single 3.3V or 2.5V supply. As most other ECL compatible devices, the MC100ES6210 supports positive (PECL) and negative (ECL) supplies. The is function and pin compatible to the MC100EP210.

1. AC specifications are design targets and subject to change



**Rev 0**

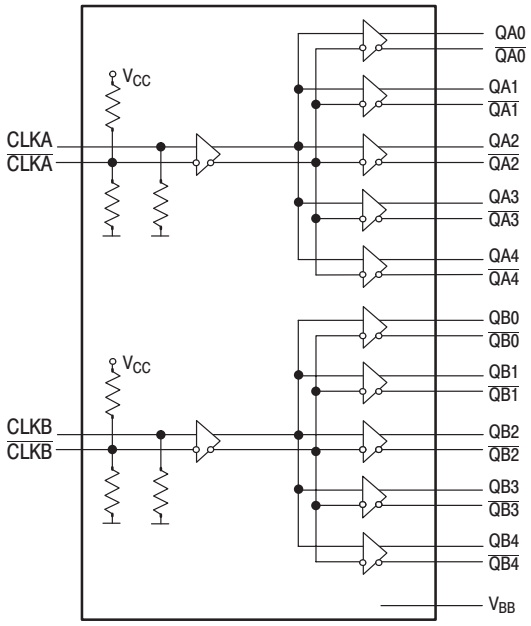


**Figure 1. MC100ES6210 Logic Diagram**

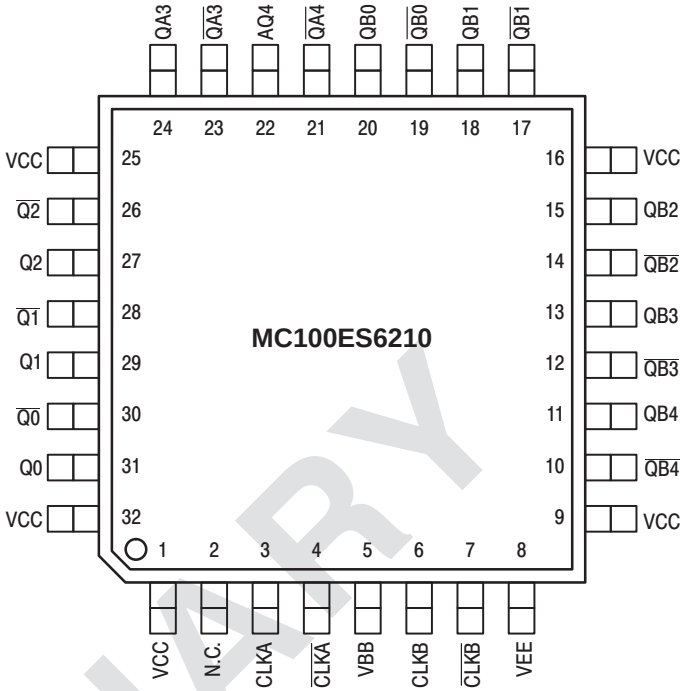


**Figure 2. 32–Lead Package Pinout** (Top View)

**Table 1. Pin configuration**

| Pin | I/O | Type | Function |
|---|---|---|---|
| CLKA, $\overline{\text{CLKA}}$ | Input | ECL/PECL | Differential reference clock signal input (fanout buffer A) |
| CLKB, $\overline{\text{CLKB}}$ | Input | ECL/PECL | Differential reference clock signal input (fanout buffer B) |
| QA[0-4], $\overline{\text{QA[0-4]}}$ | Output | ECL/PECL | Differential clock outputs (fanout buffer A) |
| QB[0-4], $\overline{\text{QB[0-4]}}$ | Output | ECL/PECL | Differential clock outputs (fanout buffer B) |
| VEE[a] | Supply | | Negative power supply |
| $V_{CC}$ | Supply | | Positive power supply. All $V_{CC}$ pins must be connected to the positive power supply for correct DC and AC operation. |
| VBB | Output | DC | Reference voltage output for single ended ECL or PECL operation |

a. In ECL mode (negative power supply mode), VEE is either -3.3V or -2.5V and VCC is connected to GND (0V).
In PECL mode (positive power supply mode), VEE is connected to GND (0V) and VCC is either +3.3V or +2.5V .
In both modes, the input and output levels are referenced to the most positive supply (VCC).



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**Table 2. ABSOLUTE MAXIMUM RATINGS[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -65 | 125 | °C | |

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 3. General Specifications**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output termination voltage | | $V_{CC}$ - 2[a] | | V | |
| MM | ESD Protection (Machine model) | TBD | | | V | |
| HBM | ESD Protection (Human body model) | TBD | | | V | |
| CDM | ESD Protection (Charged device model | TBD | | | V | |
| LU | Latch-up immunity | 200 | | | mA | |
| $C_{IN}$ | | | 4.0 | | pF | Inputs |
| $\theta_{JA}$ | Thermal resistance junction to ambient | | | | | |
| | JESD 51-3, single layer tes board | | 83.1 | 86.0 | °C/W | Natural convection |
| | | | 73.3 | 75.4 | °C/W | 100 ft/min |
| | | | 68.9 | 70.9 | °C/W | 200 ft/min |
| | | | 63.8 | 65.3 | °C/W | 400 ft/min |
| | | | 57.4 | 59.6 | °C/W | 800 ft/min |
| | JESD 51-6, 2S2P multilayer test board | | 59.0 | 60.6 | °C/W | Natural convection |
| | | | 54.4 | 55.7 | °C/W | 100 ft/min |
| | | | 52.5 | 53.8 | °C/W | 200 ft/min |
| | | | 50.4 | 51.5 | °C/W | 400 ft/min |
| | | | 47.8 | 48.8 | °C/W | 800 ft/min |
| $\theta_{JC}$ | Thermal resistance junction to case | | 23.0 | 26.3 | °C/W | MIL-SPEC 883E Method 1012.1 |
| $T_J$ | Operating junction temperature[b] (continuous operation) MTBF = 9.1 years | | | 110 | °C | |

a. Output termination voltage $V_{TT}$ = 0V for $V_{CC}$ = 2.5V operation is supported but the power consumption of the device will increase

b. Operating junction temperature impacts device life time. Maximum continues operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6210 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6210 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

**Table 4. PECL DC Characteristics** ($V_{CC}$ = 2.5V + 5% or $V_{CC}$ = 3.3V + 5%, $V_{EE}$ = GND, $T_J$ = 0°C to +110°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Clock input pair CLKA, $\overline{\text{CLKA}}$, CLKB, $\overline{\text{CLKB}}$ (PECL differential signals) | | | | | | |
| $V_{PP}$ | Differential input voltage[a] | 0.1 | | 1.3 | V | Differential operation |
| $V_{CMR}$ | Differential cross point voltage[b] | 1.0 | | $V_{CC}$ - 0.3 | V | Differential operation |
| $I_{IN}$ | Input Current[a] | | | ±TBD | µA | $V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$ |
| PECL clock outputs (QA0-4, $\overline{\text{QA0-4}}$, QB0-4, $\overline{\text{QB0-4}}$) | | | | | | |
| $V_{OH}$ | Output High Voltage | TBD | $V_{CC}$-1.005 | TBD | V | Termination 50Ω to $V_{TT}$ |
| $V_{OL}$ | Output Low Voltage | TBD | $V_{CC}$-1.705 | TBD | V | Termination 50Ω to $V_{TT}$ |
| Supply current and $V_{BB}$ | | | | | | |
| $I_{EE}$ | Maximum Quiescent Supply Current without output termination current | | TBD | TBD | mA | $V_{EE}$ pin |
| $I_{CC}$ | Maximum Quiescent Supply Current, outputs terminated 50Ω to $V_{TT}$ | | TBD | TBD | mA | All $V_{CC}$ Pins |
| $V_{BB}$ | Output reference voltage | $V_{CC}$-1.38 | | $V_{CC}$-1.26 | V | $I_{BB}$ = 0.4 mA |

a. $V_{PP}$ (DC) is the minimum differential input voltage swing required to maintain device functionality
b. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.

**Table 5. ECL DC Characteristics** ($V_{EE}$ = -2.5V+5% or $V_{EE}$ = -3.3V+5%, $V_{CC}$ = GND, $T_J$ = 0°C to +110°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Clock input pair CLKA, $\overline{\text{CLKA}}$, CLKB, $\overline{\text{CLKB}}$ (ECL differential signals) | | | | | | |
| $V_{PP}$ | Differential input voltage[a] | 0.1 | | 1.3 | V | Differential operation |
| $V_{CMR}$ | Differential cross point voltage[b] | $V_{EE}$ + 1.0 | | -0.3 | V | Differential operation |
| $I_{IN}$ | Input Current[a] | | | ±TBD | µA | $V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$ |
| ECL clock outputs (QA0-4, $\overline{\text{QA0-4}}$, QB0-4, $\overline{\text{QB0-4}}$) | | | | | | |
| $V_{OH}$ | Output High Voltage | TBD | -1.005 | TBD | V | Termination 50Ω to $V_{TT}$ |
| $V_{OL}$ | Output Low Voltage | TBD | -1.705 | TBD | V | Termination 50Ω to $V_{TT}$ |
| Supply current and $V_{BB}$ | | | | | | |
| $I_{EE}$ | Maximum Quiescent Supply Current without output termination current | | TBD | TBD | mA | $V_{EE}$ pin |
| $I_{CC}$ | Maximum Quiescent Supply Current, outputs terminated 50Ω to $V_{TT}$ | | TBD | TBD | mA | All $V_{CC}$ Pins |
| $V_{BB}$ | Output reference voltage | -1.38 | | -1.26 | V | $I_{BB}$ = 0.4 mA |

a. $V_{PP}$ (DC) is the minimum differential input voltage swing required to maintain device functionality
b. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.

**Table 6. AC Characteristics** (ECL: $V_{EE}$ = -3.3V + 5% or $V_{EE}$ = -2.5V+ 5%, $V_{CC}$ = GND) or (PECL: $V_{CC}$ = 3.3V + 5% or $V_{CC}$ = 2.5V+ 5%, $V_{EE}$ = GND, $T_J$ = 0°C to +110°C)[a b]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Clock input pair CLKA, $\overline{\text{CLKA}}$, CLKB, $\overline{\text{CLKB}}$ (PECL or ECL differential signals) | | | | | | |
| $V_{PP}$ | Differential input voltage[c] (peak-to-peak) | TBD | 0.3 | 1.3 | V | |
| $V_{CMR}$ | Differential input crosspoint voltage[d]<br>PECL<br>ECL | <br>TBD<br>TBD | | <br>$V_{CC}$ - 0.3<br>-0.3V | <br>V<br>V | |
| ECL clock outputs (Q0-9, $\overline{\text{Q0-9}}$) | | | | | | |
| $f_{CLK}$ | Input Frequency | | 0-3000 | TBD | MHz | Differential |
| $t_{PD}$ | Propagation Delay<br>CLKA to QAx or CLKB to QBx | | | <br>TBD | <br>ps | <br>Differential |
| $V_{O(P-P)}$ | Differential output voltage (peak-to-peak)<br>$f_O$ < 1.1 GHz<br>$f_O$ < 2.5 GHz<br>$f_O$ < 3.0 GHz | <br>TBD<br>TBD<br>TBD | <br>0.8<br>0.6 | | <br>V<br>V<br>V | |
| $t_{sk(O)}$ | Output-to-output skew | | | 35 | ps | Differential |
| $t_{sk(PP)}$ | Output-to-output skew (part-to-part) | | | TBD | ps | Differential |
| $t_{JIT(CC)}$ | Output cycle-to-cycle jitter | | | | | |
| $DC_O$ | Output duty cycle | TBD | 50 | TBD | % | $DC_{fref}$ = 50% |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.05 | | TBD | ns | 20% to 80% |

a. AC characteristics are design targets and pending characterization
b. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$
c. $V_{PP}$ (AC) is the minimum differential ECL/PECL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew
d. $V_{CMR}$ (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ (AC) range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ (AC) or $V_{PP}$ (AC) impacts the device propagation delay, device and part-to-part skew

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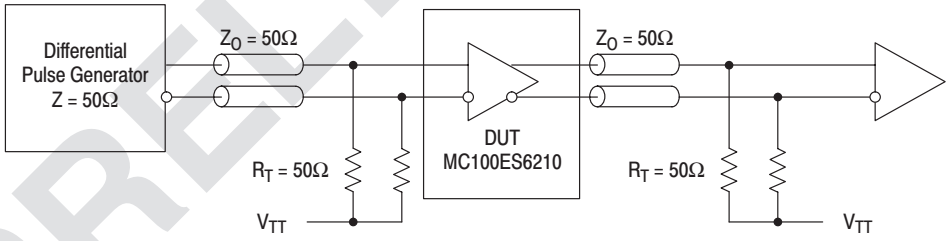


**Figure 3. MC100ES6210 AC test reference**

**Order Number: MC100ES6220/D**
**Rev 0, 11/2001**

*Preliminary Information*

# Low Voltage Dual 1:10 Differential ECL/PECL Clock Fanout Buffer

**MC100ES6220**

**LOW VOLTAGE DUAL 1:10 DIFFERENTIAL ECL/PECL CLOCK FANOUT BUFFER**

**TB SUFFIX**
52–LEAD LQFP PACKAGE
EXPOSED PAD
CASE 1336

The Motorola MC100ES6220 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6220 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver are high performance clock distribution in computing, networking and telecommunication systems.

**Features**

- Two independent 1:10 differential clock fanout buffers
- 35 ps maximum device skew[1]
- SiGe technology
- Supports DC to 3GHz operation[1] of clock or data signals
- ECL/PECL compatible differential clock outputs
- ECL/PECL compatible differential clock inputs
- Single 3.3V, -3.3V, 2.5V or -2.5V supply
- Standard 52 lead LQFP package with exposed pad for enhanced thermal characteristics
- Supports industrial temperature range
- Pin and function compatible to the MC100EP220

**Functional Description**

The MC100ES6220 is designed for low skew clock distribution systems and supports clock frequencies up to 3 GHz[1]. The device consists of two independent clock fanout buffers. The CLKA and CLKB inputs can be driven by ECL or PECL compatible signals. The input signal of each clock buffer is distributed to 10 identical, differential ECL/PECL outputs. If VBB is connected to the $\overline{\text{CLKA}}$ or $\overline{\text{CLKB}}$ input and bypassed to GND by a 10 nF capacitor, the MC100ES6220 can be driven by single-ended ECL/PECL signals utilizing the VBB bias voltage output.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all ten outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The MC100ES6220 can be operated from a single 3.3V or 2.5V supply. As most other ECL compatible devices, the MC100ES6220 supports positive (PECL) and negative (ECL) supplies. The MC100ES6220 is pin and function compatible to the MC100EP220.



6

1. AC specifications are design targets and subject to change


**Rev 0**

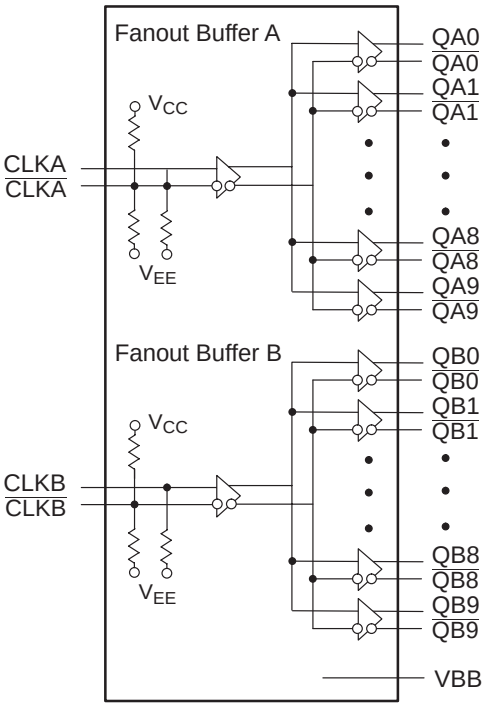


**Figure 1. MC100ES6220 Logic Diagram**

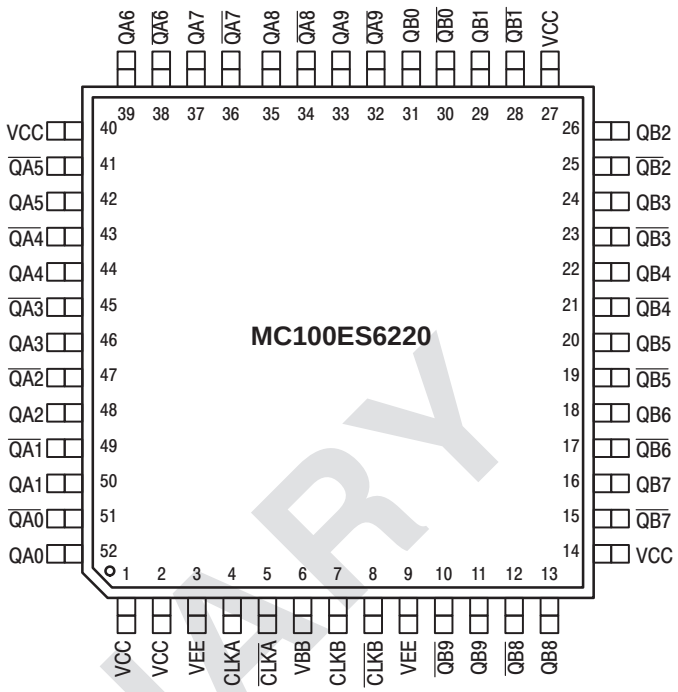


**Figure 2. 52–Lead Package Pinout** (Top View)

**Table 1. Pin configuration**

| Pin | I/O | Type | Function |
|---|---|---|---|
| CLKA, $\overline{\text{CLKA}}$ | Input | ECL/PECL | Differential reference clock signal input for fanout buffer A |
| CLKB, $\overline{\text{CLKB}}$ | Input | ECL/PECL | Differential reference clock signal input for fanout buffer B |
| QA[0-9], $\overline{\text{QA[0-9]}}$ | Output | ECL/PECL | Differential clock outputs of fanout buffer A |
| QB[0-9], $\overline{\text{QB[0-9]}}$ | Output | ECL/PECL | Differential clock outputs of fanout buffer B |
| VEE[a] | Supply | | Negative power supply |
| $V_{CC}$ | Supply | | Positive power supply. All $V_{CC}$ pins must be connected to the positive power supply for correct DC and AC operation. |
| VBB | Output | DC | Reference voltage output for single ended ECL or PECL operation |

a. In ECL mode (negative power supply mode), VEE is either -3.3V or -2.5V and VCC is connected to GND (0V). In PECL mode (positive power supply mode), VEE is connected to GND (0V) and VCC is either +3.3V or +2.5V. In both modes, the input and output levels are referenced to the most positive supply (VCC).

**Table 2. Absolute Maximum Ratings[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -65 | 125 | °C | |

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 3. General Specifications**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output termination voltage | | $V_{CC}$ - 2[a] | | V | |
| MM | ESD Protection (Machine model) | 200 | | | V | |
| HBM | ESD Protection (Human body model) | 2000 | | | V | |
| CDM | ESD Protection (Charged device model | TBD | | | V | |
| LU | Latch-up immunity | 200 | | | mA | |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | Inputs |
| $\theta_{JA}$ ,$\theta_{JC}$ $\theta_{JB}$ | Thermal resistance (junction-to-ambient, junction-to-board, junction-to-case) | See Table 7, Thermal Resistance | | | °C/W | |
| $T_J$ | Operating junction temperature[b] (continuous operation) MTBF = 9.1 years | 0 | | 110 | °C | |

a. Output termination voltage $V_{TT}$ = 0V for $V_{CC}$ = 2.5V operation is supported but the power consumption of the device will increase.
b. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6220 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6220 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

**Table 4. PECL DC Characteristics** ($V_{CC}$ = 2.5V ± 5% or $V_{CC}$ = 3.3V ± 5%, $V_{EE}$ = GND, $T_J$ = 0°C to +110°C)[a]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Clock input pair CLKA, $\overline{\text{CLKA}}$, CLKB, $\overline{\text{CLKB}}$ (PECL differential signals) | | | | | | |
| $V_{PP}$ | Differential input voltage[b] | 0.1 | | 1.3 | V | Differential operation |
| $V_{CMR}$ | Differential cross point voltage[c] | 1.0 | | $V_{CC}$ - 0.3 | V | Differential operation |
| $I_{IN}$ | Input Current[a] | | | ±150 | µA | $V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$ |
| Clock inputs (PECL single ended signals) | | | | | | |
| $V_{IL}$ | Input voltage low | | | $V_{CC}$ - 1.46 | V | |
| $V_{IH}$ | Input voltage high | $V_{CC}$ - 1.14 | | | V | |
| $I_{IN}$ | Input Current[d] | | | ±150 | µA | $V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$ |
| PECL clock outputs (QA0-A9, $\overline{\text{QA0-A9}}$, QB0-B9, $\overline{\text{QB0-B9}}$) | | | | | | |
| $V_{OH}$ | Output High Voltage | TBD | $V_{CC}$-1.005 | TBD | V | Termination 50Ω to $V_{TT}$ |
| $V_{OL}$ | Output Low Voltage | TBD | $V_{CC}$-1.705 | TBD | V | Termination 50Ω to $V_{TT}$ |
| Supply current and $V_{BB}$ | | | | | | |
| $I_{EE}$ | Maximum Quiescent Supply Current without output termination current | | TBD | TBD | mA | $V_{EE}$ pins |
| $I_{CC}$[e] | Maximum Quiescent Supply Current, outputs terminated 50Ω to $V_{TT}$ | | TBD | TBD | mA | $V_{CC}$ pins |
| $V_{BB}$ | Output reference voltage | $V_{CC}$ - 1.36 | | $V_{CC}$ - 1.24 | V | $I_{BB}$ = 0.4 mA |

a. DC characteristics are design targets and pending characterization.
b. $V_{PP}$ (DC) is the minimum differential input voltage swing required to maintain device functionality.
c. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.
d. Input have internal pullup/pulldown resistors which affect the input current.
e. $I_{CC}$ includes current through the output resistors (all outputs terminated to $V_{TT}$).



6

**Table 5. ECL DC Characteristics** ($V_{EE}$ = -2.5V ± 5% or $V_{EE}$ = -3.3V ± 5%, $V_{CC}$ = GND, $T_J$ = 0°C to +110°C)[a]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Clock input pair CLKA, $\overline{\text{CLKA}}$, CLKB, $\overline{\text{CLKB}}$ (ECL differential signals) | | | | | | |
| $V_{PP}$ | Differential input voltage[b] | 0.1 | | 1.3 | V | Differential operation |
| $V_{CMR}$ | Differential cross point voltage[c] | $V_{EE}$ + 1.0 | | -0.3 | V | Differential operation |
| $I_{IN}$ | Input Current[a] | | | ±150 | µA | $V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$ |
| Clock inputs (ECL single ended signals) | | | | | | |
| $V_{IL}$ | Input voltage low | | | -1.46 | V | |
| $V_{IH}$ | Input voltage high | -1.14 | | | V | |
| $I_{IN}$ | Input Current[d] | | | ±150 | µA | $V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$ |
| ECL clock outputs (QA0-A9, $\overline{\text{QA0-A9}}$, QB0-B9, $\overline{\text{QB0-B9}}$) | | | | | | |
| $V_{OH}$ | Output High Voltage | TBD | -1.005 | TBD | V | Termination 50Ω to $V_{TT}$ |
| $V_{OL}$ | Output Low Voltage | TBD | -1.705 | TBD | V | Termination 50Ω to $V_{TT}$ |
| Supply current and $V_{BB}$ | | | | | | |
| $I_{EE}$ | Maximum Quiescent Supply Current without output termination current | | TBD | 190 | mA | $V_{EE}$ pins |
| $I_{CC}$[e] | Maximum Quiescent Supply Current, outputs terminated 50Ω to $V_{TT}$ | | TBD | 750 | mA | $V_{CC}$ pins |
| $V_{BB}$ | Output reference voltage | -1.36 | | -1.24 | V | $I_{BB}$ = 0.4 mA |

a. DC characteristics are design targets and pending characterization.
b. $V_{PP}$ (DC) is the minimum differential input voltage swing required to maintain device functionality.
c. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.
d. Input have internal pullup/pulldown resistors which affect the input current.
e. $I_{CC}$ includes current through the output resistors (all outputs terminated to $V_{TT}$).

6

**Table 6. AC Characteristics** (ECL: $V_{EE}$ = -3.3V ± 5% or $V_{EE}$ = -2.5V ± 5%, $V_{CC}$ = GND) or (PECL: $V_{CC}$ = 3.3V ± 5% or $V_{CC}$ = 2.5V ± 5%, $V_{EE}$ = GND, $T_J$ = 0°C to +110°C)[a b]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Clock input pair CLKA, $\overline{\text{CLKA}}$, CLKB, $\overline{\text{CLKB}}$ (PECL or ECL differential signals) | | | | | | |
| $V_{PP}$ | Differential input voltage[c] (peak-to-peak) | TBD | 0.3 | 1.3 | V | |
| $V_{CMR}$ | Differential input crosspoint voltage[d] PECL<br>ECL | TBD<br>TBD | | $V_{CC}$ - 0.3<br>-0.3V | V<br>V | |
| $f_{CLK}$ | Input Frequency | | 0 - 3000 | TBD | MHz | Differential |
| PECL/ECL clock outputs (QA0-A9, $\overline{\text{QA0-A9}}$, QB0-B9, $\overline{\text{QB0-B9}}$) | | | | | | |
| $t_{PD}$ | Propagation Delay CLKx to Qx0-9 | | | TBD | ps | Differential |
| $V_{O(P-P)}$ | Differential output voltage (peak-to-peak)<br>$f_O$ < 1.1 GHz<br>$f_O$ < 2.5 GHz<br>$f_O$ < 3.0 GHz | <br>TBD<br>TBD<br>TBD | <br>0.8<br>0.6 | | <br>V<br>V<br>V | |
| $t_{sk(O)}$ | Output-to-output skew | | | 35 | ps | Differential |
| $t_{sk(PP)}$ | Output-to-output skew (part-to-part) | | | TBD | ps | Differential |
| $t_{JIT(CC)}$ | Output cycle-to-cycle jitter | | | | | |
| $DC_O$ | Output duty cycle | TBD | 50 | TBD | % | $DC_{fref}$ = 50% |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.05 | | TBD | ns | 20% to 80% |

a. AC characteristics are design targets and pending characterization.
b. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
c. $V_{PP}$ (AC) is the minimum differential ECL/PECL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
d. $V_{CMR}$ (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ (AC) range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ (AC) or $V_{PP}$ (AC) impacts the device propagation delay, device and part-to-part skew.





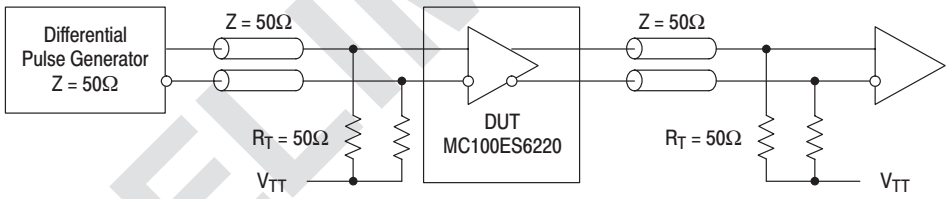


**Figure 3. MC100ES6220 AC test reference**

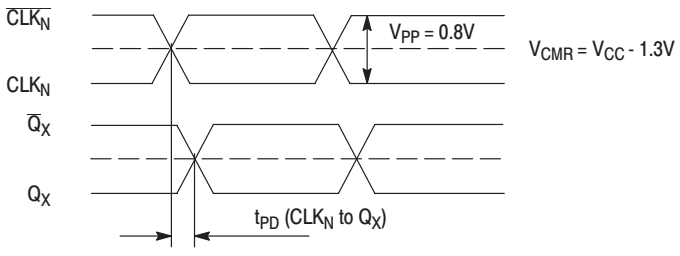


**Figure 4. MC100ES6220 AC reference measurement waveform**

## APPLICATIONS INFORMATION

### Using the thermally enhanced package of the MC100ES6220

The MC100ES6220 uses a thermally enhanced exposed pad (EP) 52 lead LQFP package. The package is molded so that the leadframe is exposed at the surface of the package bottom side. The exposed metal pad will provide the low thermal impedance that supports the power consumption of the MC100ES6220 high-speed bipolar integrated circuit and eases the power management task for the system design. A thermal land pattern on the printed circuit board and thermal vias are recommended in order to take advantage of the enhanced thermal capabilities of the MC100ES6220. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal path. In multilayer board designs, thermal vias thermally connect the exposed pad to internal copper planes. Number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package. A nine thermal via array, arranged in a 3 x 3 array and using a 1.2 mm pitch in the center of the thermal land is the absolute minimum requirement for MC100ES6220 applications on multi-layer boards. The recommended thermal land design comprises a 5 x 5 thermal via array as shown in Figure 5 “Recommended thermal land pattern”, providing an efficient heat removal path.

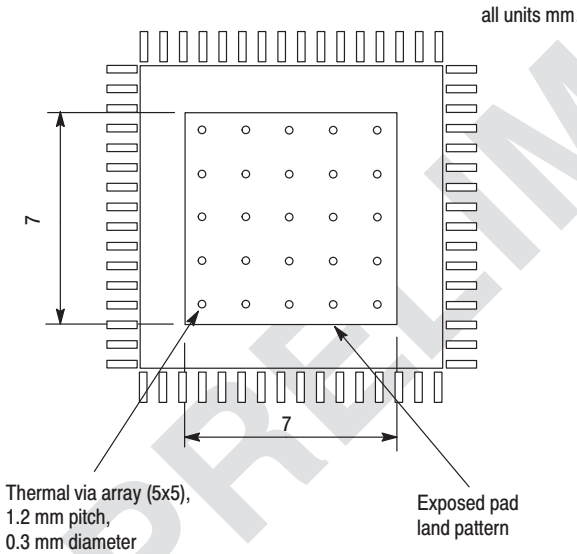


**Figure 5. Recommended thermal land pattern**

The via diameter is should be approx. 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via resulting in voids during the solder process must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for exposed pad package is equivalent to standard surface mount packages. Figure 6 “Recommended solder mask openings” shows a recommend solder mask opening with respect to the recommended 5 x 5 thermal via array. Because a large solder mask opening may result in a poor release, the opening should be subdivided as shown in Figure 6 For the nominal package standoff 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

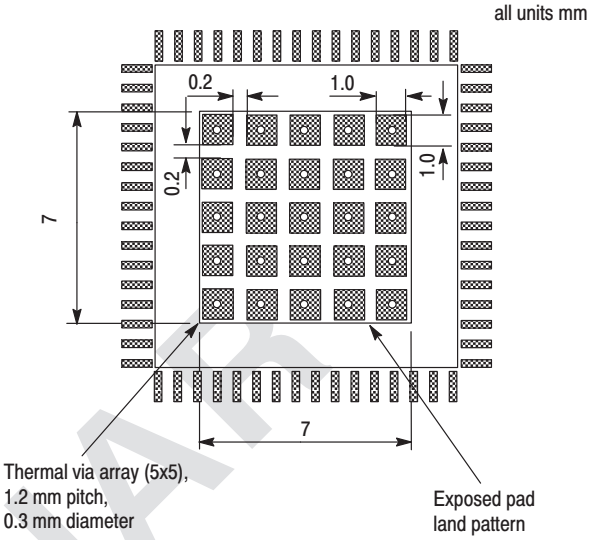


**Figure 6. Recommended solder mask openings**

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided. For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

**Table 7. Thermal Resistance[a]**

| Convection-LFPM | $R_{THJA}$[b] °C/W | $R_{THJA}$[c] °C/W | $R_{THJC}$[d] °C/W | $R_{THJB}$[e] °C/W |
|---|---|---|---|---|
| Natural | 57.1 | 24.9 | 15.8 | 9.7 |
| 100 | 50.0 | 21.3 | | |
| 200 | 46.9 | 20.0 | | |
| 400 | 43.4 | 18.7 | | |
| 800 | 38.6 | 16.9 | | |

a. Thermal data pattern with a 3 x 3 thermal via array on 2S2P boards (based on empirical results)
b. Junction to ambient, single layer test board, per JESD51-6
c. Junction to ambient, four conductor layer test board (2S2P), per JES51-6
d. Junction to case, per MIL-SPEC 883E, method 1012.1
e. Junction to board, four conductor layer test board (2S2P) per JESD 51-8

It is recommended that users employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100ES6220 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals. The thermal land should be connected to GND through connection of internal board layers.

**Order Number: MC100ES6221/D**
**Rev 0, 11/2001**

*Preliminary Information*

# Low Voltage 1:20 Differential ECL/PECL/HSTL Clock Fanout Buffer

**MC100ES6221**

**LOW–VOLTAGE 1:20 DIFFERENTIAL ECL/PECL/HSTL CLOCK FANOUT DRIVER**

**TB SUFFIX**
52–LEAD LQFP PACKAGE
EXPOSED PAD
CASE 1336

The Motorola MC100ES6221 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6221 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver is high performance clock distribution in computing, networking and telecommunication systems.

**Features**

- 1:20 differential clock fanout buffer
- 35 ps maximum device skew[1]
- SiGe technology
- Supports DC to 3 GHz operation[1] of clock or data signals
- ECL/PECL compatible differential clock outputs
- ECL/PECL/HSTL compatible differential clock inputs
- Single 3.3V, -3.3V, 2.5V or -2.5V supply
- Standard 52 lead LQFP package with exposed pad for enhanced thermal characteristics
- Supports industrial temperature range
- Pin and function compatible to the MC100EP211

**Functional Description**

The MC100ES6221 is designed for low skew clock distribution systems and supports clock frequencies up to 3 GHz[1]. The device accepts two clock sources. The CLK0 input can be driven by ECL or PECL compatible signals, the CLK1 input accepts ECL, PECL or HSTL compatible signals. The selected input signal is distributed to 20 identical, differential ECL/PECL outputs. If VBB is connected to the $\overline{\text{CLK0}}$ or $\overline{\text{CLK1}}$ input and bypassed to GND by a 10 nF capacitor, the MC100ES6221 can be driven by single-ended ECL/PECL signals utilizing the VBB bias voltage output.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all ten outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The MC100ES6221 can be operated from a single 3.3V or 2.5V supply. As most other ECL compatible devices, the MC100ES6221 supports positive (PECL) and negative (ECL) supplies. The MC100ES6221 is pin and function compatible to the MC100EP221.



6

1. AC specifications are design targets and subject to change



**Rev 0**

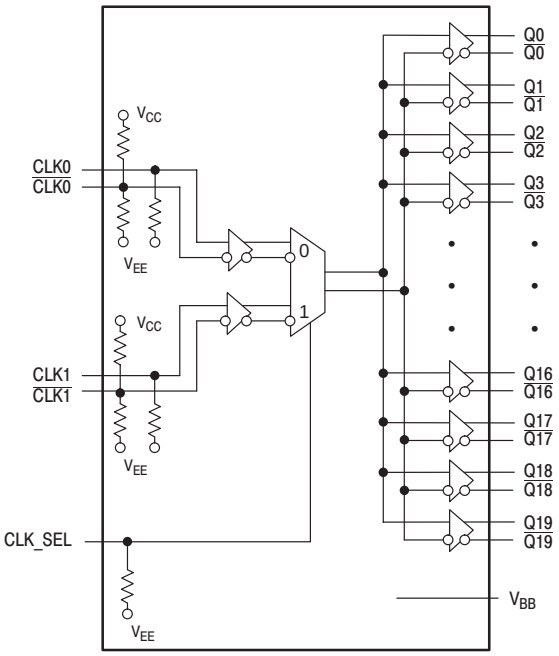


**Figure 1. MC100ES6221 Logic Diagram**

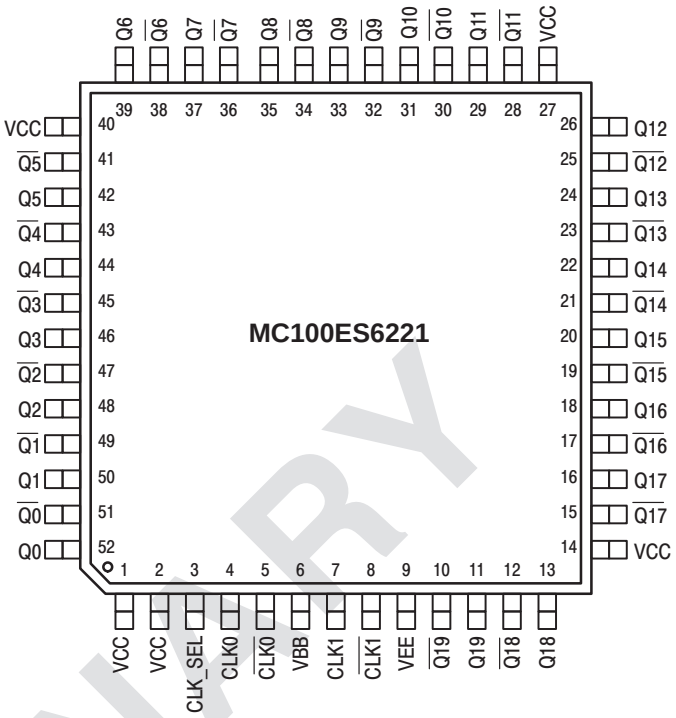


**Figure 2. 52–Lead Package Pinout** (Top View)

**Table 1. PIN CONFIGURATION**

| Pin | I/O | Type | Function |
|---|---|---|---|
| CLK0, $\overline{\text{CLK0}}$ | Input | ECL/PECL | Differential reference clock signal input |
| CLK1, $\overline{\text{CLK1}}$ | Input | ECL/PECL/HSTL | Alternative differential reference clock signal input |
| CLK_SEL | Input | ECL/PECL | Reference clock input select |
| Q[0–19], $\overline{\text{Q[0–19]}}$ | Output | ECL/PECL | Differential clock outputs |
| $V_{EE}$[a] | Supply | | Negative power supply |
| $V_{CC}$ | Supply | | Positive power supply. All $V_{CC}$ pins must be connected to the positive power supply for correct DC and AC operation. |
| $V_{BB}$ | Output | DC | Reference voltage output for single ended ECL or PECL operation |

a. In ECL mode (negative power supply mode), $V_{EE}$ is either –3.3V or –2.5V and $V_{CC}$ is connected to GND (0V). In PECL mode (positive power supply mode), $V_{EE}$ is connected to GND (0V) and VCC is either +3.3V or +2.5V. In both modes, the input and output levels are referenced to the most positive supply ($V_{CC}$).

**Table 2. FUNCTION TABLE**

| Pin | 0 | 1 |
|---|---|---|
| CLK_SEL | CLK0, $\overline{\text{CLK0}}$ input pair is the reference clock. CLK0 can be driven by ECL or PECL compatible signals. | CLK1, $\overline{\text{CLK1}}$ input pair is the reference clock. CLK1 can be driven by either ECL, PECL, or HSTL compatible signals. |

**Table 3. Absolute Maximum Ratings[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -65 | 125 | °C | |

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 4. General Specifications**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output termination voltage | | $V_{CC}$ – 2[a] | | V | |
| MM | ESD Protection (Machine model) | 200 | | | V | |
| HBM | ESD Protection (Human body model) | 2000 | | | V | |
| CDM | ESD Protection (Charged device model) | TBD | | | V | |
| LU | Latch-up immunity | 200 | | | mA | |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | Inputs |
| $\theta_{JA}$, $\theta_{JB}$, $\theta_{JC}$ | Thermal resistance (junction–to–ambient, junction–to–board, junction–to–case) | See Table 8 ”Thermal Resistance” on page 602 | | | °C/W | |
| $T_J$ | Operating junction temperature[b] (continuous operation) MTBF = 9.1 years | | | 110 | °C | |

a. Output termination voltage $V_{TT}$ = 0V for $V_{CC}$ = 2.5V operation is supported but the power consumption of the device will increase.

b. Operating junction temperature impacts device life time. Maximum continues operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6221 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6221 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

**Table 5. PECL DC Characteristics** ($V_{CC}$ = 2.5V ± 5% or $V_{CC}$ = 3.3V±5%, $V_{EE}$ = GND, $T_J$ = 0°C to + 110°C)[a]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Clock input pair CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$[b] (PECL differential signals) | | | | | | |
| $V_{PP}$ | Differential input voltage[c] | 0.1 | | 1.3 | V | Differential operation |
| $V_{CMR}$ | Differential cross point voltage[d] | 1.0 | | $V_{CC}$-0.3 | V | Differential operation |
| $I_{IN}$ | Input Current[a] | | | ±150 | µA | $V_{IN}$ = $V_{IL}$ or $V_{IN}$ = $V_{IH}$ |
| Clock input pair CLK1, $\overline{CLK1}$[e] (HSTL differential signals) | | | | | | |
| $V_{DIF}$ | Differential input voltage[f] | 0.4 | | | V | |
| $V_X$ | Differential cross point voltage[g] | 0.68 | | 0.9 | V | |
| $V_{IH}$ | Input high voltage | $V_X$+0.2 | | $V_X$+0.5 | V | |
| $V_{IL}$ | Input low voltage | $V_X$-0.5 | | $V_X$-0.2 | V | |
| $I_{IN}$ | Input Current | | | ±150 | µA | $V_{IN}$ = $V_X$ ± 0.2V |
| Clock inputs (PECL single ended signals) | | | | | | |
| $V_{IH}$ | Input voltage high | $V_{CC}$-1.165 | | $V_{CC}$-0.880 | V | |
| $V_{IL}$ | Input voltage low | $V_{CC}$-1.810 | | $V_{CC}$-1.475 | V | |
| $I_{IN}$ | Input Current[h] | | | ±150 | µA | $V_{IN}$ = $V_{IL}$ or $V_{IN}$ = $V_{IH}$ |
| PECL clock outputs (Q0-19, $\overline{Q0\text{-}19}$) | | | | | | |
| $V_{OH}$ | Output High Voltage | TBD | $V_{CC}$-1.005 | TBD | V | Termination 50Ω to $V_{TT}$ |
| $V_{OL}$ | Output Low Voltage | TBD | $V_{CC}$-1.705 | TBD | V | Termination 50Ω to $V_{TT}$ |
| Supply current and $V_{BB}$ | | | | | | |
| $I_{EE}$ | Maximum Quiescent Supply Current without output termination current | | TBD | 190 | mA | $V_{EE}$ pins |
| $I_{CCi}$ | Maximum Quiescent Supply Current, outputs terminated 50Ω to $V_{TT}$ | | TBD | 750 | mA | $V_{CC}$ pins |
| $V_{BB}$ | Output reference voltage | $V_{CC}$-1.36 | | $V_{CC}$-1.24 | V | $I_{BB}$ = 0.4 mA |

a. DC characteristics are design targets and pending characterization.
b. The input pairs CLK0, CLK1 are compatible to differential signaling standards. CLK0 is compatible to LVPECL signals and CLK1 meets both HSTL and LVPECL differential signal specifications. The difference between CLK0 and CLK1 is the differential input threshold voltage ($V_{CMR}$).
c. $V_{PP}$ (DC) is the minimum differential input voltage swing required to maintain device functionality.
d. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.
e. Clock inputs driven by differential HSTL compatible signals. Only applicable to CLK1, $\overline{CLK1}$.
f. $V_{DIF}$ (DC) is the minimum differential HSTL input voltage swing required for device functionality.
g. $V_X$ (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the $V_X$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.
h. Input have internal pullup/pulldown resistors which affect the input current.
i. $I_{CC}$ includes current through the output resistors (all outputs terminated to $V_{TT}$).

**Table 6. ECL DC Characteristics** ($V_{EE}$ = –2.5V ± 5% or $V_{EE}$ = –3.3V±5%, $V_{CC}$ = GND, $T_J$ = 0°C to + 110°C)[a]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Clock input pair CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$ (ECL differential signals) | | | | | | |
| $V_{PP}$ | Differential input voltage[b] | 0.1 | | 1.3 | V | Differential operation |
| $V_{CMR}$ | Differential cross point voltage[c] | $V_{EE}$+1.0 | | -0.3 | V | Differential operation |
| $I_{IN}$ | Input Current[a] | | | ±150 | µA | $V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$ |
| Clock inputs (ECL single ended signals) | | | | | | |
| $V_{IH}$ | Input voltage high | -1.165 | | -0.880 | V | |
| $V_{IL}$ | Input voltage low | -1.810 | | -1.475 | V | |
| $I_{IN}$ | Input Current[d] | | | ±150 | µA | $V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$ |
| ECL clock outputs (Q0-A19, $\overline{Q0\text{-}A19}$) | | | | | | |
| $V_{OH}$ | Output High Voltage | TBD | -1.005 | TBD | V | Termination 50Ω to $V_{TT}$ |
| $V_{OL}$ | Output Low Voltage | TBD | -1.705 | TBD | V | Termination 50Ω to $V_{TT}$ |
| Supply current and $V_{BB}$ | | | | | | |
| $I_{EE}$ | Maximum Quiescent Supply Current without output termination current | | TBD | 190 | mA | $V_{EE}$ pins |
| $I_{CCe}$ | Maximum Quiescent Supply Current, outputs terminated 50Ω to $V_{TT}$ | | TBD | 750 | mA | $V_{CC}$ pins |
| $V_{BB}$ | Output reference voltage | -1.36 | | -1.24 | V | $I_{BB}$ = 0.4 mA |

a. DC characteristics are design targets and pending characterization.
b. $V_{PP}$ (DC) is the minimum differential input voltage swing required to maintain device functionality.
c. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.
d. Input have internal pullup/pulldown resistors which affect the input current.
e. $I_{CC}$ includes current through the output resistors (all outputs terminated to $V_{TT}$).

**Table 7. AC Characteristics** (ECL: $V_{EE}$ = -3.3V ± 5% or $V_{EE}$ = -2.5V± 5%, $V_{CC}$ = GND) or (PECL: $V_{CC}$ = 3.3V ± 5% or $V_{CC}$ = 2.5V± 5%, $V_{EE}$ = GND, $T_J$ = 0°C to + 110°C)[a] [b]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Clock input pair CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$ (PECL or ECL differential signals) | | | | | | |
| $V_{PP}$ | Differential input voltage[c] (peak-to-peak) | TBD | 0.3 | 1.3 | V | |
| $V_{CMR}$ | Differential input crosspoint voltage[d] PECL<br>ECL | TBD<br>TBD | | $V_{CC}$-0.3<br>-0.3V | V<br>V | |
| $f_{CLK}$ | Input Frequency | | 0-3000 | TBD | MHz | Differential |
| $t_{PD}$ | Propagation Delay CLK0 or CLK1 to Q0-19 | | | TBD | ps | Differential |
| Clock input pair CLK1, $\overline{CLK1}$ (HSTL differential signals) | | | | | | |
| $V_{DIF}$ | Differential input voltage[e] (peak-to-peak) | 0.4 | | 1.0 | V | |
| $V_X$ | Differential input crosspoint voltage[f] | 0.68 | | 0.9 | V | |
| $f_{CLK}$ | Input Frequency | | 0-800 | | MHz | Differential |
| $t_{PD}$ | Propagation Delay CLKB to Q0-19 | | | TBD | ps | Differential |
| PECL/ECL clock outputs (Q0-19, $\overline{Q0\text{-}19}$) | | | | | | |
| $V_{O(P\text{-}P)}$ | Differential output voltage (peak-to-peak)<br>$f_O$ < 1.1 GHz<br>$f_O$ < 2.5 GHz<br>$f_O$ < 3.0 GHz | <br>TBD<br>TBD<br>TBD | <br>0.8<br>0.6 | | <br>V<br>V<br>V | |
| $t_{sk(O)}$ | Output-to-output skew | | | 35 | ps | Differential |
| $t_{sk(PP)}$ | Output-to-output skew (part-to-part) | | | TBD | ps | Differential |
| $t_{JIT(CC)}$ | Output cycle-to-cycle jitter | | | | | |
| $DC_O$ | Output duty cycle | TBD | 50 | TBD | % | $DC_{fref}$= 50% |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.05 | | TBD | ns | 20% to 80% |

a. AC characteristics are design targets and pending characterization.
b. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
c. $V_{PP}$ (AC) is the minimum differential ECL/PECL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
d. $V_{CMR}$ (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ (AC) range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ (AC) or $V_{PP}$ (AC) impacts the device propagation delay, device and part-to-part skew.
e. $V_{DIF}$ (AC) is the minimum differential HSTL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew. Only applicable to CLKB.
f. $V_X$ (AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the $V_X$ (AC) range and the input swing lies within the $V_{DIF}$ (AC) specification. Violation of $V_X$ (AC) or $V_{DIF}$ (AC) impacts the device propagation delay, device and part-to-part skew.

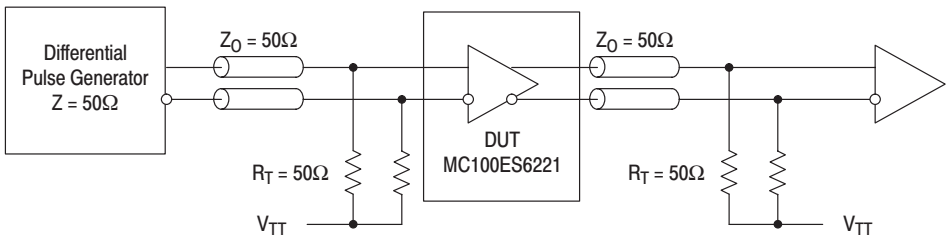


**Figure 3. MC100ES6221 AC test reference**

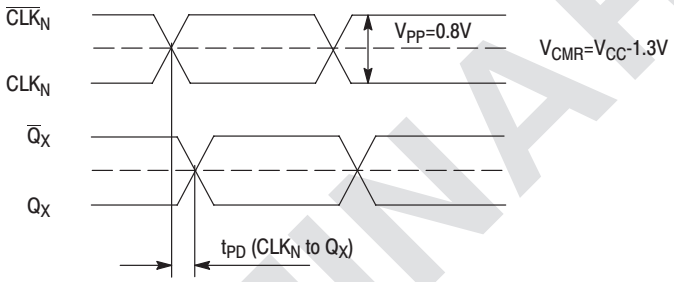


**Figure 4. MC100ES6221 AC reference measurement waveform**



6

## APPLICATIONS INFORMATION

### Using the thermally enhanced package of the MC100ES6221

The MC100ES6221 uses a thermally enhanced exposed pad (EP) 52 lead LQFP package. The package is molded so that the leadframe is exposed at the surface of the package bottom side. The exposed metal pad will provide the low thermal impedance that supports the power consumption of the MC100ES6221 high-speed bipolar integrated circuit and eases the power management task for the system design. A thermal land pattern on the printed circuit board and thermal vias are recommended in order to take advantage of the enhanced thermal capabilities of the MC100ES6221. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal path. In multilayer board designs, thermal vias thermally connect the exposed pad to internal copper planes. Number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package. A nine thermal via array, arranged in a 3 x 3 array and using a 1.2 mm pitch in the center of the thermal land is the absolute minimum requirement for MC100ES6221 applications on multi-layer boards. The recommended thermal land design comprises a 5 x 5 thermal via array as shown in Figure 5 “Recommended thermal land pattern”, providing an efficient heat removal path.

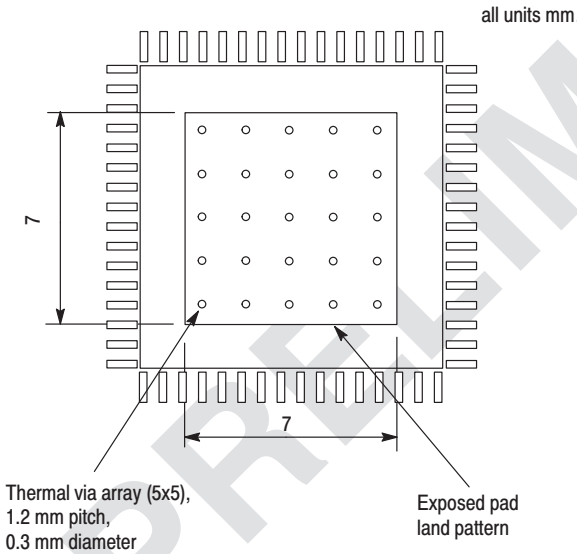


**Figure 5. Recommended thermal land pattern**

The via diameter is should be approx. 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via resulting in voids during the solder process must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for exposed pad package is equivalent to standard surface mount packages. Figure 6 “Recommended solder mask openings” shows a recommend solder mask opening with respect to the recommended 5 x 5 thermal via array. Because a large solder mask opening may result in a poor release, the opening should be subdivided as shown in Figure 6 For the nominal package standoff 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

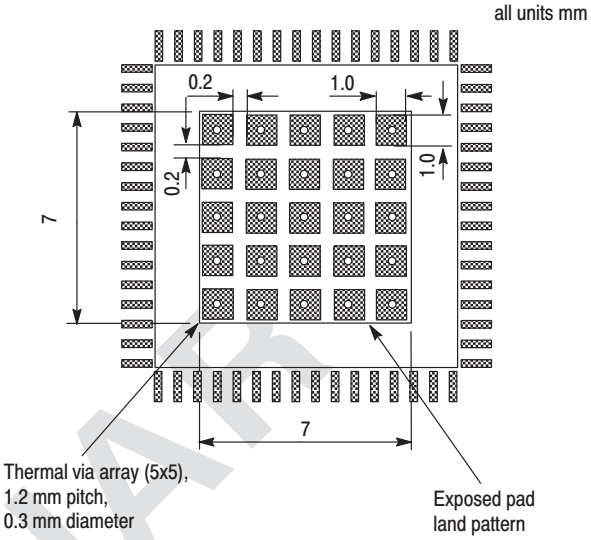


**Figure 6. Recommended solder mask openings**

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided. For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

**Table 8. Thermal Resistance[a]**

| Convection-LFPM | $R_{THJA}$[b] °C/W | $R_{THJA}$[c] °C/W | $R_{THJC}$[d] °C/W | $R_{THJB}$[e] °C/W |
|---|---|---|---|---|
| Natural | 57.1 | 24.9 | 15.8 | 9.7 |
| 100 | 50.0 | 21.3 | | |
| 200 | 46.9 | 20.0 | | |
| 400 | 43.4 | 18.7 | | |
| 800 | 38.6 | 16.9 | | |

a. Thermal data pattern with a 3 x 3 thermal via array on 2S2P boards (based on empirical results)
b. Junction to ambient, single layer test board, per JESD51-6
c. Junction to ambient, four conductor layer test board (2S2P), per JES51-6
d. Junction to case, per MIL-SPEC 883E, method 1012.1
e. Junction to board, four conductor layer test board (2S2P) per JESD 51-8

It is recommended that users employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100ES6221 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals. The thermal land should be connected to GND through connection of internal board layers.

**Order Number: MC100ES6222/D**
**Rev 0, 11/2001**

*Preliminary Information*

# Low Voltage 1:15 Differential ECL/PECL Clock Divider and Fanout Buffer

**MC100ES6222**

**LOW–VOLTAGE 1:15 DIFFERENTIAL ECL/PECL CLOCK DIVIDER AND FANOUT DRIVER**

**TB SUFFIX**
52–LEAD LQFP PACKAGE
EXPOSED PAD
CASE 1336

The Motorola MC100ES6222 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6222 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver is high performance clock distribution in computing, networking and telecommunication systems.

**Features**

- 15 differential ECL/PECL outputs (4 output banks)
- 2 selectable differential ECL/PECL inputs
- Selectable ÷1 or ÷2 frequency divider
- 35 ps maximum device skew[1]
- Supports DC to 3 GHz input frequency[1]
- Single 3.3V, -3.3V, 2.5V or -2.5V supply
- Standard 52 lead LQFP package with exposed pad for enhanced thermal characteristics
- Supports industrial temperature range
- Pin and function compatible to the MC100EP222

**Functional Description**

The MC100ES6222 is designed for low skew clock distribution systems and supports clock frequencies up to 3 GHz[1].The device consists of two independent clock fanout buffers. The CLK0 and CLK1 inputs can be driven by ECL or PECL compatible signals. Each of the four output banks of two, three, four and six differential clock output pairs can be independently configured to distribute the input frequency or ÷2 of the input frequency. The FSELA, FSELB, FSELC, FSELD and CLK_SEL are asychronous control inputs. Any changes of the control inputs require a MR pulse for resynchronization of the the ÷2 outputs. For the functionality of the MR control input, see Figure 5, “Functional Diagram,” on page 609.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all ten outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The MC100ES6222 can be operated from a single 3.3V or 2.5V supply. As most other ECL compatible devices, the MC100ES6222 supports positive (PECL) and negative (ECL) supplies. The MC100ES6222 is pin and function compatible to the MC100EP222.



6

1. AC specifications are design targets and subject to change



**Rev 0**

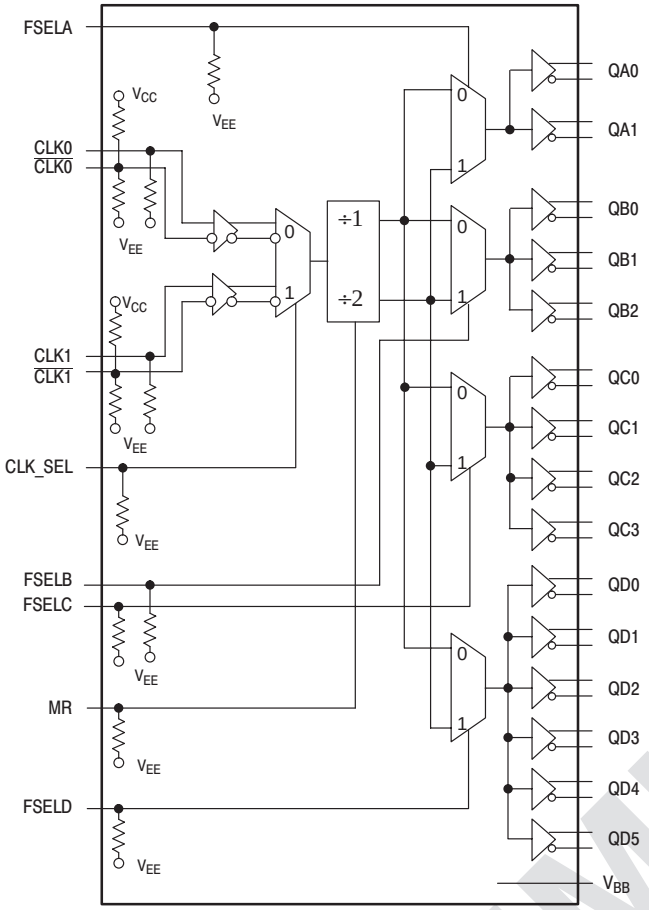


**Figure 1. MC100ES6222 Logic Diagram**

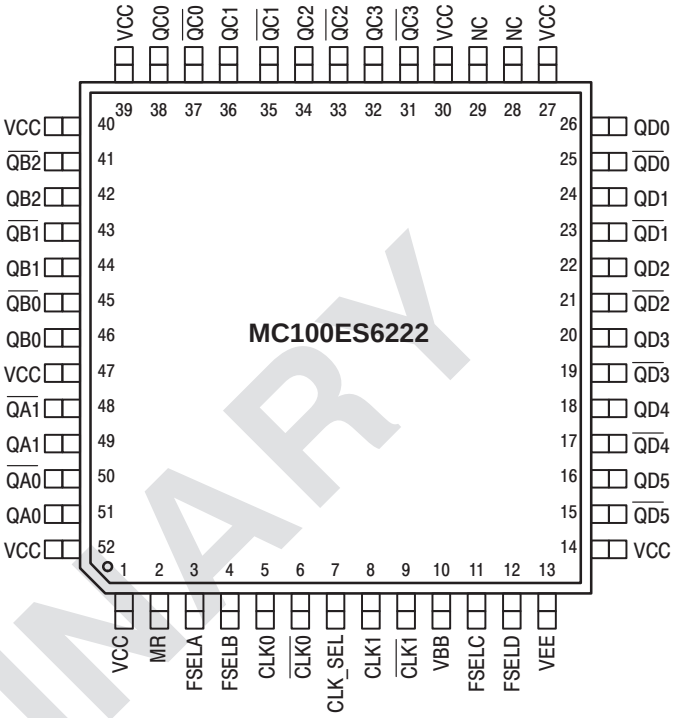


**Figure 2. 52–Lead Package Pinout** (Top View)

**Table 1. Function Table**

| Control Pin | 0 | 1 |
|---|---|---|
| FSELA (asynchronous) | ÷1 | ÷2 |
| FSELB (asynchronous) | ÷1 | ÷2 |
| FSELC (asynchronous) | ÷1 | ÷2 |
| FSELD (asynchronous) | ÷1 | ÷2 |
| CLK_SEL (asynchronous) | CLK0 | CLK1 |
| MR (asynchronous) | Active | Reset. $Q_X$ = L and $\overline{Q}_X$ = H. |

**Table 2. Pin Configuration**

| Pin | I/O | Type | Description |
|---|---|---|---|
| CLK0, $\overline{CLK0}$ | Input | ECL/PECL | Differential reference clock signal input |
| CLK1, $\overline{CLK1}$ | Input | ECL/PECL | Alternative differential reference clock signal input |
| FSELA, FSELB, FSELC, FSELD | Input | ECL/PECL | Selection output frequency divider for bank A, B, C and D |
| MR | Input | ECL/PECL | Reset |
| CLK_SEL | Input | ECL/PECL | Clock reference select input |
| QA[0:1], $\overline{QA[0:1]}$ | Output | ECL/PECL | Bank A differential outputs |
| QB[0:2], $\overline{QB[0:2]}$ | Output | ECL/PECL | Bank B differential outputs |
| QC[0:3], $\overline{QC[0:3]}$ | Output | ECL/PECL | Bank C differential outputs |
| QD[0:5], $\overline{QD[0:5]}$ | Output | ECL/PECL | Bank D differential outputs |
| VBB | Output | DC | Reference voltage output for single ended ECL or PECL operation |
| VEE[a] | | Power supply | Negative power supply |
| VCC | | Power supply | Positive power supply. All $V_{CC}$ pins must be connected to the positive power supply for correct DC and AC operation. |

a. In ECL mode (negative power supply mode), $V_{EE}$ is either -3.3V or -2.5V and $V_{CC}$ is connected to GND (0V). In PECL mode (positive power supply mode), $V_{EE}$ is connected to GND (0V) and $V_{CC}$ is either +3.3V or +2.5V. In both modes, the input and output levels are referenced to the most positive supply ($V_{CC}$).

**Table 3. Absolute Maximum Ratings[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -65 | 125 | °C | |

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 4. General Specifications**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output termination voltage | | $V_{CC}$ - 2[a] | | V | |
| MM | ESD Protection (Machine model) | 200 | | | V | |
| HBM | ESD Protection (Human body model) | 2000 | | | V | |
| CDM | ESD Protection (Charged device model | TBD | | | V | |
| LU | Latch-up immunity | 200 | | | mA | |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | Inputs |
| $\theta_{JA}$, $\theta_{JC}$ $\theta_{JB}$ | Thermal resistance (junction-to-ambient, junction-to-board, junction-to-case) | See Table 8, “Thermal Resistance” | | | °C/W | |
| $T_J$ | Operating junction temperature[b] (continuous operation) MTBF = 9.1 years | 0 | | 110 | °C | |

a. Output termination voltage $V_{TT}$ = 0V for $V_{CC}$ = 2.5V operation is supported but the power consumption of the device will increase.
b. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6222 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6222 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

**Table 5. PECL DC Characteristics** ($V_{CC}$ = 2.5V ± 5% or $V_{CC}$ = 3.3V ± 5%, $V_{EE}$ = GND, $T_J$ = 0°C to +110°C)[a]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Clock input pair CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$ (PECL differential signals) | | | | | | |
| $V_{PP}$ | Differential input voltage[b] | 0.1 | | 1.3 | V | Differential operation |
| $V_{CMR}$ | Differential cross point voltage[c] | 1.0 | | $V_{CC}$ - 0.3 | V | Differential operation |
| $I_{IN}$ | Input Current[a] | | | ±150 | µA | $V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$ |
| Clock inputs MR, CLK_SEL, FSELA, FSELB, FSELC, FSELD (PECL single ended signals) | | | | | | |
| $V_{IL}$ | Input voltage low | | | $V_{CC}$ - 1.46 | V | |
| $V_{IH}$ | Input voltage high | $V_{CC}$ - 1.14 | | | V | |
| $I_{IN}$ | Input Current[d] | | | ±150 | µA | $V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$ |
| PECL clock outputs (QA[0:1], $\overline{QA[0:1]}$, QB[0:2], $\overline{QB[0:2]}$, QC[0:3], $\overline{QC[0:3]}$, QD[0:5], $\overline{QD[0:5]}$ | | | | | | |
| $V_{OH}$ | Output High Voltage | TBD | $V_{CC}$ - 1.005 | TBD | V | Termination 50Ω to $V_{TT}$ |
| $V_{OL}$ | Output Low Voltage | TBD | $V_{CC}$ - 1.705 | TBD | V | Termination 50Ω to $V_{TT}$ |
| Supply current and $V_{BB}$ | | | | | | |
| $I_{EE}$ | Maximum Quiescent Supply Current without output termination current | | TBD | 190 | mA | $V_{EE}$ pins |
| $I_{CC}$[e] | Maximum Quiescent Supply Current, outputs terminated 50Ω to $V_{TT}$ | | TBD | 675 | mA | $V_{CC}$ pins |
| $V_{BB}$ | Output reference voltage | $V_{CC}$ - 1.36 | | $V_{CC}$ - 1.24 | V | $I_{BB}$ = 0.4 mA |

a. DC characteristics are design targets and pending characterization.
b. $V_{PP}$ (DC) is the minimum differential input voltage swing required to maintain device functionality.
c. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.
d. Input have internal pullup/pulldown resistors which affect the input current.
e. $I_{CC}$ includes current through the output resistors (all outputs terminated to $V_{TT}$).

**Table 6. ECL DC Characteristics** ($V_{EE}$ = -2.5V ± 5% or $V_{EE}$ = -3.3V ± 5%, $V_{CC}$ = GND, $T_J$ = $T_J$ = 0°C to +110°C)[a]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Clock input pair CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$ (ECL differential signals) | | | | | | |
| $V_{PP}$ | Differential input voltage[b] | 0.1 | | 1.3 | V | Differential operation |
| $V_{CMR}$ | Differential cross point voltage[c] | $V_{EE}$ + 1.0 | | -0.3 | V | Differential operation |
| $I_{IN}$ | Input Current[a] | | | ±150 | µA | $V_{IN}$ = $V_{IL}$ or $V_{IN}$ = $V_{IH}$ |
| Clock inputs MR, CLK_SEL, FSELA, FSELB, FSELC, FSELD (PECL single ended signals) | | | | | | |
| $V_{IL}$ | Input voltage low | | | -1.46 | V | |
| $V_{IH}$ | Input voltage high | -1.14 | | | V | |
| $I_{IN}$ | Input Current[d] | | | ±150 | µA | $V_{IN}$ = $V_{IL}$ or $V_{IN}$ = $V_{IH}$ |
| ECL clock outputs (QA[0:1], $\overline{QA[0:1]}$, QB[0:2], $\overline{QB[0:2]}$, QC[0:3], $\overline{QC[0:3]}$, QD[0:5], $\overline{QD[0:5]}$ | | | | | | |
| $V_{OH}$ | Output High Voltage | TBD | -1.005 | TBD | V | Termination 50Ω to $V_{TT}$ |
| $V_{OL}$ | Output Low Voltage | TBD | -1.705 | TBD | V | Termination 50Ω to $V_{TT}$ |
| Supply current and $V_{BB}$ | | | | | | |
| $I_{EE}$ | Maximum Quiescent Supply Current without output termination current | | TBD | 190 | mA | $V_{EE}$ pins |
| $I_{CC}$[e] | Maximum Quiescent Supply Current, outputs terminated 50Ω to $V_{TT}$ | | TBD | 750 | mA | $V_{CC}$ pins |
| $V_{BB}$ | Output reference voltage | -1.36 | | -1.24 | V | $I_{BB}$ = 0.4 mA |

a. DC characteristics are design targets and pending characterization.
b. $V_{PP}$ (DC) is the minimum differential input voltage swing required to maintain device functionality.
c. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.
d. Input have internal pullup/pulldown resistors which affect the input current.
e. $I_{CC}$ includes current through the output resistors (all outputs terminated to $V_{TT}$).

**Table 7. AC Characteristics** (ECL: $V_{EE}$ = -3.3V ± 5% or $V_{EE}$ = -2.5V ± 5%, $V_{CC}$ = GND) or (PECL: $V_{CC}$ = 3.3V ± 5% or $V_{CC}$ = 2.5V ± 5%, $V_{EE}$ = GND, $T_J$ = 0°C to +110°C)[a b]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Clock input pair CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$ (PECL or ECL differential signals) | | | | | | |
| $V_{PP}$ | Differential input voltage[c] (peak-to-peak) | TBD | 0.3 | 1.3 | V | |
| $V_{CMR}$ | Differential input crosspoint voltage[d] PECL<br>ECL | TBD<br>TBD | | $V_{CC}$ - 0.3<br>-0.3V | V<br>V | |
| $f_{CLK}$ | Input Frequency | | 0 - 3000 | TBD | MHz | Differential |
| ECL/PECL clock outputs (QA[0:1], $\overline{QA[0:1]}$, QB[0:2], $\overline{QB[0:2]}$, QC[0:3], $\overline{QC[0:3]}$, QD[0:5], $\overline{QD[0:5]}$ | | | | | | |
| $t_{PD}$ | Propagation Delay $CLK_N$ to Qx<br>MR to Qx | | 500 | TBD | ps<br>ps | Differential |
| $V_{O(P-P)}$ | Differential output voltage (peak-to-peak)<br>$f_O$ < 1.1 GHz<br>$f_O$ < 2.5 GHz<br>$f_O$ < 3.0 GHz | <br>TBD<br>TBD<br>TBD | <br>0.8<br>0.6 | | <br>V<br>V<br>V | |
| $t_{sk(O)}$ | Output-to-output skew | | | 5 | ps | Differential |
| $t_{sk(PP)}$ | Output-to-output skew (part-to-part) | | | TBD | ps | Differential |
| $t_{JIT(CC)}$ | Output cycle-to-cycle jitter | | | | | |
| $DC_O$ | Output duty cycle | TBD | 50 | TBD | % | $DC_{fref}$ = 50% |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.05 | | TBD | ns | 20% to 80% |

a. AC characteristics are design targets and pending characterization.
b. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
c. $V_{PP}$ (AC) is the minimum differential ECL/PECL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
d. $V_{CMR}$ (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ (AC) range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ (AC) or $V_{PP}$ (AC) impacts the device propagation delay, device and part-to-part skew.

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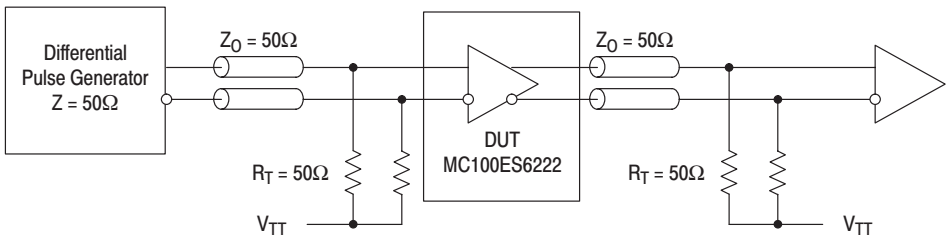


**Figure 3. MC100ES6222 AC test reference**

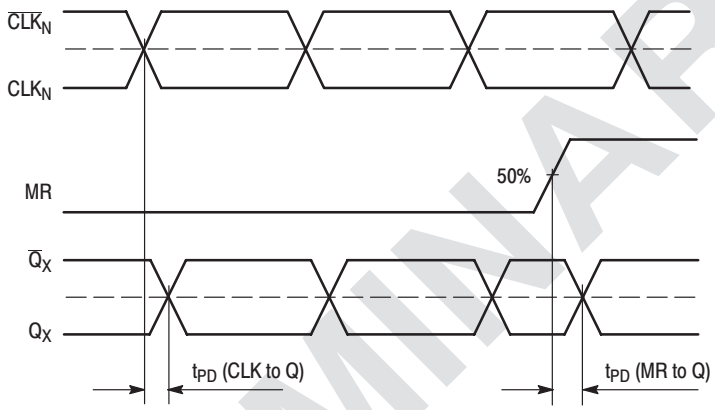


**Figure 4. MC100ES6222 $t_{PD}$ measurement waveform**



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## APPLICATIONS INFORMATION

### Asynchronous Reset Functional Diagram

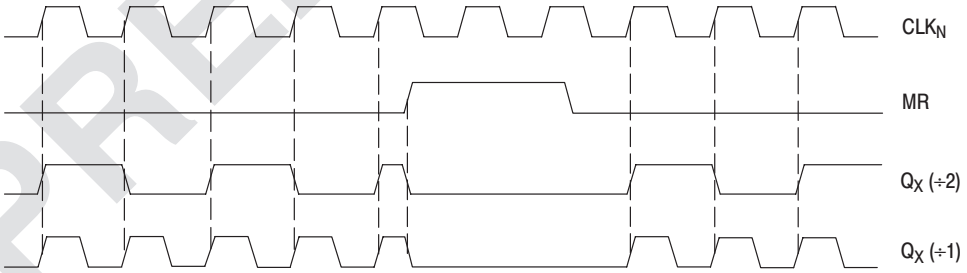


**Figure 5. Functional diagram**

## APPLICATIONS INFORMATION

### Using the thermally enhanced package of the MC100ES6222

The MC100ES6222 uses a thermally enhanced exposed pad (EP) 52 lead LQFP package. The package is molded so that the leadframe is exposed at the surface of the package bottom side. The exposed metal pad will provide the low thermal impedance that supports the power consumption of the MC100ES6222 high-speed bipolar integrated circuit and eases the power management task for the system design. A thermal land pattern on the printed circuit board and thermal vias are recommended in order to take advantage of the enhanced thermal capabilities of the MC100ES6222. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal path. In multilayer board designs, thermal vias thermally connect the exposed pad to internal copper planes. Number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package. A nine thermal via array, arranged in a 3 x 3 array and using a 1.2 mm pitch in the center of the thermal land is the absolute minimum requirement for MC100ES6222 applications on multi-layer boards. The recommended thermal land design comprises a 5 x 5 thermal via array as shown in Figure 6 “Recommended thermal land pattern”, providing an efficient heat removal path.

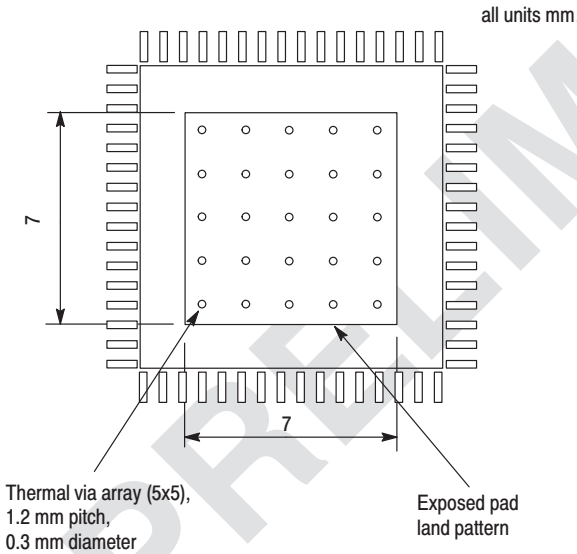


**Figure 6. Recommended thermal land pattern**

The via diameter is should be approx. 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via resulting in voids during the solder process must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for exposed pad package is equivalent to standard surface mount packages. Figure 7 “Recommended solder mask openings” shows a recommend solder mask opening with respect to the recommended 5 x 5 thermal via array. Because a large solder mask opening may result in a poor release, the opening should be subdivided as shown in Figure 7 For the nominal package standoff 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

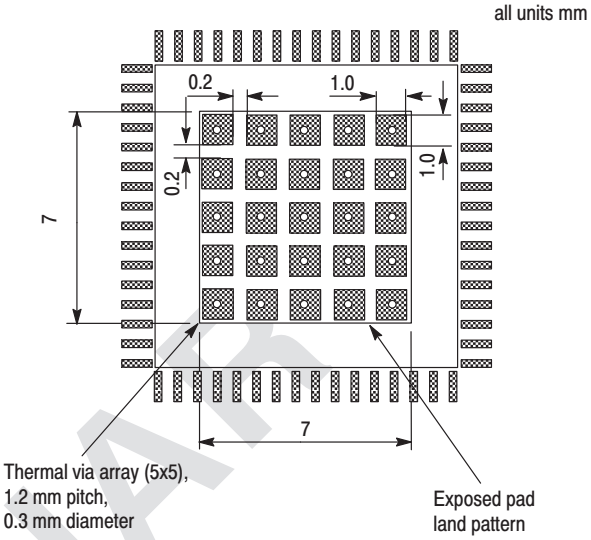


**Figure 7. Recommended solder mask openings**

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided. For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

**Table 8. Thermal Resistance[a]**

| Convection-LFPM | $R_{THJA}$[b] °C/W | $R_{THJA}$[c] °C/W | $R_{THJC}$[d] °C/W | $R_{THJB}$[e] °C/W |
|---|---|---|---|---|
| Natural | 57.1 | 24.9 | 15.8 | 9.7 |
| 100 | 50.0 | 21.3 | | |
| 200 | 46.9 | 20.0 | | |
| 400 | 43.4 | 18.7 | | |
| 800 | 38.6 | 16.9 | | |

a. Thermal data pattern with a 3 x 3 thermal via array on 2S2P boards (based on empirical results)
b. Junction to ambient, single layer test board, per JESD51-6
c. Junction to ambient, four conductor layer test board (2S2P), per JES51-6
d. Junction to case, per MIL-SPEC 883E, method 1012.1
e. Junction to board, four conductor layer test board (2S2P) per JESD 51-8

It is recommended that users employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100ES6222 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals. The thermal land should be connected to GND through connection of internal board layers.

**Order Number: MC100ES6226/D**
**Rev 1, 12/2001**

# 2.5/3.3V Differential LVPECL 1:9 Clock Distribution Buffer and Clock Divider

**MC100ES6226**

**2.5V/3.3V DIFFERENTIAL LVPECL 1:9 CLOCK DISTRIBUTION BUFFER AND CLOCK DIVIDER**

The Motorola MC100ES6226 is a bipolar monolithic differential clock distribution buffer and clock divider. Designed for most demanding clock distribution systems, the MC100ES6226 supports various applications that require a large number of outputs to drive precisely aligned clock signals. Using SiGe technology and a fully differential architecture, the device offers superior digitial signal characteristics and very low clock skew error. Target applications for this clock driver are high performance clock distribution systems for computing, networking and telecommunication systems.

**Features:**

- Fully differential architecture from input to all outputs
- SiGe technology supports near-zero output skew
- Selectable 1:1 or 1:2 frequency outputs
- LVPECL compatible differential clock inputs and outputs
- LVCMOS compatible control inputs
- Single 3.3V or 2.5V supply
- Max. 35 ps maximum output skew (within output bank)
- Max. 50 ps maximum device skew
- Supports DC operation and up to 3 GHz (typ.) clock signals
- Synchronous output enable eliminating output runt pulse generation and metastability
- Standard 32 lead LQFP package
- Industrial temperature range

**FA SUFFIX**
32–LEAD LQFP PACKAGE
CASE 873A

6

**Functional Description**

MC100ES6226 is designed for very skew critical differential clock distribution systems and supports clock frequencies from DC up to 3.0 GHz. Typical applications for the MC100ES6226 are primary clock distribution systems on backplanes of high-performance computer, networking and telecommunication systems, as well as on-board clocking of OC-3, OC-12 and OC-48 speed communication systems.

The MC100ES6226 can be operated from a 3.3V or 2.5V positive supply without the requirement of a negative supply line. Each of the output banks of three differential clock output pairs may be independently configured to distribute the input frequency or half of the input frequency. The FSEL0 and FSEL1 clock frequency selects are asychronous control inputs. Any changes of the control inputs require a MR pulse for resynchronization of the ÷2 outputs.

**Rev 1**

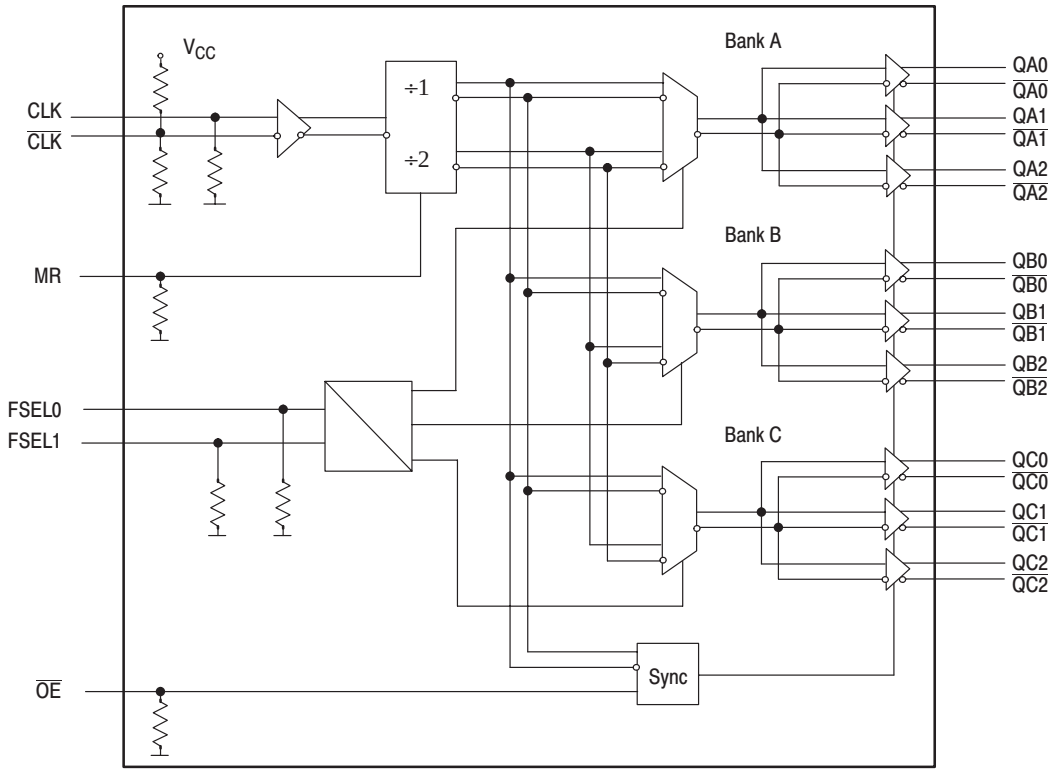


**Figure 1. MC100ES6226 Logic Diagram**

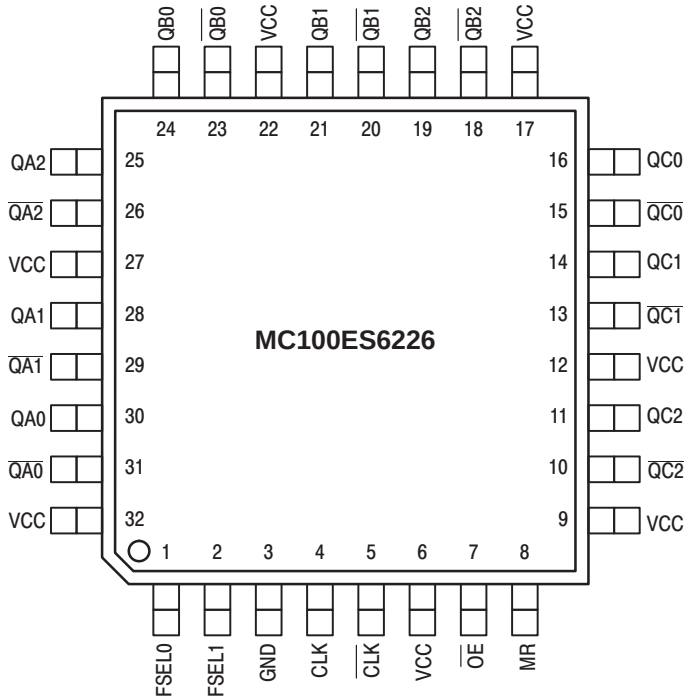


**Figure 2. 32–Lead Package Pinout** (Top View)

**TABLE 1: PIN CONFIGURATION**

| Pin | I/O | Type | Function |
|---|---|---|---|
| CLK, $\overline{CLK}$ | Input | LVPECL | Differential reference clock signal input |
| $\overline{OE}$ | Input | LVCMOS | Output enable |
| MR | Input | LVCMOS | Device reset |
| FSEL0, FSEL1 | Input | LVCMOS | Output frequency divider select |
| QA[0-2], $\overline{QA[0\text{-}2]}$<br>QB[0-2], $\overline{QB[0\text{-}2]}$<br>QC[0-2], $\overline{QC[0\text{-}2]}$ | Output | LVPECL | Differential clock outputs (banks A, B and C) |
| GND | Supply | GND | Negative power supply |
| $V_{CC}$ | Supply | VCC | Positive power supply. All $V_{CC}$ pins must be connected to the positive power supply for correct DC and AC operation |

**TABLE 2: FUNCTION TABLE**

| Control | Default | 0 | 1 |
|---|---|---|---|
| $\overline{OE}$ | 0 | Qx[0-2], $\overline{Qx[0\text{-}2]}$ are active. Deassertion of $\overline{OE}$ can be asynchronous to the reference clock without generation of output runt pulses | Qx[0-2] = L, $\overline{Qx[0\text{-}2]}$ =H (outputs disabled). Assertion of $\overline{OE}$ can be asynchronous to the reference clock without generation of output runt pulses |
| MR | 0 | Normal operation | Device reset (asynchronous) |
| FSEL0, FSEL1 | 00 | See Following Table | |

**TABLE 3: Output Frequency Select Control**

| FSEL0 | FSEL1 | QA0 to QA2 | QB0 to QB2 | QC0 to QC2 |
|---|---|---|---|---|
| 0 | 0 | $f_{QA0:2} = f_{CLK}$ | $f_{QB0:2} = f_{CLK}$ | $f_{QC0:2} = f_{CLK}$ |
| 0 | 1 | $f_{QA0:2} = f_{CLK}$ | $f_{QB0:2} = f_{CLK}$ | $f_{QC0:2} = f_{CLK} \div 2$ |
| 1 | 0 | $f_{QA0:2} = f_{CLK}$ | $f_{QB0:2} = f_{CLK} \div 2$ | $f_{QC0:2} = f_{CLK} \div 2$ |
| 1 | 1 | $f_{QA0:2} = f_{CLK} \div 2$ | $f_{QB0:2} = f_{CLK} \div 2$ | $f_{QC0:2} = f_{CLK} \div 2$ |

**TABLE 4: ABSOLUTE MAXIMUM RATINGS[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -65 | 125 | °C | |

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

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**TABLE 5: GENERAL SPECIFICATIONS**

| Sym-bol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output termination voltage | | $V_{CC}$ - 2[a] | | V | |
| MM | ESD Protection (Machine model) | 200 | | | V | |
| HBM | ESD Protection (Human body model) | 2000 | | | V | |
| CDM | ESD Protection (Charged device model) | 1000 | | | V | |
| LU | Latch-up immunity | 200 | | | mA | |
| $C_{IN}$ | | | 4.0 | | pF | Inputs |
| $\theta_{JA}$ | Thermal resistance junction to ambient | | | | | |
| | JESD 51-3, single layer test board | | 83.1 | 86.0 | °C/W | Natural convection |
| | | | 73.3 | 75.4 | °C/W | 100 ft/min |
| | | | 68.9 | 70.9 | °C/W | 200 ft/min |
| | | | 63.8 | 65.3 | °C/W | 400 ft/min |
| | | | 57.4 | 59.6 | °C/W | 800 ft/min |
| | JESD 51-6, 2S2P multilayer test board | | 59.0 | 60.6 | °C/W | Natural convection |
| | | | 54.4 | 55.7 | °C/W | 100 ft/min |
| | | | 52.5 | 53.8 | °C/W | 200 ft/min |
| | | | 50.4 | 51.5 | °C/W | 400 ft/min |
| | | | 47.8 | 48.8 | °C/W | 800 ft/min |
| $\theta_{JC}$ | Thermal resistance junction to case | | 23.0 | 26.3 | °C/W | MIL-SPEC 883E Method 1012.1 |
| | Operating junction temperature[b] (continuous operation) MTBF = 9.1 years | 0 | | 110 | °C | |

a. Output termination voltage $V_{TT}$ = 0V for $V_{CC}$ = 2.5V operation is supported but the power consumption of the device will increase.

b. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6226 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6226 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

**TABLE 6: DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5% and 2.5V ± 5%, $T_J$ = 0°C to +110°C)[a]

| Sym-bol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| LVCMOS control inputs ($\overline{OE}$, FSEL0, FSEL1, MR) | | | | | | | |
| $V_{IL}$ | Input voltage low | $V_{CC}$ = 3.3 V<br>$V_{CC}$ = 2.5 V | | | 0.8<br>0.7 | V | |
| $V_{IH}$ | Input voltage high | $V_{CC}$ = 3.3 V<br>$V_{CC}$ = 2.5 V | 2.2<br>1.7 | | | V | |
| $I_{IN}$ | Input Current[b] | | | | ±150 | µA | $V_{IN}$ = $V_{CC}$ or $V_{IN}$ = GND |
| LVPECL clock inputs (CLK, $\overline{CLK}$)[c] | | | | | | | |
| $V_{PP}$ | DC differential input voltage[d] | | 0.1 | | 1.3 | V | Differential operation |
| $V_{CMR}$ | Differential cross point voltage[e] | | 1.0 | | $V_{CC}$-0.3 | V | Differential operation |
| $V_{IH}$ | Input high voltage | | TBD | | TBD | | |
| $V_{IL}$ | Input low voltage | | TBD | | TBD | | |
| $I_{IN}$ | Input Current | | | | ±150 | µA | $V_{IN}$ = TBD or $V_{IN}$ = TBD |
| LVPECL clock outputs (QA[2:0], QB[2:0], QC[2:0]) | | | | | | | |
| $V_{OH}$ | Output High Voltage | | $V_{CC}$-1.1 | | $V_{CC}$-0.8 | V | Termination 50Ω to $V_{TT}$ |
| $V_{OL}$ | Output Low Voltage | | $V_{CC}$-1.8 | | $V_{CC}$-1.4 | V | Termination 50Ω to $V_{TT}$ |
| Supply current | | | | | | | |
| $I_{GND}$ | Maximum Quiescent Supply Current without output termination current | | | 65 | 110 | mA | GND pin |
| $I_{CC}$ | Maximum Quiescent Supply Current with output termination current | | | 325 | 400 | mA | All $V_{CC}$ Pins |

a. AC characterisitics are design targets and pending characterization.
b. Input have internal pullup/pulldown resistors which affect the input current.
c. Clock inputs driven by LVPECL compatible signals.
d. $V_{PP}$ is the minimum differential input voltage swing required to maintain AC characteristic.
e. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.

**TABLE 7: AC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5% and 2.5V ± 5%, $T_J$ = 0°C to +110°C)[a b]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{PP}$ | Differential input voltage[c] (peak-to-peak) | 0.2 | 0.3 | 1.3 | V | |
| $V_{CMR}$ | Differential input crosspoint voltage[d] | 1.0 | | $V_{CC}$-0.3 | V | |
| $V_{X,OUT}$ | Differential output crosspoint voltage | $V_{CC}$-1.45 | | $V_{CC}$-1.1 | V | |
| $V_{O(P-P)}$ | Differential output voltage (peak-to-peak)<br>$f_O$ < 300 MHz<br>$f_O$ < 1.5 GHz<br>$f_O$ < 2.7 GHz | <br>0.45<br>0.3<br>TBD | <br>0.72<br>0.55<br>0.37 | <br>0.95<br>0.95<br>0.95 | <br>V<br>V<br>V | |
| $f_{CLK}$ | Input Frequency | 0 | | 3000[e] | MHz | |
| $t_{PD}$ | Propagation Delay CLK to Qx[] | 475 | 500 | 800 | ps | Differential |
| $t_{sk(O)}$ | Output-to-output skew (within QA[2:0])<br>(within QB[2:0])<br>(within QC[2:0])<br>(within device) | | <br>11<br>12<br>4 | <br>25<br>25<br>20<br>60 | <br>ps<br>ps<br>ps<br>ps | <br>Differential |
| $t_{sk(PP)}$ | Output-to-output skew (part-to-part) | | | 325 | ps | Differential |
| $t_{JIT(CC)}$ | Output cycle-to-cycle jitter<br>single frequency configuration<br>÷1/÷2 frequency configuration | | | <br>TBD<br>TBD | | <br>FSEL0 = FSEL1<br>FSEL0 ≠ FSEL1 |
| $DC_O$ | Output duty cycle Qx = ÷1, $f_O$ < 300 MHz<br>Qx = ÷1, $f_O$ > 300 MHz<br><br>Qx = ÷2, $f_O$ < 300 MHz<br>Qx = ÷2, $f_O$ > 300 MHz | 48<br>45<br><br>49<br>47.5 | 50<br>50<br><br>50<br>50 | 52<br>55<br><br>51<br>52.5 | %<br>%<br><br>%<br>% | $DC_{fref}$= 50% |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.05 | | 200 | ns | 20% to 80% |
| $t_{PDL}$[f] | Output disable time | 2.5·T + $t_{PD}$ | | 4.5·T + $t_{PD}$ | ns | T=CLK period |
| $t_{PLD}$[g] | Output enable time | 3·T + $t_{PD}$ | | 5·T + $t_{PD}$ | ns | T=CLK period |

a. AC characterisitics are design targets and pending characterization.
b. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
c. $V_{PP}$ is the minimum differential input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
d. $V_{CMR}$ (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ (AC) range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ (AC) or $V_{PP}$ (AC) impacts the device propagation delay, device and part-to-part skew.
e. The MC100ES6226 is fully operational up to 3.0 GHz and is characterized up to 2.7 GHz.
f. Propagation delay $\overline{OE}$ deassertion to differential output disabled (differential low: true output low, complementary output high).
g. Propagation delay $\overline{OE}$ assertion to output enabled (active).

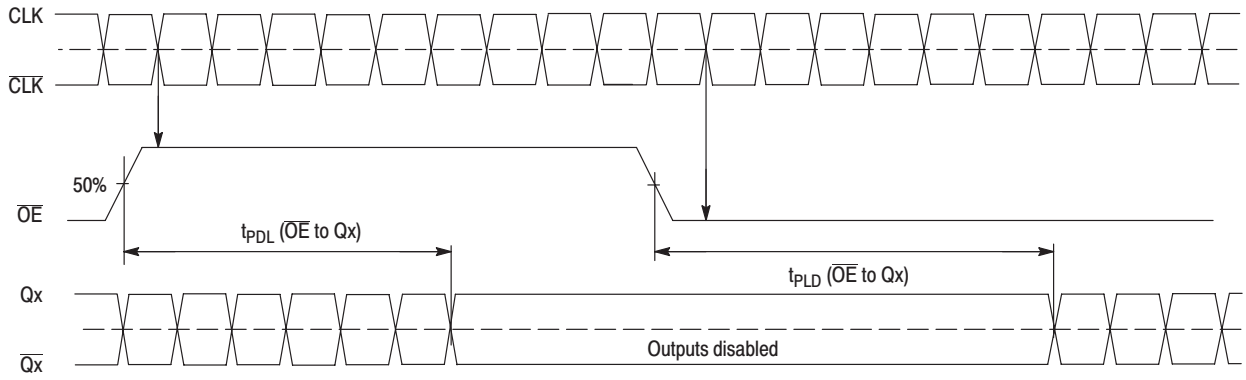


**Figure 3. MC100ES6226 output disable/enable timing**

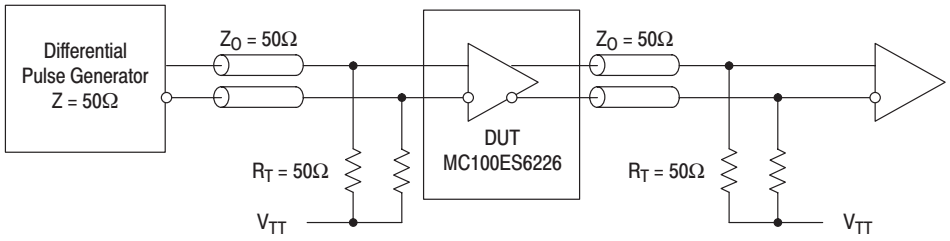


**Figure 4. MC100ES6226 AC test reference**

## APPLICATIONS INFORMATION

### Maintaining Lowest Device Skew

The MC100ES6226 guarantees low output-to-output bank skew of 35 ps and a part-to-part skew of max. TBD ps. To ensure low skew clock signals in the application, both outputs of any differential output pair need to be terminated identically, even if only one output is used. When fewer than all nine output pairs are used, identical termination of all output pairs within the output bank is recommended. If an entire output bank is not used, it is recommended to leave all of these outputs open and unterminated. This will reduce the device power consumption while maintaining minimum output skew.

### Power Supply Bypassing

The MC100ES6226 is a mixed analog/digital product. The differential architecture of the MC100ES6226 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all $V_{CC}$ pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

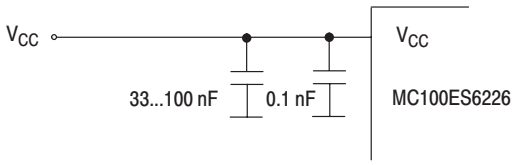


**Figure 5. $V_{CC}$ Power Supply Bypass**

6

*Product Preview*

# 2.5/3.3V Differential LVPECL 2x2 Clock Switch and Fanout Buffer

**MC100ES6254**

**2.5V/3.3V DIFFERENTIAL LVPECL 2x2 CLOCK SWITCH AND FANOUT BUFFER**

**FA SUFFIX**
32–LEAD LQFP PACKAGE
CASE 873A

The Motorola MC100ES6254 is a bipolar monolithic differential 2x2 clock switch and fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6254 supports various applications that require to drive precisely aligned clock signals. The device is capable of driving and switching differential LVPECL signals. Using SiGe technology and a fully differential architecture, the device offers superior digitial signal characteristics and very low clock skew error. Target applications for this clock driver are high performance clock/data switching, clock distribution or data loopback in computing, networking and telecommunication systems.

**Features:**

- Fully differential architecture from input to all outputs
- SiGe technology supports near-zero output skew
- Supports DC to 3GHz operation[1] of clock or data signals
- LVPECL compatible differential clock inputs and outputs
- LVCMOS compatible control inputs
- Single 3.3V or 2.5V supply
- 25 ps maximum output skew (within output bank)[1]
- 35 ps maximum device skew[1]
- Synchronous output enable eliminating output runt pulse generation and metastability
- Standard 32 lead LQFP package
- Industrial temperature range

6

**Functional Description**

MC100ES6254 is designed for very skew critical differential clock distribution systems and supports clock frequencies from DC up to 3.0 GHz. Typical applications for the MC100ES6254 are primary clock distribution, switching and loopback systems of high-performance computer, networking and telecommunication systems, as well as on-board clocking of OC-3, OC-12 and OC-48 speed communication systems. Primary purpose of the MC100ES6254 is high–speed clock switching applications. In addition, the MC100ES6254 can be configured as single 1:6 or dual 1:3 LVPECL fanout buffer for clock signals, or as loopback device in high–speed data applications.

The MC100ES6254 can be operated from a 3.3V or 2.5V positive supply without the requirement of a negative supply line.



1. AC specifications are design targets and subject to change



**Rev 0**

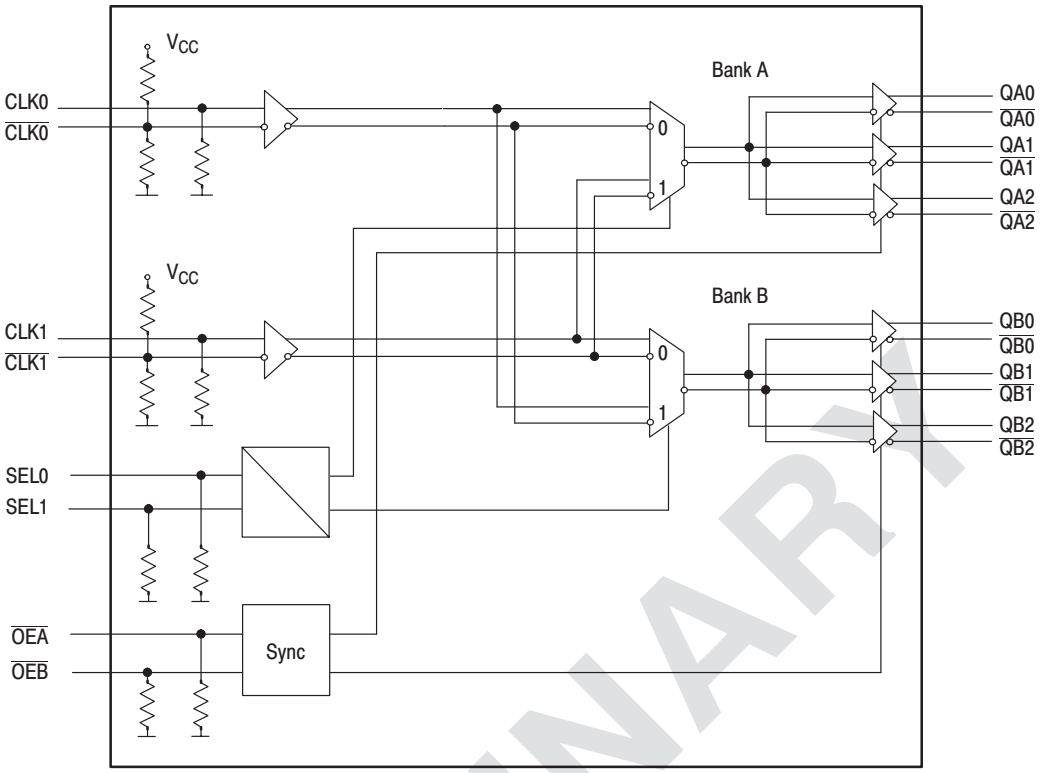


**Figure 1. MC100ES6254 Logic Diagram**

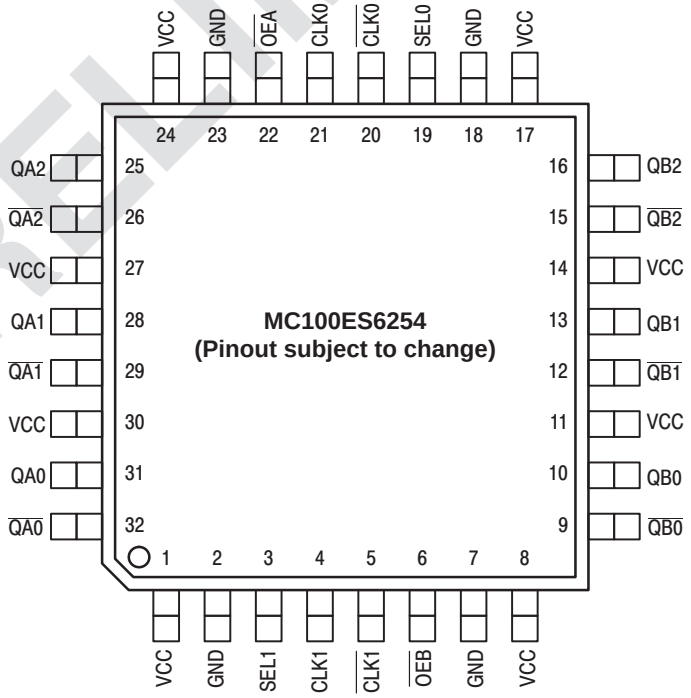


**Figure 2. 32–Lead Package Pinout** (Top View)

**TABLE 1: PIN CONFIGURATION**

| Pin | I/O | Type | Function |
|---|---|---|---|
| CLK0, $\overline{\text{CLK0}}$ | Input | LVPECL | Differential reference clock signal input 0 |
| CLK1, $\overline{\text{CLK1}}$ | Input | LVPECL | Differential reference clock signal input 1 |
| $\overline{\text{OEA}}$, $\overline{\text{OEB}}$ | Input | LVCMOS | Output enable |
| SEL0, SEL1 | Input | LVCMOS | Clock switch select |
| QA[0-2], $\overline{\text{QA[0-2]}}$<br>QB[0-2], $\overline{\text{QB[0-2]}}$ | Output | LVPECL | Differential clock outputs (banks A and B) |
| GND | Supply | GND | Negative power supply |
| $V_{CC}$ | Supply | VCC | Positive power supply. All $V_{CC}$ pins must be connected to the positive power supply for correct DC and AC operation |

**TABLE 2: FUNCTION TABLE**

| Control | Default | 0 | 1 |
|---|---|---|---|
| $\overline{\text{OEA}}$ | 0 | QA[0-2], $\overline{\text{Qx[0-2]}}$ are active. Deassertion of $\overline{\text{OE}}$ can be asynchronous to the reference clock without generation of output runt pulses | QA[0-2] = L, $\overline{\text{QA[0-2]}}$ =H (outputs disabled). Assertion of $\overline{\text{OE}}$ can be asynchronous to the reference clock without generation of output runt pulses |
| $\overline{\text{OEB}}$ | 0 | QA[0-2], $\overline{\text{Qx[0-2]}}$ are active. Deassertion of $\overline{\text{OE}}$ can be asynchronous to the reference clock without generation of output runt pulses | QA[0-2] = L, $\overline{\text{QA[0-2]}}$ =H (outputs disabled). Assertion of $\overline{\text{OE}}$ can be asynchronous to the reference clock without generation of output runt pulses |
| SEL0, SEL1 | 00 | See Following Table | |

**TABLE 3: CLOCK SELECT CONTROL**

| SEL0 | SEL1 | CLK0 routed to | CLK1 routed to | Application Mode |
|---|---|---|---|---|
| 0 | 0 | QA[0:2] and QB[0:2] | —— | 1:6 fanout of CLK0 |
| 0 | 1 | —— | QA[0:2] and QB[0:2] | 1:6 fanout of CLK1 |
| 1 | 0 | QA[0:2] | QB[0:2] | Dual 1:3 buffer |
| 1 | 1 | QB[0:2] | QA[0:2] | Dual 1:3 buffer (crossed) |

**TABLE 4: ABSOLUTE MAXIMUM RATINGS[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$+0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -65 | 125 | °C | |

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**TABLE 5: GENERAL SPECIFICATIONS**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output termination voltage | | $V_{CC}$ - 2[a] | | V | |
| MM | ESD Protection (Machine model) | TBD | | | V | |
| HBM | ESD Protection (Human body model) | TBD | | | V | |
| CDM | ESD Protection (Charged device model) | TBD | | | V | |
| LU | Latch-up immunity | 200 | | | mA | |
| $C_{IN}$ | | | 4.0 | | pF | Inputs |
| $\theta_{JA}$ | Thermal resistance junction to ambient | | | | | |
| | JESD 51-3, single layer test board | | 83.1 | 86.0 | °C/W | Natural convection |
| | | | 73.3 | 75.4 | °C/W | 100 ft/min |
| | | | 68.9 | 70.9 | °C/W | 200 ft/min |
| | | | 63.8 | 65.3 | °C/W | 400 ft/min |
| | | | 57.4 | 59.6 | °C/W | 800 ft/min |
| | JESD 51-6, 2S2P multilayer test board | | 59.0 | 60.6 | °C/W | Natural convection |
| | | | 54.4 | 55.7 | °C/W | 100 ft/min |
| | | | 52.5 | 53.8 | °C/W | 200 ft/min |
| | | | 50.4 | 51.5 | °C/W | 400 ft/min |
| | | | 47.8 | 48.8 | °C/W | 800 ft/min |
| $\theta_{JC}$ | Thermal resistance junction to case | | 23.0 | 26.3 | °C/W | MIL-SPEC 883E Method 1012.1 |
| | Operating junction temperature[b] (continuous operation) MTBF = 9.1 years | | | 110 | °C | |

a. Output termination voltage $V_{TT}$ = 0V for $V_{CC}$=2.5V operation is supported but the power consumption of the device will increase.

b. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6254 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6254 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

**TABLE 6: DC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5% or 2.5V ± 5%, $T_J$ = 0° to +110°C)[a]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| LVCMOS control inputs ($\overline{OEA}$, $\overline{OEB}$, SEL0, SEL1) | | | | | | |
| $V_{IL}$ | Input voltage low | | | 0.8 | V | |
| $V_{IH}$ | Input voltage high | 2.0 | | | V | |
| $I_{IN}$ | Input Current[b] | | | ±TBD | µA | $V_{IN}$ = $V_{CC}$ or $V_{IN}$ = GND |
| LVPECL clock inputs (CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$)[c] | | | | | | |
| $V_{PP}$ | AC differential input voltage[d] | 0.1 | | 1.3 | V | Differential operation |
| $V_{CMR}$ | Differential cross point voltage[e] | 1.0 | | $V_{CC}$-0.3 | V | Differential operation |
| $V_{IH}$ | Input high voltage | TBD | | TBD | | |
| $V_{IL}$ | Input low voltage | TBD | | TBD | | |
| $I_{IN}$ | Input Current | | | ±TBD | µA | $V_{IN}$ = TBD or $V_{IN}$ = TBD |
| LVPECL clock outputs (QA0-2, $\overline{QA0-2}$, QB0-2, $\overline{QB0-2}$) | | | | | | |
| $V_{OH}$ | Output High Voltage | TBD | $V_{CC}$-1.005 | TBD | V | Termination 50Ω to $V_{TT}$ |
| $V_{OL}$ | Output Low Voltage | TBD | $V_{CC}$-1.705 | TBD | V | Termination 50Ω to $V_{TT}$ |
| | | | | | | |
| $I_{GND}$ | Maximum Quiescent Supply Current without output termination current | | TBD | TBD | mA | GND pin |
| $I_{CC}$ | Maximum Quiescent Supply Current, outputs terminated 50Ω to $V_{TT}$ | | TBD | TBD | mA | All $V_{CC}$ Pins |

a. AC characterisitics are design targets and pending characterization.
b. Input have internal pullup/pulldown resistors which affect the input current.
c. Clock inputs driven by LVPECL compatible signals.
d. $V_{PP}$ is the minimum differential input voltage swing required to maintain AC characteristic.
e. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.

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**TABLE 7: AC CHARACTERISTICS** ($V_{CC}$ = 3.3V ± 5% or 2.5V ± 5%, $T_J$ = 0° to +110°C)[a b]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{PP}$ | Differential input voltage[c] (peak-to-peak) | | 0.3 | 1.3 | V | |
| $V_{CMR}$ | Differential input crosspoint voltage[d] | | | $V_{CC}$-0.3 | V | |
| $V_{O(P-P)}$ | Differential output voltage (peak-to-peak)<br>$f_O$ < 1.1 GHz<br>$f_O$ < 2.5 GHz<br>$f_O$ < 3.0 GHz | | <br>0.8<br>0.6 | <br>TBD<br>TBD<br>TBD | <br>V<br>V<br>V | |
| $f_{CLK}$ | Input Frequency | | 0-3000 | TBD | MHz | |
| $t_{PD}$ | Propagation Delay CLKX to QA[] or QB[] | | 500 | TBD | ps | Differential |
| $t_{sk(O)}$ | Output-to-output skew (within bank)<br>(within device) | | | 25<br>35 | ps<br>ps | Differential<br>Differential |
| $t_{sk(PP)}$ | Output-to-output skew (part-to-part) | | | TBD | ps | Differential |
| $t_{JIT(CC)}$ | Output cycle-to-cycle jitter (SEL0 = 0) | | | TBD | ps | Differential |
| $DC_O$ | Output duty cycle | TBD | 50 | TBD | % | $DC_{fref}$= 50% |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.05 | | TBD | ns | 20% to 80% |
| $t_{PDL}$[e] | Output disable time | 2.5·T + $t_{PD}$ | | 3.5·T + $t_{PD}$ | ns | T=CLK period |
| $t_{PLD}$[f] | Output enable time | 3·T + $t_{PD}$ | | 4·T + $t_{PD}$ | ns | T=CLK period |

a. AC characterisitics are design targets and pending characterization.
b. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
c. $V_{PP}$ is the minimum differential input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
d. $V_{CMR}$ (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ (AC) range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ (AC) or $V_{PP}$ (AC) impacts the device propagation delay, device and part-to-part skew.
e. Propagation delay $\overline{OE}$ deassertion to differential output disabled (differential low: true output low, complementary output high).
f. Propagation delay $\overline{OE}$ assertion to output enabled (active).

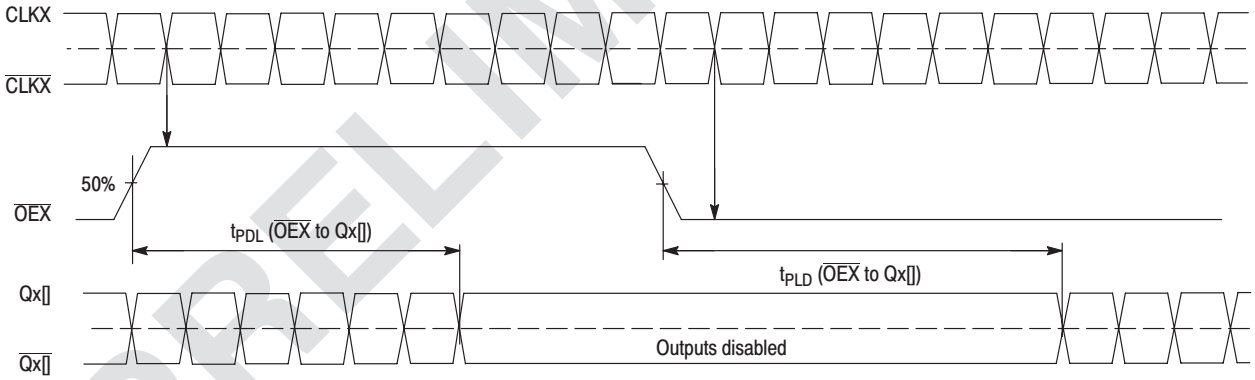



**Figure 3. MC100ES6254 output disable/enable timing**

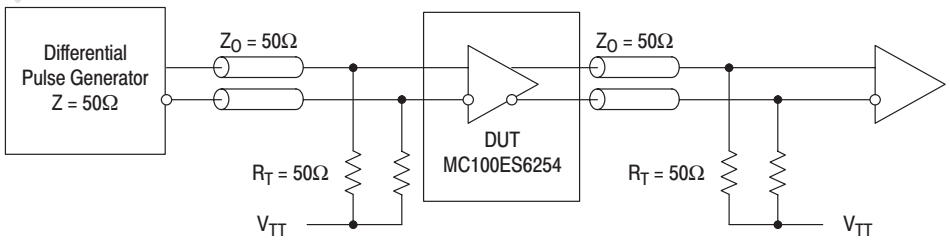
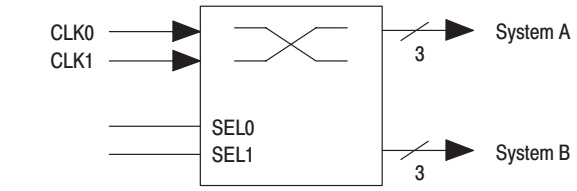



**Figure 4. MC100ES6254 AC test reference**

## APPLICATIONS INFORMATION

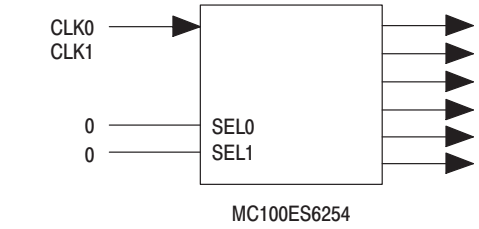
### Example Configurations

2x2 clock switch

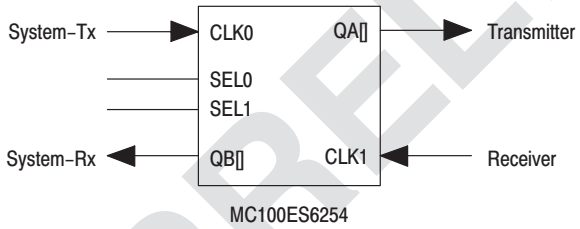



| SEL0 | SEL1 | Switch configuration |
|---|---|---|
| 0 | 0 | CLK0 clocks system A and system B |
| 0 | 1 | CLK1 clocks system A and system B |
| 1 | 0 | CLK0 clocks system A and CLK1 clocks system B |
| 1 | 1 | CLK1 clocks system B and CLK1 clocks system A |

1:6 Clock Fanout Buffer




Loopback device




| SEL0 | SEL1 | Switch configuration |
|---|---|---|
| 0 | 0 | System loopback |
| 0 | 1 | Line loopback |
| 1 | 0 | Transmit / Receive operation |
| 1 | 1 | System and line loopback |

### Maintaining Lowest Device Skew

The MC100ES6254 guarantees low output-to-output bank skew of 25 ps[1] and a part-to-part skew of max. TBD ps. To ensure low skew clock signals in the application, both outputs of any differential output pair need to be terminated identically, even if only one output is used. When fewer than all nine output pairs are used, identical termination of all output pairs within the output bank is recommended. If an entire output bank is not used, it is recommended to leave all of these outputs open and unterminated. This will reduce the device power consumption while maintaining minimum output skew.

### Power Supply Bypassing

The MC100ES6254 is a mixed analog/digital product. The differential architecture of the MC100ES6254 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all $V_{CC}$ pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

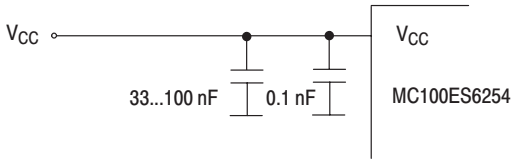



**Figure 5. $V_{CC}$ Power Supply Bypass**

1. Pending final characterization

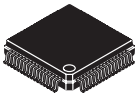
**Order Number: MC100ES8223/D**
**Rev 0, 11/2001**

*Preliminary Information*

# Low Voltage 1:22 Differential HSTL Clock Fanout Buffer

**MC100ES8223**

**LOW–VOLTAGE**
**1:22 DIFFERENTIAL HSTL**
**CLOCK FANOUT DRIVER**



**TC SUFFIX**
64–LEAD LQFP PACKAGE
EXPOSED PAD
CASE 840K

The Motorola MC100ES8223 is a bipolar monolithic differential clock fanout buffer. Designed for the most demanding clock distribution systems, the MC100ES8223 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver are high performance clock distribution in computing, networking and telecommunication systems.

**Features**

- 1:22 differential clock fanout buffer
- 50 ps maximum device skew[1]
- SiGe technology
- Supports DC to 800 MHz operation[1] of clock or data signals
- 1.5V HSTL compatible differential clock outputs
- PECL and HSTL compatible differential clock inputs
- 3.3V power supply for device core, 1.5V or 1.8V HSTL output supply
- Standard 64 lead LQFP package with exposed pad for enhanced thermal characteristics
- Supports industrial temperature range
- Pin and function compatible to the MC100EP223

**Functional Description**

The MC100ES8223 is designed for low skew clock distribution systems and supports clock frequencies up to 800 MHz[1]. The device accepts two clock sources. The HCLK input can be driven by HSTL compatible signals, the PCLK input accepts PECL compatible signals. The selected input signal is distributed to 22 identical, differential HSTL outputs.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all 22 outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The HSTL compatible output levels are generated with an open emitter architecture. This minimizes part–to–part and output–to–output skew. The open-emitter outputs require a 50Ω DC termination to GND (0V). The output supply voltage can be either 1.5V or 1.8V, the core voltage supply is 3.3V. The output enable (OE) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. In the case of an asynchronous control, there is a chance of generating a 'runt' clock pulse when the device is enabled/disabled.

The MC100ES8223 is pin and function compatible to the MC100EP223.



6

1. AC specifications are design targets and subject to change



**Rev 0**

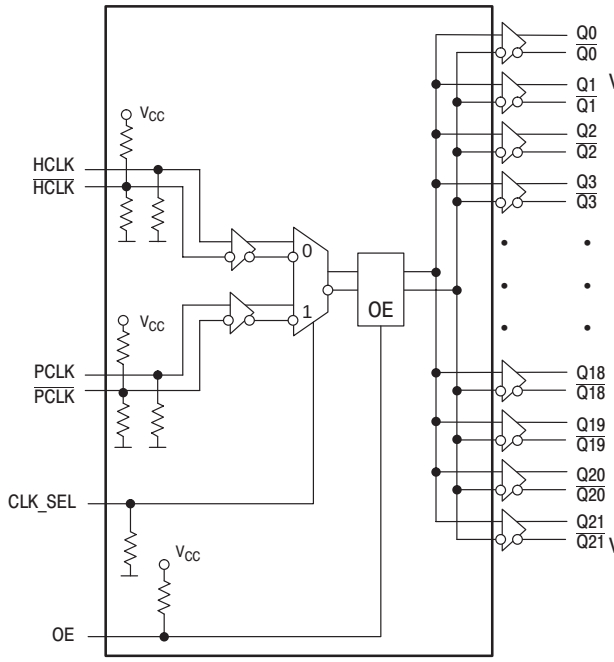



**Figure 1. MC100ES8223 Logic Diagram**

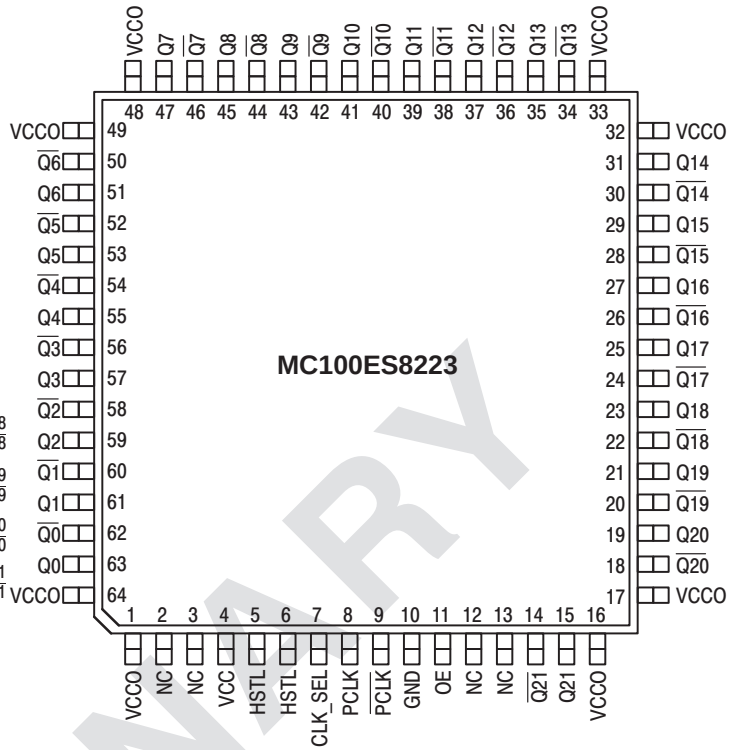



**Figure 2. 64–Lead Package Pinout** (Top View)

**Table 1. Pin Configuration**

| Pin | I/O | Type | Function |
|---|---|---|---|
| HCLK1, $\overline{HCLK}$ | Input | HSTL | Differential HSTL reference clock signal input |
| PCLK, $\overline{PCLK0}$ | Input | PECL | Differential PECL reference clock signal input |
| CLK_SEL | Input | LVCMOS | Reference clock input select |
| OE | Input | LVCMOS | Output enable/disable. OE is synchronous to the input reference clock which eliminates possible output runt pulses when the OE state is changed. |
| Q[0-21], $\overline{Q[0\text{-}21]}$ | Output | HSTL | Differential clock outputs |
| GND | Supply | | Negative power supply |
| $V_{CC}$ | Supply | | Positive power supply of the device core (3.3V) |
| $V_{CCO}$ | Supply | | Positive power supply of the HSTL outputs. All $V_{CCO}$ pins must be connected to the positive power supply (1.5V or 1.8V) for correct DC and AC operation. |

**Table 2. Function Table**

| Pin | 0 | 1 |
|---|---|---|
| CLK_SEL | HCLK, $\overline{HCLK}$ input pair is the reference clock. HCLK is HSTL compatible. | PCLK, $\overline{PCLK}$ input pair is the reference clock. PCLK is PECL compatible. |
| OE | Outputs disabled, Q[0:21]=L, $\overline{Q[0:21]}$=H | Outputs enabled |

**Table 3. Absolute Maximum Ratings[a]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{CCO}$ | Supply Voltage | -0.3 | 3.6 | V | |
| $V_{IN}$ | DC Input Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | -0.3 | $V_{CC}$ + 0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | -65 | 125 | °C | |

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 4. General Specifications**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output termination voltage | | 0 | | V | |
| MM | ESD Protection (Machine model) | 200 | | | V | |
| HBM | ESD Protection (Human body model) | 2000 | | | V | |
| CDM | ESD Protection (Charged device model) | TBD | | | V | |
| LU | Latch-up immunity | 200 | | | mA | |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | Inputs |
| $\theta_{JA}$, $\theta_{JB}$, $\theta_{JC}$ | Thermal resistance (junction–to–ambient, junction–to–board, junction–to–case) | See Table 7 ”Thermal Resistance” on page 630 | | | °C/W | |
| $T_J$ | Operating junction temperature[a] (continuous operation) MTBF = 9.1 years | 0 | | 110 | °C | |

a. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES8223 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES8223 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

**Table 5. DC Characteristics** ($V_{CC}$ = 3.3V±5%, $V_{CCO}$ = 1.5V±0.1V or $V_{CCO}$=1.8V±0.1V, $T_J$ = 0°C to + 110°C)[a]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Clock input pair HCLK, $\overline{HCLK}$ (HSTL differential signals) | | | | | | |
| $V_{DIF}$ | Differential input voltage[b] | 0.2 | | | V | |
| $V_{X, IN}$ | Differential cross point voltage[c] | 0.68 | | 0.9 | V | |
| $V_{IH}$ | Input high voltage | $V_X$+0.1 | | | V | |
| $V_{IL}$ | Input low voltage | | | $V_X$-0.1 | V | |
| $I_{IN}$ | Input Current | | | ±150 | µA | $V_{IN} = V_X \pm 0.1V$ |
| Clock input pair PCLK, $\overline{PCLK}$ (PECL differential signals) | | | | | | |
| $V_{PP}$ | Differential input voltage[d] | 0.15 | | 1.0 | V | Differential operation |
| $V_{CMR}$ | Differential cross point voltage[e] | 1.0 | | $V_{CC}$-0.6 | V | Differential operation |
| $V_{IH}$ | Input voltage high | $V_{CC}$-1.165 | | $V_{CC}$-0.880 | V | |
| $V_{IL}$ | Input voltage low | $V_{CC}$-1.810 | | $V_{CC}$-1.475 | V | |
| $I_{IN}$ | Input Current[a] | | | ±150 | µA | $V_{IN} = V_{IH}$ or $V_{IN}$ |
| LVCMOS control inputs OE, CLK_SEL | | | | | | |
| $V_{IL}$ | Input voltage low | | | 0.8 | V | |
| $V_{IH}$ | Input voltage high | 2.0 | | | V | |
| $I_{IN}$ | Input Current | | | ±150 | µA | $V_{IN} = V_{IH}$ or $V_{IN}$ |
| HSTL clock outputs (Q[0-21], $\overline{Q[0-21]}$) | | | | | | |
| $V_{X, OUT}$ | Output differential crosspoint | 0.68 | 0.75 | 0.9 | V | |
| $V_{OH}$ | Output High Voltage | 1.1 | | | V | |
| $V_{OL}$ | Output Low Voltage | | | 0.4 | V | |
| Supply current | | | | | | |
| $I_{CC}$ | Maximum Quiescent Supply Current without output termination current | | TBD | TBD | mA | $V_{CC}$ pin (core) |
| $I_{CCO}$[f] | Maximum Quiescent Supply Current, outputs terminated 50Ω to $V_{TT}$ | | TBD | TBD | mA | $V_{CCO}$ pins (outputs) |

a. DC characteristics are design targets and pending characterization.
b. $V_{DIF}$ (DC) is the minimum differential HSTL input voltage swing required for device functionality.
c. $V_X$ (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the $V_X$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.
d. $V_{PP}$ (DC) is the minimum differential input voltage swing required to maintain device functionality.
e. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.
f. $I_{CC}$ includes current through the output resistors (all outputs terminated to $V_{TT}$).

**Table 6. AC Characteristics** ($V_{CC}$ = 3.3V±5%, $V_{CCO}$ = 1.5V±0.1V or $V_{CCO}$ = 1.8V±0.1V, $T_J$ = 0°C to + 110°C)[a] [b]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Clock input pair HCLK, $\overline{HCLK}$ (HSTL differential signals) | | | | | | |
| $V_{DIF}$ | Differential input voltage[c] (peak-to-peak) | 0.4 | | | V | |
| $V_{X, IN}$ | Differential cross point voltage[d] | 0.68 | | 0.9 | V | |
| $f_{CLK}$ | Input Frequency | | 0-800 | TBD | MHz | |
| $t_{PD}$ | Propagation Delay HCLK0 to Q[0-21] | | | TBD | ps | |
| Clock input pair PCLK, $\overline{PCLK}$ (PECL differential signals) | | | | | | |
| $V_{PP}$ | Differential input voltage[e] (peak-to-peak) | 0.2 | | 1.0 | V | |
| $V_{CMR}$ | Differential input crosspoint voltage[f] | 1 | | $V_{CC}$-0.6 | V | |
| $f_{CLK}$ | Input Frequency | | 0-800 | | MHz | Differential |
| $t_{PD}$ | Propagation Delay PCLK0 to Q[0-21] | | | TBD | ps | Differential |
| HSTL clock outputs (Q[0-21], $\overline{Q[0-21]}$) | | | | | | |
| $V_{X, OUT}$ | Output differential crosspoint | 0.68 | 0.75 | 0.9 | V | |
| $V_{OH}$ | Output High Voltage | 1 | | | V | |
| $V_{OL}$ | Output Low Voltage | | | 0.5 | V | |
| $V_{O(P-P)}$ | Differential output voltage (peak-to-peak) | 0.5 | | | V | |
| $t_{sk(O)}$ | Output-to-output skew | | | 50 | ps | Differential |
| $t_{sk(PP)}$ | Output-to-output skew (part-to-part) | | | TBD | ps | Differential |
| $t_{JIT(CC)}$ | Output cycle-to-cycle jitter | | | TBD | | |
| $DC_O$ | Output duty cycle | TBD | 50 | TBD | % | $DC_{fref}$= 50% |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.05 | | TBD | ns | 20% to 80% |

a. DC characteristics are design targets and pending characterization.
b. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$.
c. $V_{DIF}$ (DC) is the minimum differential HSTL input voltage swing required for device functionality.
d. $V_X$ (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the $V_X$ (DC) range and the input swing lies within the $V_{DIF}$ (DC) specification.
e. $V_{PP}$ (AC) is the minimum differential PECL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
f. $V_{CMR}$ (AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ (AC) range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ (AC) or $V_{PP}$ (AC) impacts the device propagation delay, device and part-to-part skew.



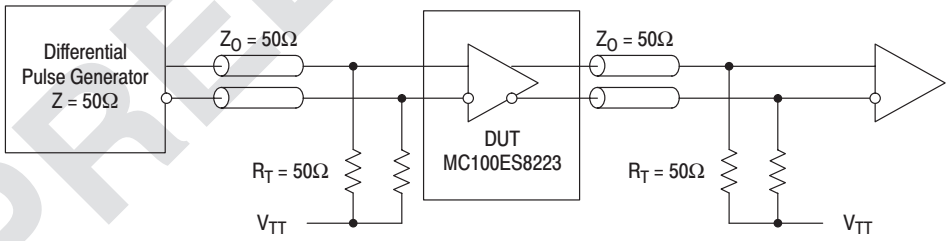



**Figure 3. MC100ES8223 AC test reference**

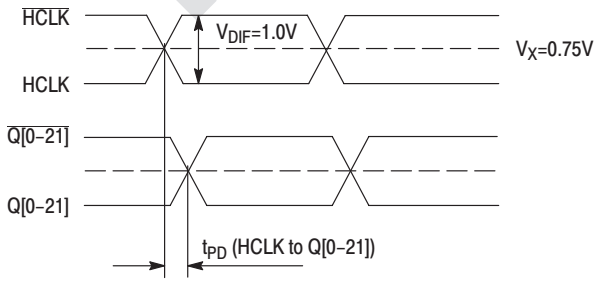



**Figure 4. MC100ES8223 AC reference measurement waveform**

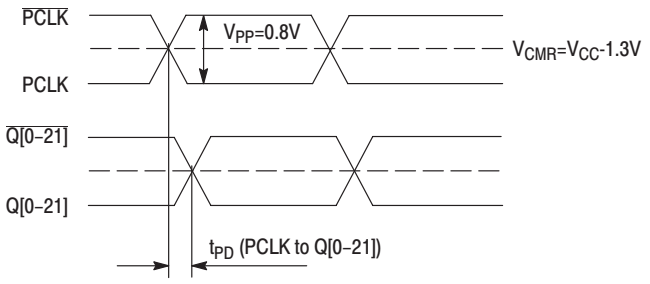



**Figure 5. MC100ES8223 AC reference measurement waveform**

## APPLICATIONS INFORMATION

### Using the thermally enhanced package of the MC100ES8223

The MC100ES8223 uses a thermally enhanced exposed pad (EP) 64 lead LQFP package. The package is molded so that the leadframe is exposed at the surface of the package bottom side. The exposed metal pad will provide the low thermal impedance that supports the power consumption of the MC100ES8223 high-speed bipolar integrated circuit and eases the power management task for the system design. A thermal land pattern on the printed circuit board and thermal vias are recommended in order to take advantage of the enhanced thermal capabilities of the MC100ES8223. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal path. In multilayer board designs, thermal vias thermally connect the exposed pad to internal copper planes. Number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package. A nine thermal via array, arranged in a 3 x 3 array and using a 1.2 mm pitch in the center of the thermal land is the absolute minimum requirement for MC100ES8223 applications on multi-layer boards. The recommended thermal land design comprises a 5 x 5 thermal via array as shown in Figure 6 “Recommended thermal land pattern”, providing an efficient heat removal path.

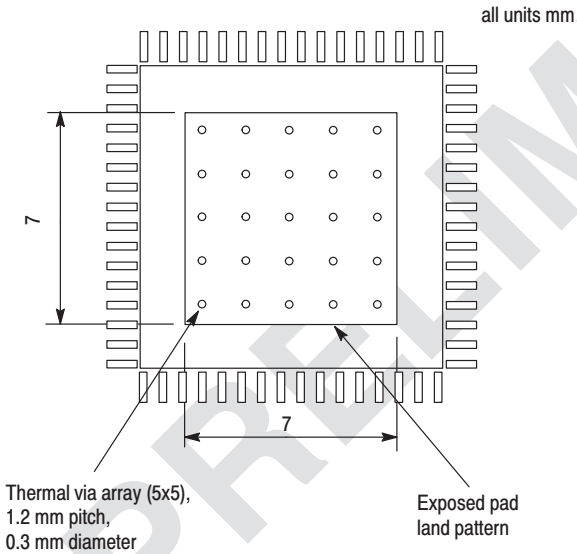



**Figure 6. Recommended thermal land pattern**

The via diameter is should be approx. 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via resulting in voids during the solder process must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for exposed pad package is equivalent to standard surface mount packages. Figure 7 “Recommended solder mask openings” shows a recommend solder mask opening with respect to the recommended 5 x 5 thermal via array. Because a large solder mask opening may result in a poor release, the opening should be subdivided as shown in Figure 7 For the nominal package standoff 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

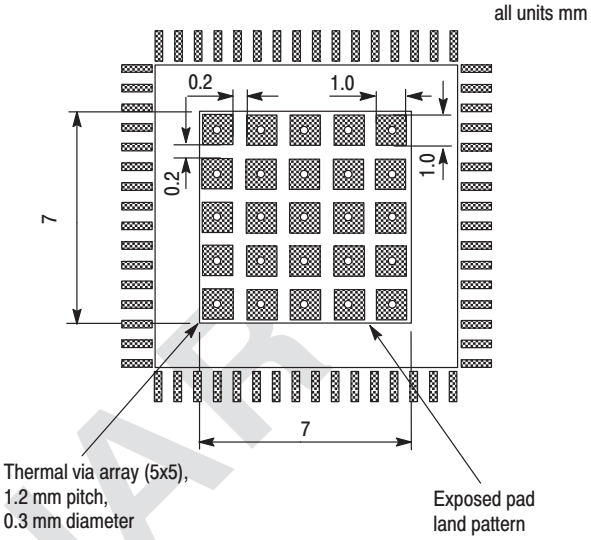



**Figure 7. Recommended solder mask openings**

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided. For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

**Table 7. Thermal Resistance[a]**

| Convection-LFPM | $R_{THJA}$[b] °C/W | $R_{THJA}$[c] °C/W | $R_{THJC}$[d] °C/W | $R_{THJB}$[e] °C/W |
|---|---|---|---|---|
| Natural | 57.1 | 24.9 | 15.8 | 9.7 |
| 100 | 50.0 | 21.3 | | |
| 200 | 46.9 | 20.0 | | |
| 400 | 43.4 | 18.7 | | |
| 800 | 38.6 | 16.9 | | |

a. Thermal data pattern with a 3 x 3 thermal via array on 2S2P boards (based on empirical results)
b. Junction to ambient, single layer test board, per JESD51-6
c. Junction to ambient, four conductor layer test board (2S2P), per JES51-6
d. Junction to case, per MIL-SPEC 883E, method 1012.1
e. Junction to board, four conductor layer test board (2S2P) per JESD 51-8

It is recommended that users employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100ES8223 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals. The thermal land should be connected to GND through connection of internal board layers.

# Chapter Seven
# Packaging Information

The packaging information for each device type can be determined in one of two ways: by the specific case number indicated on the individual data sheet (for example, the case number for MPC9600/D is 932), or by using the *Case Dimension Cross–Reference Tables* provided at the beginning of this chapter. Case dimension information is presented in numerical order; by case number.

7

# Case Dimension Cross-Reference Tables

**Table 1. Clock Generators**

| Device | Package | Case Number | Page |
|---|---|---|---|
| MPC930 | 32 TQFP | 873A | 638 |
| MPC931 | 32 TQFP | 873A | 638 |
| MPC9315 | 32 LQFP | 873A | 638 |
| MPC932 | 32 TQFP | 873A | 638 |
| MPC9350 | 32 LQFP | 873A | 638 |
| MPC9351 | 32 LQFP | 873A | 638 |
| MPC9352 | 32 LQFP | 873A | 638 |
| MPC950 | 32 LQFP | 873A | 638 |
| MPC951 | 32 LQFP | 873A | 638 |
| MPC952 | 32 LQFP | 873A | 638 |
| MPC9600 | 48 LQFP | 932 | 639 |
| MPC972 | 52 TQFP | 848D | 637 |
| MPC973 | 52 TQFP | 848D | 637 |
| MPC974 | 52 TQFP | 848D | 637 |
| MPC9893 | 48 LQFP | 932 | 639 |
| MPC9857FA | 48 TSSOP | 1201 | 641 |
| MPC990 | 52 TQFP | 848D | 637 |
| MPC991 | 52 TQFP | 848D | 637 |
| MPC992 | 32 LQFP | 873A | 638 |
| MPC993 | 32 LQFP | 873A | 638 |
| MPC9952 | 32 LQFP | 873A | 638 |
| MPC9990 | 48 LQFP | 932 | 639 |
| MC88915T | 28 LQFP | 776 | 635 |
| MC88LV915T | 28 LQFP | 776 | 635 |
| MC88LV926 | 20 LQFP | 751D | 634 |

**Table 2. Clock Synthesizers**

| Device | Package | Case Number | Page |
|---|---|---|---|
| MC12429 | 28 PLCC | 776 | 635 |
| | 32 LQFP | 873A | 638 |
| MC12430 | 28 PLCC | 776 | 635 |
| | 32 LQFP | 873A | 638 |
| MC12439 | 28 PLCC | 776 | 635 |
| MPC998 | 32 LQFP | 873A | 638 |
| MPC9994 | 32 LQFP | 873A | 638 |

**Table 3. Zero–Delay Buffers**

| Device | Package | Case Number | Page |
|---|---|---|---|
| MPC953 | 32 LQFP | 873A | 638 |
| MPC954 | 24 TSSOP | 948H | 640 |
| MPC958 | 32 LQFP | 873A | 638 |
| MPC961C | 32 LQFP | 873A | 638 |
| MPC961P | 32 LQFP | 873A | 638 |
| MPC9608 | 32 LQFP | 873A | 638 |

**Table 4. LVCMOS Fanout Buffers**

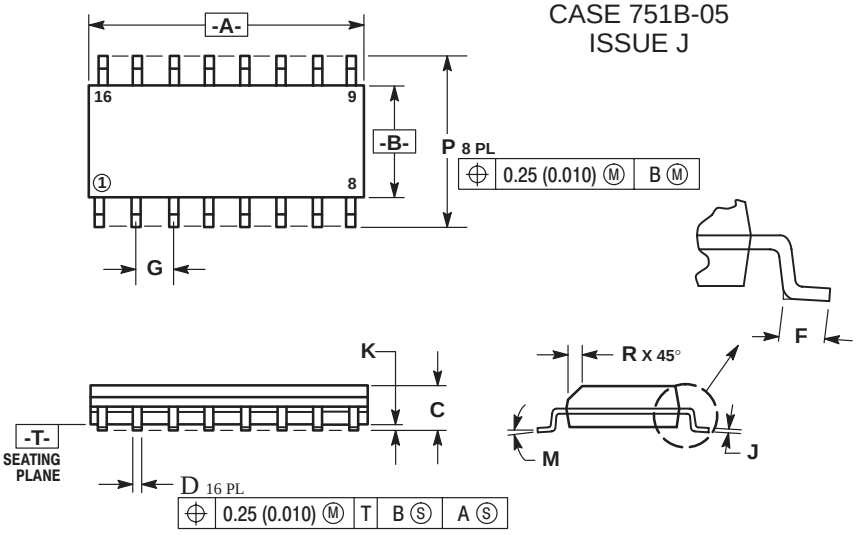
| Device | Package | Case Number | Page |
|---|---|---|---|
| MPC905 | 16 SOIC | 751B | 634 |
| MPC940L | 32 QFP/LQFP | 873A | 638 |
| MPC941 | 48 LQFP | 932 | 639 |
| MPC942C | 32 LQFP | 873A | 638 |
| MPC942P | 32 LQFP | 873A | 638 |
| MPC9443 | 48 LQFP | 932 | 639 |
| MPC9446 | 32 LQFP | 873A | 638 |
| MPC9456 | 32 LQFP | 873A | 638 |
| MPC946 | 32 LQFP | 873A | 638 |
| MPC947 | 32 LQFP | 873A | 638 |
| MPC948 | 32 LQFP | 873A | 638 |
| MPC949 | 52 LQFP | 848D | 637 |

**Table 5. Differential Fanout Buffers**

| Device | Package | Case Number | Page |
|---|---|---|---|
| MC100EP111 | 32 LQFP | 873A | 638 |
| MC100EP210 | 32 LQFP | 873A | 638 |
| MC100EP220 | 52 LQFP exposed pad | 848D | 637 |
| MC100EP221 | 52 LQFP exposed pad | 848D | 637 |
| MC100EP222 | 52 LQFP exposed pad | 848D | 637 |
| MC100EP223 | 64 LQFP exposed pad | 840K | 636 |
| MC100ES6226 | 32 LQFP | 873A | 638 |
| MC100ES6254 | 32 LQFP | 873A | 638 |

# Case Dimensions

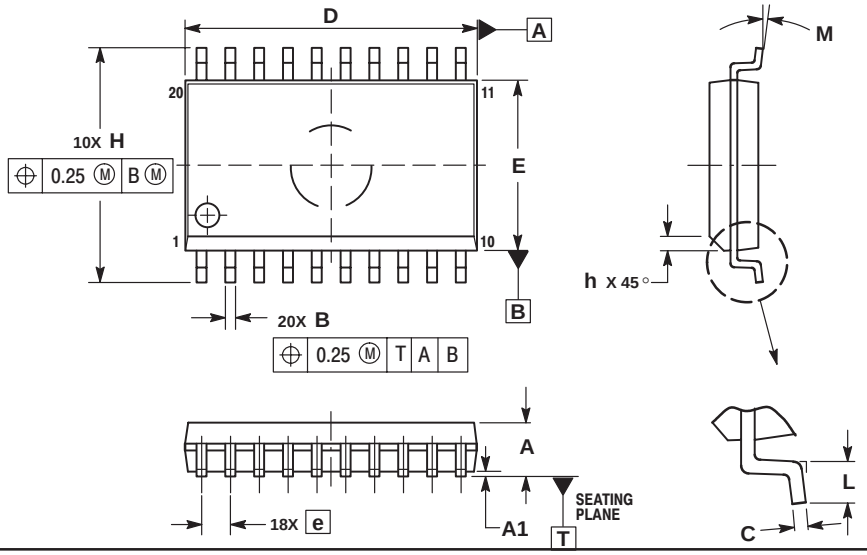
**D SUFFIX**
PLASTIC SOIC PACKAGE
CASE 751B-05
ISSUE J




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

**DW SUFFIX**
PLASTIC SOIC PACKAGE
CASE 751D-06
ISSUE G

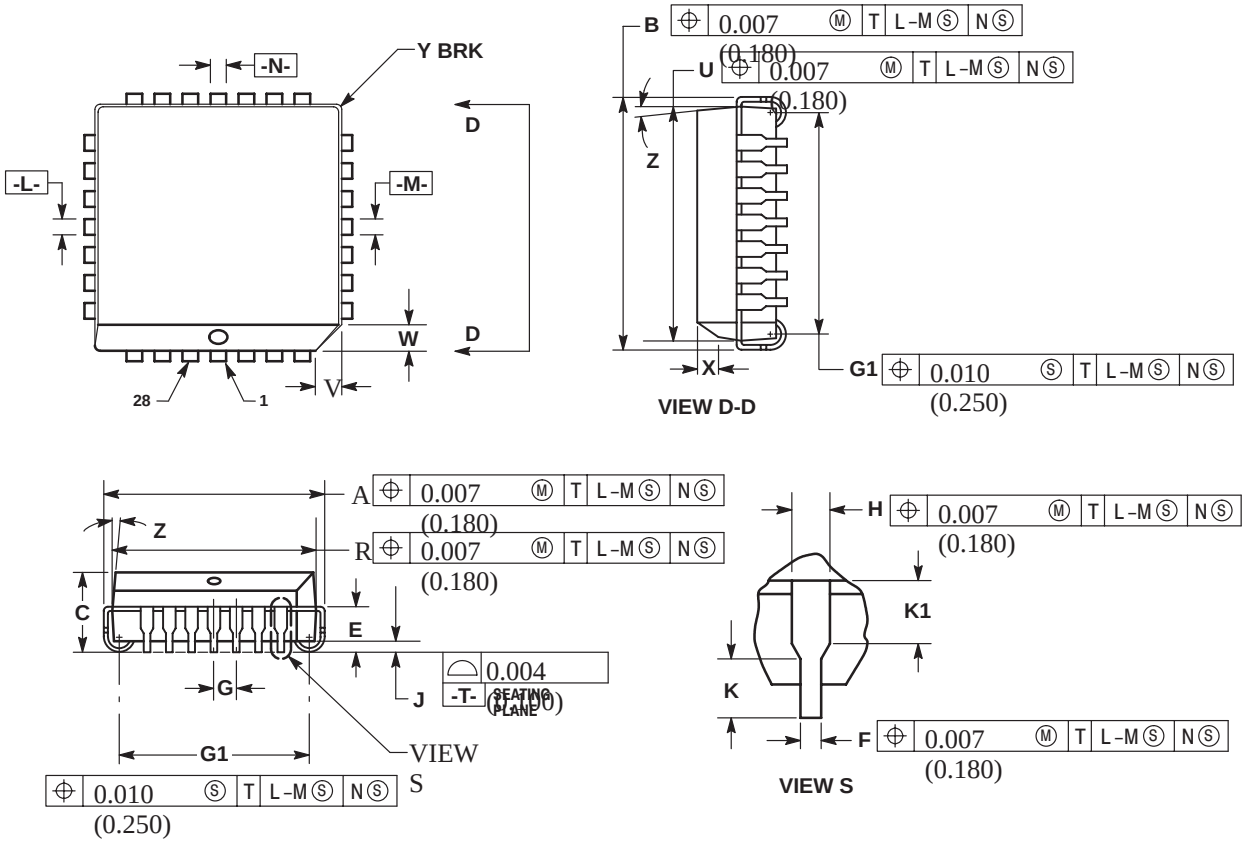



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.40 | 1.00 |
| θ | 0 ° | 7 ° |

7

**FN SUFFIX**
PLASTIC PLCC PACKAGE
CASE 776-02
ISSUE D

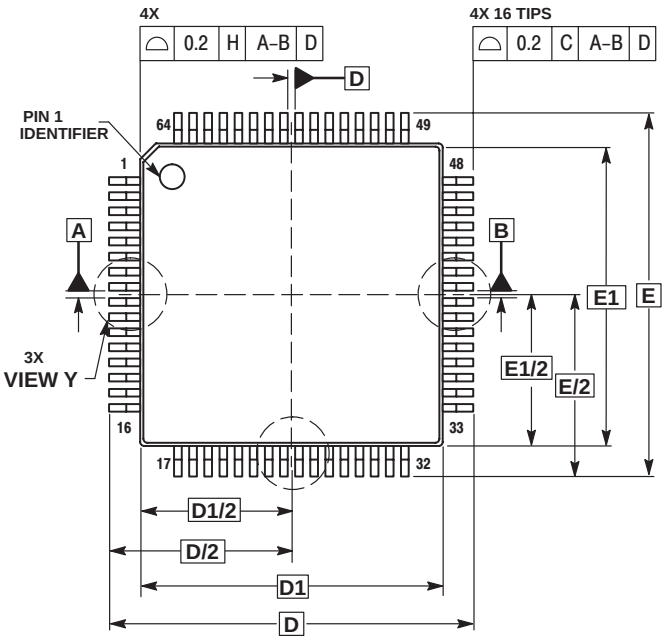


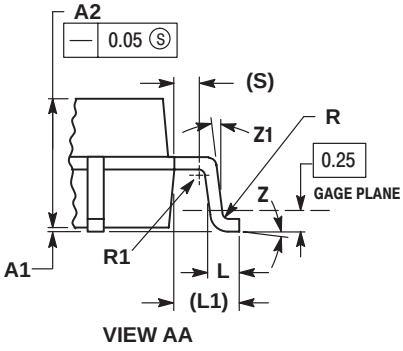

NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.485 | 0.495 | 12.32 | 12.57 |
| B | 0.485 | 0.495 | 12.32 | 12.57 |
| C | 0.165 | 0.180 | 4.20 | 4.57 |
| E | 0.090 | 0.110 | 2.29 | 2.79 |
| F | 0.013 | 0.019 | 0.33 | 0.48 |
| G | 0.050 BSC | | 1.27 BSC | |
| H | 0.026 | 0.032 | 0.66 | 0.81 |
| J | 0.020 | — | 0.51 | — |
| K | 0.025 | — | 0.64 | — |
| R | 0.450 | 0.456 | 11.43 | 11.58 |
| U | 0.450 | 0.456 | 11.43 | 11.58 |
| V | 0.042 | 0.048 | 1.07 | 1.21 |
| W | 0.042 | 0.048 | 1.07 | 1.21 |
| X | 0.042 | 0.056 | 1.07 | 1.42 |
| Y | — | 0.020 | — | 0.50 |
| Z | 2° | 10° | 2° | 10° |
| G1 | 0.410 | 0.430 | 10.42 | 10.92 |
| K1 | 0.040 | — | 1.02 | — |

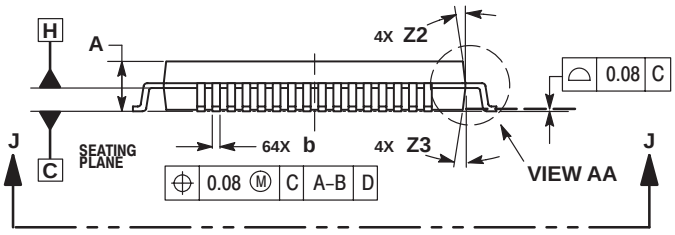
7

**DT SUFFIX**
PLASTIC SSOP PACKAGE
CASE 840K-01
ISSUE O

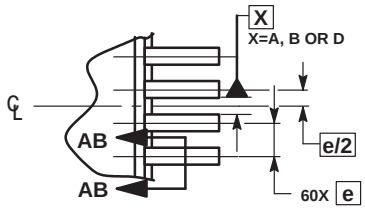


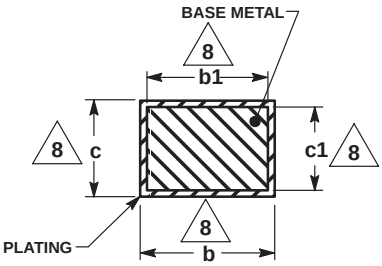

VIEW AA



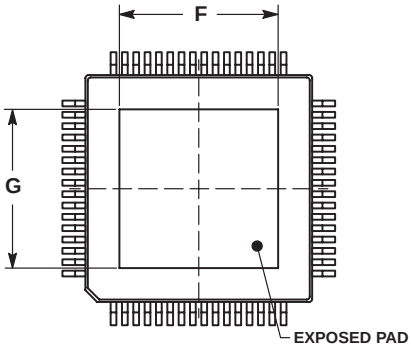

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 mm.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.




VIEW Y




SECTION AB–AB
ROTATED 90° CLOCKWISE

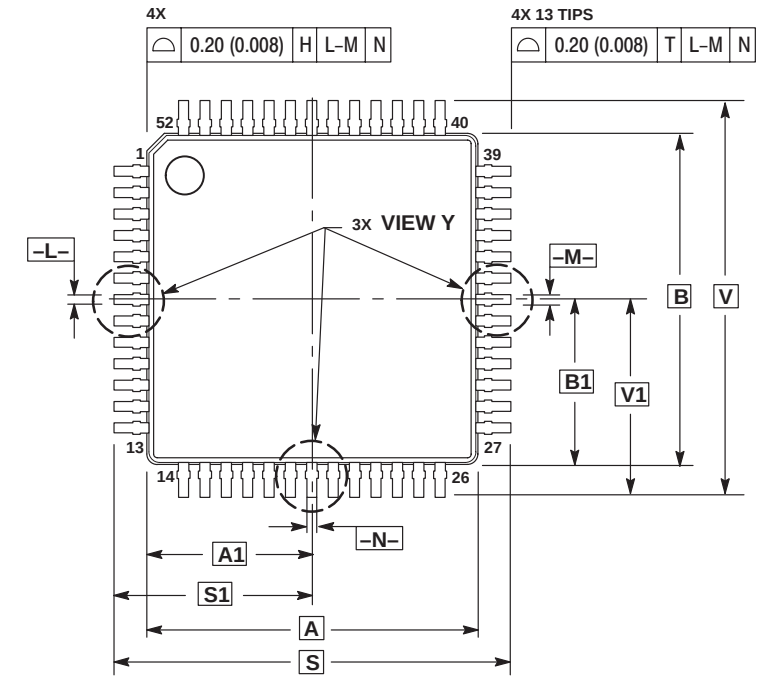


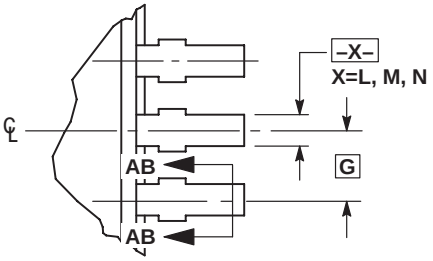

VIEW J–J

| DIM | MILLIMETERS MIN | MAX |
|---|---|---|
| A | --- | 1.60 |
| A1 | 0.05 | 0.15 |
| A2 | 1.35 | 1.45 |
| b | 0.17 | 0.27 |
| b1 | 0.17 | 0.23 |
| c | 0.09 | 0.20 |
| c1 | 0.09 | 0.16 |
| D | 12.00 BSC | |
| D1 | 10.00 BSC | |
| e | 0.50 BSC | |
| E | 12.00 BSC | |
| E1 | 10.00 BSC | |
| L | 0.45 | 0.75 |
| L1 | 1.00 REF | |
| R1 | 0.08 | --- |
| R2 | 0.08 | --- |
| S | 0.20 | --- |
| F | 6.00 | 7.00 |
| G | 6.00 | 7.00 |
| Z | 0° | 7° |
| Z1 | 0° | --- |
| Z2 | 11° | 13° |
| Z3 | 11° | 13° |

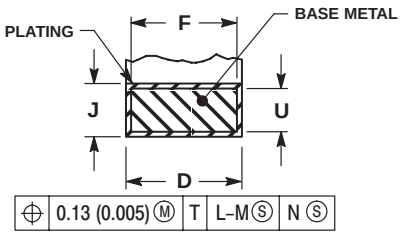
7

**FA SUFFIX**
PLASTIC TQFP PACKAGE
CASE 848D–03
ISSUE D

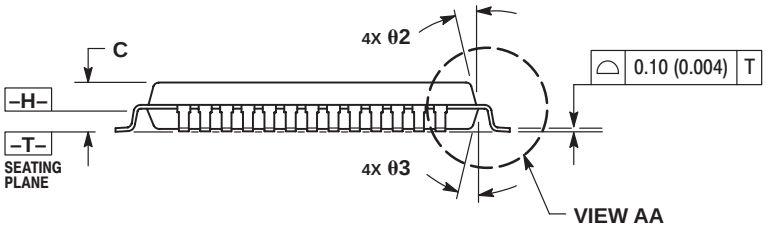


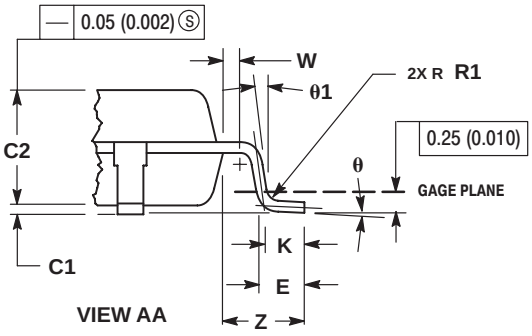




VIEW Y




SECTION AB–AB
ROTATED 90° CLOCKWISE



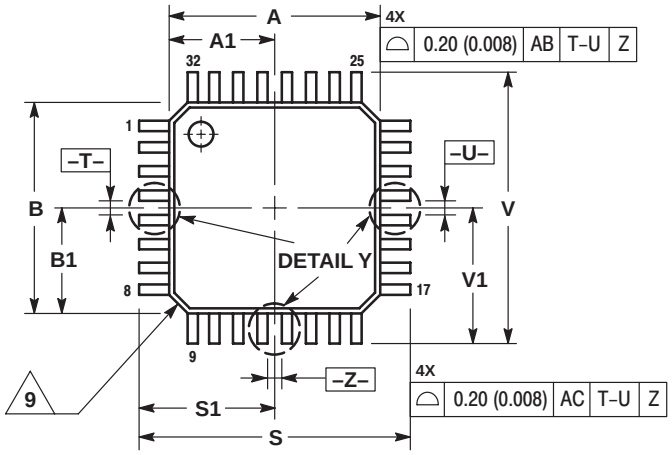



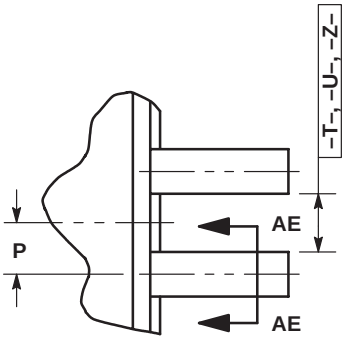

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 10.00 BSC | | 0.394 BSC | |
| A1 | 5.00 BSC | | 0.197 BSC | |
| B | 10.00 BSC | | 0.394 BSC | |
| B1 | 5.00 BSC | | 0.197 BSC | |
| C | --- | 1.70 | --- | 0.067 |
| C1 | 0.05 | 0.20 | 0.002 | 0.008 |
| C2 | 1.30 | 1.50 | 0.051 | 0.059 |
| D | 0.20 | 0.40 | 0.008 | 0.016 |
| E | 0.45 | 0.75 | 0.018 | 0.030 |
| F | 0.22 | 0.35 | 0.009 | 0.014 |
| G | 0.65 BSC | | 0.026 BSC | |
| J | 0.07 | 0.20 | 0.003 | 0.008 |
| K | 0.50 REF | | 0.020 REF | |
| R1 | 0.08 | 0.20 | 0.003 | 0.008 |
| S | 12.00 BSC | | 0.472 BSC | |
| S1 | 6.00 BSC | | 0.236 BSC | |
| U | 0.09 | 0.16 | 0.004 | 0.006 |
| V | 12.00 BSC | | 0.472 BSC | |
| V1 | 6.00 BSC | | 0.236 BSC | |
| W | 0.20 REF | | 0.008 REF | |
| Z | 1.00 REF | | 0.039 REF | |
| θ | 0° | 7° | 0° | 7° |
| θ1 | 0° | --- | 0° | --- |
| θ2 | 12° REF | | 12° REF | |
| θ3 | 12° REF | | 12° REF | |

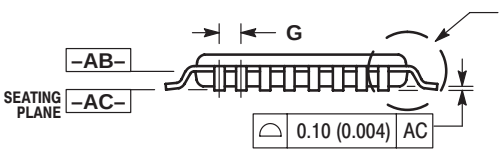
7

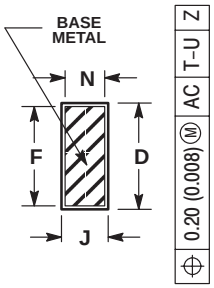
**FA SUFFIX**
PLASTIC TQFP PACKAGE
CASE 873A-02
ISSUE A



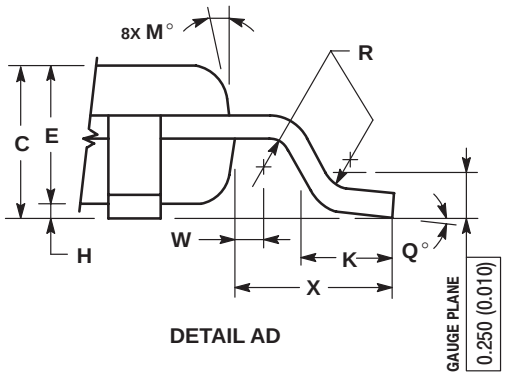




**DETAIL Y**




**SECTION AE–AE**



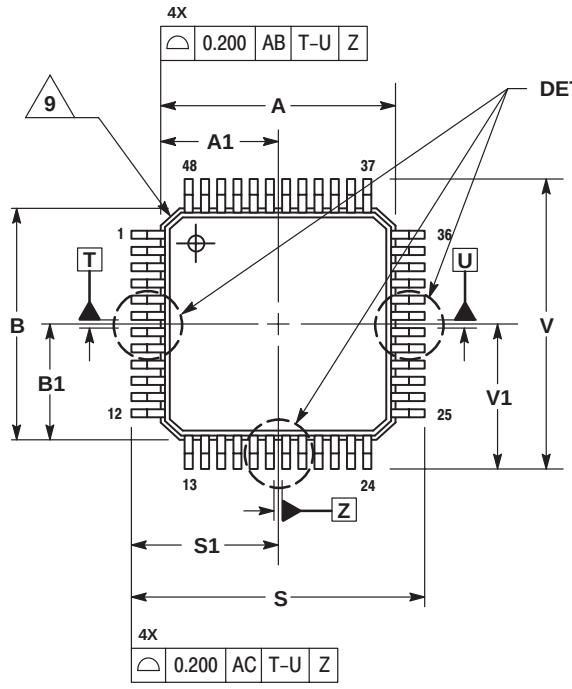

**DETAIL AD**

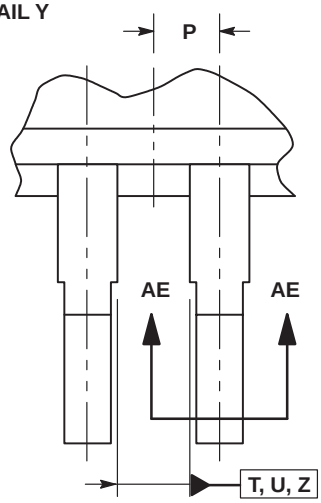
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 7.000 BSC | | 0.276 BSC | |
| A1 | 3.500 BSC | | 0.138 BSC | |
| B | 7.000 BSC | | 0.276 BSC | |
| B1 | 3.500 BSC | | 0.138 BSC | |
| C | 1.400 | 1.600 | 0.055 | 0.063 |
| D | 0.300 | 0.450 | 0.012 | 0.018 |
| E | 1.350 | 1.450 | 0.053 | 0.057 |
| F | 0.300 | 0.400 | 0.012 | 0.016 |
| G | 0.800 BSC | | 0.031 BSC | |
| H | 0.050 | 0.150 | 0.002 | 0.006 |
| J | 0.090 | 0.200 | 0.004 | 0.008 |
| K | 0.500 | 0.700 | 0.020 | 0.028 |
| M | 12° REF | | 12° REF | |
| N | 0.090 | 0.160 | 0.004 | 0.006 |
| P | 0.400 BSC | | 0.016 BSC | |
| Q | 1° | 5° | 1° | 5° |
| R | 0.150 | 0.250 | 0.006 | 0.010 |
| S | 9.000 BSC | | 0.354 BSC | |
| S1 | 4.500 BSC | | 0.177 BSC | |
| V | 9.000 BSC | | 0.354 BSC | |
| V1 | 4.500 BSC | | 0.177 BSC | |
| W | 0.200 REF | | 0.008 REF | |
| X | 1.000 REF | | 0.039 REF | |

7

**FA SUFFIX**
PLASTIC LQFP PACKAGE
CASE 932-03
ISSUE F

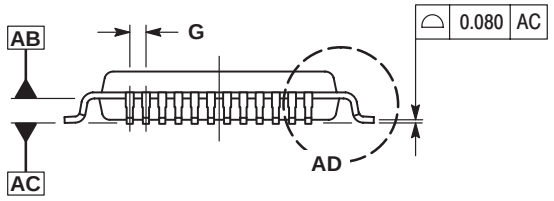


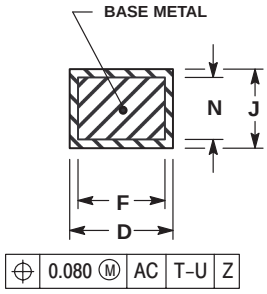




DETAIL Y

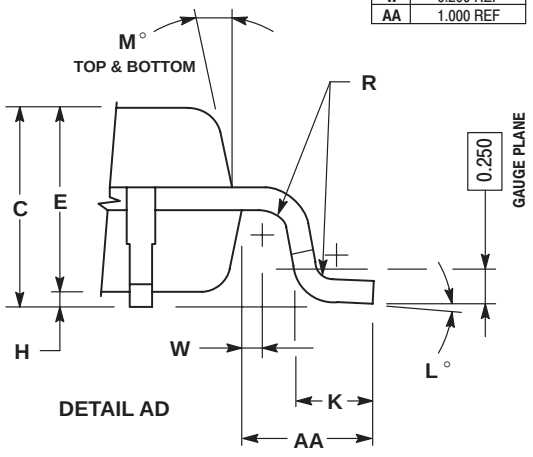
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 7.000 BSC | |
| A1 | 3.500 BSC | |
| B | 7.000 BSC | |
| B1 | 3.500 BSC | |
| C | 1.400 | 1.600 |
| D | 0.170 | 0.270 |
| E | 1.350 | 1.450 |
| F | 0.170 | 0.230 |
| G | 0.500 BSC | |
| H | 0.050 | 0.150 |
| J | 0.090 | 0.200 |
| K | 0.500 | 0.700 |
| L | 0 ° | 7 ° |
| M | 12 °REF | |
| N | 0.090 | 0.160 |
| P | 0.250 BSC | |
| R | 0.150 | 0.250 |
| S | 9.000 BSC | |
| S1 | 4.500 BSC | |
| V | 9.000 BSC | |
| V1 | 4.500 BSC | |
| W | 0.200 REF | |
| AA | 1.000 REF | |



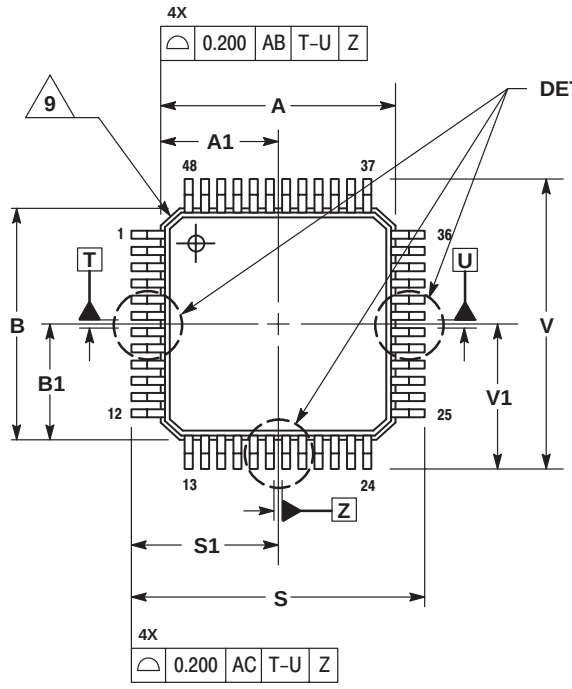

SECTION AE–AE

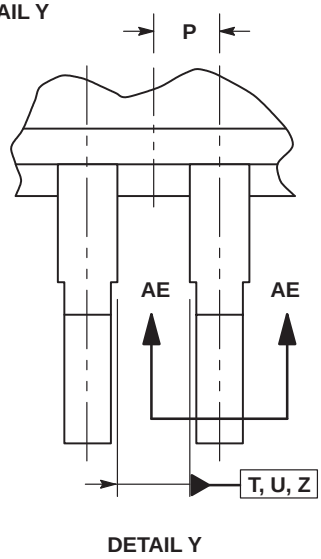



DETAIL AD

7

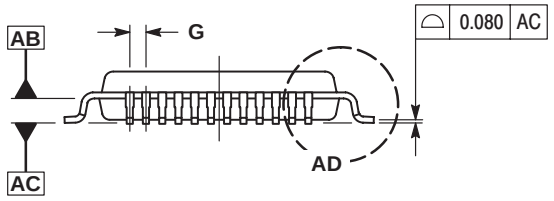
**DT SUFFIX**
PLASTIC SSOP PACKAGE
CASE 948H-01
ISSUE O

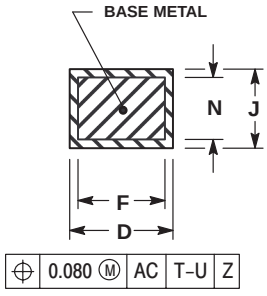


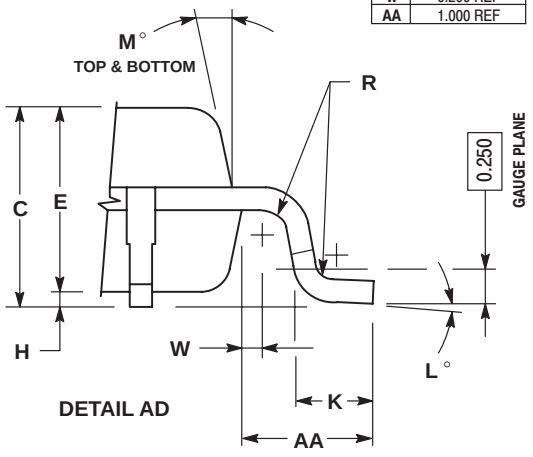

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 7.000 BSC | |
| A1 | 3.500 BSC | |
| B | 7.000 BSC | |
| B1 | 3.500 BSC | |
| C | 1.400 | 1.600 |
| D | 0.170 | 0.270 |
| E | 1.350 | 1.450 |
| F | 0.170 | 0.230 |
| G | 0.500 BSC | |
| H | 0.050 | 0.150 |
| J | 0.090 | 0.200 |
| K | 0.500 | 0.700 |
| L | 0 ° | 7 ° |
| M | 12 °REF | |
| N | 0.090 | 0.160 |
| P | 0.250 BSC | |
| R | 0.150 | 0.250 |
| S | 9.000 BSC | |
| S1 | 4.500 BSC | |
| V | 9.000 BSC | |
| V1 | 4.500 BSC | |
| W | 0.200 REF | |
| AA | 1.000 REF | |



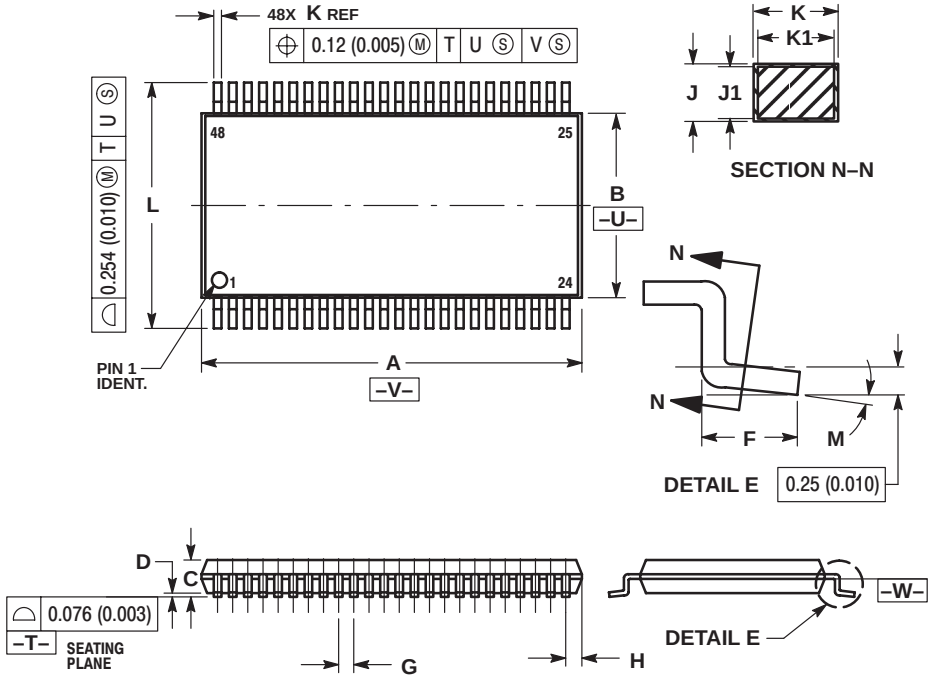

SECTION AE–AE




DETAIL AD

7

**DW SUFFIX**
PLASTIC TSSOP PACKAGE
CASE 1201-01
ISSUE A




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 12.40 | 12.60 | 0.488 | 0.496 |
| B | 6.00 | 6.20 | 0.236 | 0.244 |
| C | --- | 1.10 | --- | 0.043 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.50 BSC | | 0.0197 BSC | |
| H | 0.37 | --- | 0.015 | --- |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.17 | 0.27 | 0.007 | 0.011 |
| K1 | 0.17 | 0.23 | 0.007 | 0.009 |
| L | 7.95 | 8.25 | 0.313 | 0.325 |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

7

# Chapter Eight
# Application Notes

**Application Notes**



8

**Order Number: AN1091/D**
**Rev 4, 09/2001**

# AN1091

# Low Skew Clock Drivers and Their System Design Considerations

## ABSTRACT

This application note addresses various system design issues to help ensure that Motorola's low skew clock drivers are used effectively in a system environment.

Several varieties of clock drivers with 1 ns or less skew from output-to-output are available from Motorola. Microprocessor-based systems are now running at 33 MHz and beyond, and system clock distribution at these frequencies mandate the use of low skew clock drivers. Unfortunately, just plugging a high performance clock driver into a system does not guarantee trouble free operation. Only careful board layout and consideration of system noise issues can guarantee reliable clock distribution. This application note addresses these system design issues to help ensure that Motorola's low skew clock drivers are used effectively in a system environment.

## INTRODUCTION

With frequencies regularly reaching 33 MHz and approaching 40-50 MHz in today's CISC and RISC microprocessor systems, well controlled and precise clock signals are required to maintain a synchronous system. Many microprocessors also require input clock duty cycles very close to 50%. These stringent timing requirements mandate the use of specially designed, low skew clock distribution circuits or 'clock drivers.' However, just plugging one of these parts into your board does not ensure a trouble free system. Careful system and board design techniques must be used in conjunction with a low skew clock driver to meet system timing requirements and provide clean clock signals.

### Why are Low Skew Clock Drivers Necessary

An MPU system designer wants to utilize as much of a clock cycle as possible without adding unnecessary timing guardbands. Propagation delays of peripheral logic do not scale with frequency. Therefore, as the clock period decreases, the system designer has less time but the same logic delays to accomplish the function. How can he get more time? A viable option is to use a special clock source that minimizes clock 'uncertainty.'

A simple example illustrates this concept. At 33 MHz, $T_{cycle}$ = 30 ns. An FCT240A, for example, has a High-Low uncertainty of the min/max spread of $t_{PLH}$ to $t_{PHL}$ of approximately 3.3 ns. If 1.7 ns of pin-to-pin skew due to the actual part and PCB trace delays is also considered, then only 25 ns of the clock period is still available. The worst case $t_P$ of clock-to-data valid on the 88200 M-Bus is 12 ns, which leaves only 13 ns to accomplish additional functions. In this case 17% of a cycle is required for clock distribution or clock 'uncertainty,' which is an unacceptable penalty from a system designer's point of view. At 50 MHz this penalty becomes 25%. A maximum of 10% of the period allotted for clock distribution is an acceptable standard.

If multiple levels of clock distribution (one clock driver's output feeding the inputs of several other clock drivers) are necessary due to large clock fan-outs, the additional part-to-part skew variations add even more to the clock uncertainty. Standard logic has always been specified with a large (and conservative) delta between the minimum and maximum propagation delays. This delta creates the excessive amount of clock 'uncertainty' which the system designer has been forced to design into his system, even though it is not realistic. When system frequencies were below 16 MHz this large clock penalty could be tolerated, but as the above example points out, not anymore. A clock driver's specs guarantee this min/max delta to be a specific, small value. To reduce the clock overhead to manageable levels, a clock driver with minimal variation (<5%) from a 50% duty cycle and guaranteed low output-to-output and part-to-part skew must be used.

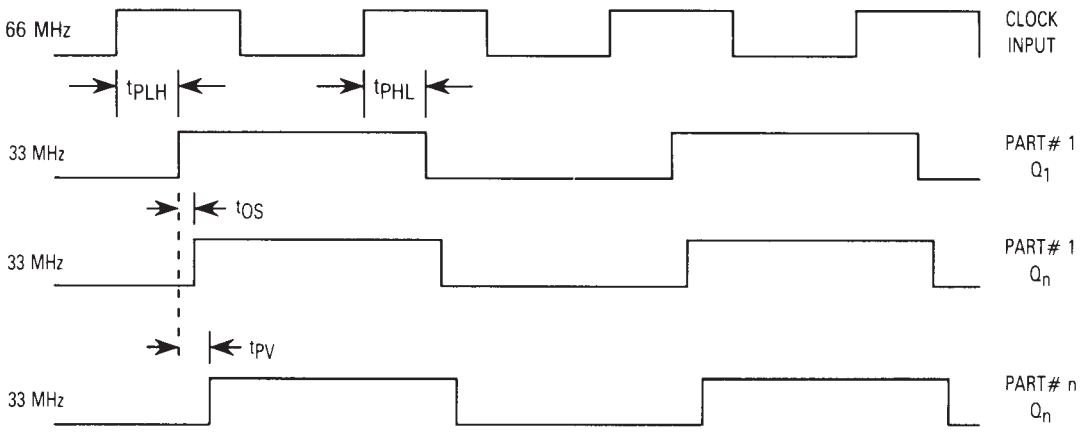
## DEFINITIONS

A typical clock driver has a single input which is usually driven by a crystal oscillator. The clock driver can have any number of outputs which have a certain frequency relationship to the clock input. Clock driver skew is typically defined by three different specs. These specs are graphically illustrated in Figure 1.

The first spec, $t_{OS}$, measures the difference between the fastest and slowest propagation delays (any transition) between the outputs of a single part. This number must be 1ns or less for high-end systems.

The second, $t_{PS}$, measures the difference between the high-to-low and low-to-high transition for a single output (pin). This spec defines how close to a 50% duty cycle the outputs of the clock driver will be. For example, if this spec is 1 ns (±0.5 ns), at 33 MHz the output duty cycle is 50% ±3.5%. A clock driver which only buffers the crystal input, creating a 1:1 input to output frequency relationship, can be a problem if a very tight tolerance to a 50% duty cycle is required. In this situation the output duty cycle is directly dependent on the input duty cycle, which is not well controlled in most crystal oscillators. The clock driver's outputs switching at half the input frequency (÷2) is a common relationship, which means that the outputs switch on only one edge of the oscillator, eliminating the output's dependence on the duty cycle of the input (crystal oscillator frequency is very stable).

The third spec, $t_{PV}$, measures the maximum propagation delay delta between any given pin on any part. This spec defines the part to part variation between any clock driver (of the same device type) which is ever shipped. This number reflects the process variation inherent in any technology. For CMOS, this spec is usually 3 ns or less. High performance ECL technologies can bring this number down into the 1-2 ns range. Another way to minimize the part-to-part variation is to use a phase-locked loop clock driver, which are just now becoming available.




Notes: 1) $t_{PS}$ measures $|t_{PLH}–t_{PHL}|$ for any single output on a part.
2) $t_{OS}$ measures the maximum difference between any $t_{PHL}$ or $t_{PLH}$ between any output on a single part.
3) $t_{PV}$ measures the maximum difference between any $t_{PHL}$ or $t_{PLH}$ between any output on any part.

**Figure 1. Timing Diagram Depicting Clock Skew Specs Within One Part and Between Any Two Parts**

An important consideration when designing a clock driver into a system is that the skew specs described above are usually specified at a fixed, lumped capacitive load. In a real system environment the clock lines usually have various loads distributed over several inches of PCB trace which can contribute additional delay and sometimes act like transmission lines, so the system designer must use careful board layout techniques to minimize the total system skew. In other words, just plugging a low skew clock driver into a board will not solve all your timing problems.

## DESIGN CONSIDERATIONS

Figure 2 is a scale replication of a section of an actual 88000 RISC system board layout. The section shown in Figure 2 includes the MC88100 MPU and the MC88200 CMMU devices and the MC88914 CMOS clock driver. The only PCB traces shown are the clock output traces from the MC88914 to the various loads. For this clock driver the output-to-output skew ($t_{OS}$) is guaranteed to be less than 1 ns at any given temperature, supply voltage, and fixed load up to 50 pF.

In calculating the total system skew, the difference in clock PCB trace length and loading must be taken into account. For an unloaded PCB trace, the signal delay per unit length, $t_{PD}$, is dependent only on the dielectric constant, $e_r$. of the board material. The characteristic impedance, $Z_O$, of the line is dependent upon $e_r$ and the geometry of the trace. These relationships are depicted in Figure 3 for a microstrip line.1 The formulas for $t_{PD}$ and $Z_O$ are slightly different for other types of strip lines, but for simplicity's sake all calculations in this article will assume a microstrip line.

The equations in Figure 3 are valid only for an unloaded trace; loading down a line will increase its delay and lower its impedance. The signal propagation delay ($t_{PD}$') and characteristic impedance ($Z_O$') due to a loaded trace are calculated by the following formulas:

$$t_{PD}' = t_{PD}\sqrt{1 + \frac{C_d}{C_O}}$$

$$Z_O' = \frac{Z_O}{\sqrt{1 + \frac{C_d}{C_O}}}$$

$C_d$ is the distributed load capacitance per unit length, which is the total input capacitance of the receiving devices divided by the length of the trace. $C_O$ is the intrinsic capacitance of the trace, which is defined as:

$$C_O = \frac{t_{PD}}{Z_O}$$

Assuming typical microstrip dimensions and characteristics as w = 0.01 in, t = 0.002 in, h = 0.012 in, and $e_r$ = 4.7, the equations of Figure 3 yield $Z_O$ = 69.4 Ω and $t_{PD}$ = 0.144 ns/in $C_O$ is then calculated as 2.075 pF/in. If it is assumed that an MC88100 or 88200 clock input load is 15 pF, and that two of these loads, in addition to a 7 pF FAST TTL load, are distributed along a 9.6 in clock trace,

$C_d$ = (2 x 15 + 7)pF/9.6 in = pF/in.

The loaded trace propagation delay and characteristic impedance are then calculated as

$t_{PD}$' = 0.243ns/in and $Z_O$' = 41 Ω.

Looking at trace C in Figure 2, the two MC88200's are approximately 3 inches apart. Using the calculated value of $t_{PD}$', the clock signal skew due to the trace is about 0.7 ns. Since these two devices are on the same trace, this is the total clock skew between these devices. Upon careful inspection of all the clock traces, it can be seen that clock signal skew was

accounted for and minimized on this board layout. The longest distance between any 88 K devices on a single clock trace is about 4.5 inches, which translates to approximately 1.1 ns of skew. The two 88 K devices farthest away from the clock driver (traces a and c), are located at almost exactly the same distance along their respective traces, making the clock skew between them the 1ns guaranteed from output to output of the clock driver. This means that the worst case clock skew between any two devices on this board is approximately 2.1 ns, which at 33 MHz is 7% of the period. Without careful attention to matching the clock traces on the board, this number could easily exceed 3 ns and the 10% cut-off point, even if a low skew clock driver is used.

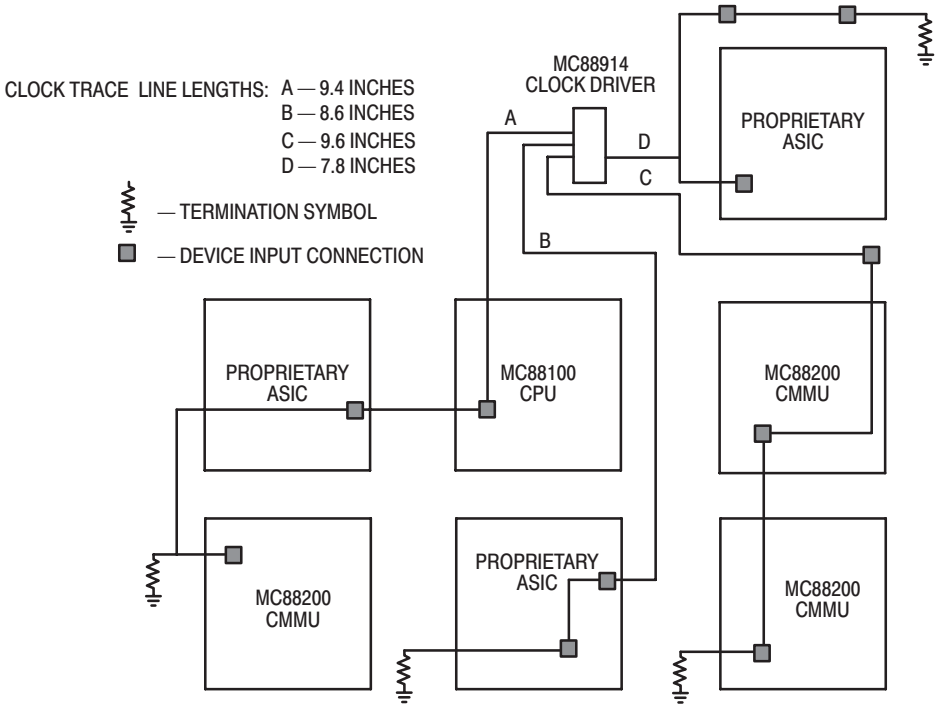
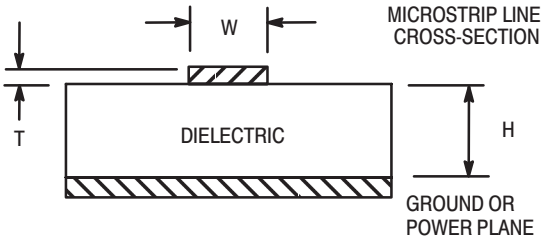



**Figure 2. Scale Representation of an Actual 88000 System PCB Layout**
(Only sections of the board related to the clock driver outputs are shown.)




$$Z_O = \frac{87}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right)$$

$$t_{pd} = 1.017 \sqrt{0.475\, e_r + 0.67} \text{ ns/ft}$$

WHERE:
$e_r$ = Relative Dielectric Constant of the Board Material
w, h, t = Dimensions Indicated in a Microstrip Diagram

**Figure 3. Formulas for the Characteristic Impedance and Propagation Delay of a Microstrip Line (Ref 1)**

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## CLOCK SIGNAL TERMINATIONS

Transmission line effects occur when a large mismatch is present between the characteristic impedance of the line and the input or output impedances of the receiving or driving device. The basic guidelines used to determine if a PCB trace needs to be examined for transmission line effects is that if the smaller of the driving device's rise or fall time is less than three times the propagation delay of a switching wave through a trace, the transmission line effects will be present.[2] This relationship can be stated in equation form as:[3]

$$3 \times t_{PD}' \times \text{trace length} \leq t_{RISE} \text{ or } t_{FALL}$$

For the MC88914 CMOS clock driver described in this article, rise and fall times are typically 1.5 ns or less (from 20% to 80% of $V_{CC}$). Analyzing the clock trace characteristics presented earlier for transmission line effects, 3 x 0.243 ns/in x trace length ≤1ns (1ns is used as 'fastest' rise or fall time). Therefore the trace length must be less than 1.5 inches for the transmission line effects to be masked by the rise and fall times.

Figure 4 shows the clock signal waveform seen at the receiver end of an unterminated 0.5 inch trace and an unterminated 9 inch trace. These results were obtained using SPICE simulations. which may not be exact, but are adequate to predict trends and for comparison purposes. The 9 inch trace, which is well beyond the 1.5 inch limit where transmission line effects come into play, exhibits unacceptable switching characteristics caused by reflections going back and forth on the trace. Even the 0.5 inch line exhibits substantial overshoot and undershoot. Any unterminated line will exhibit some overshoot and undershoot at these edge rates.

Clock lines shorter than 1-1.5 inches are unrealistic on a practical board layout, therefore it is recommended that CMOS clock lines be terminated if the driver has 1-2 ns edge rates. Termination, which is used to more closely match the line to the load or source impedances, has been a fact of life in the ECL world for many years (reference 1 is an excellent source for transmission line theory and practice in ECL systems), but CMOS and TTL devices have only recently reached the speeds and edge rates which require termination. CMOS outputs further complicate the issue by driving from rail to rail (5 V), with slew rates exceeding those of high performance ECL devices.

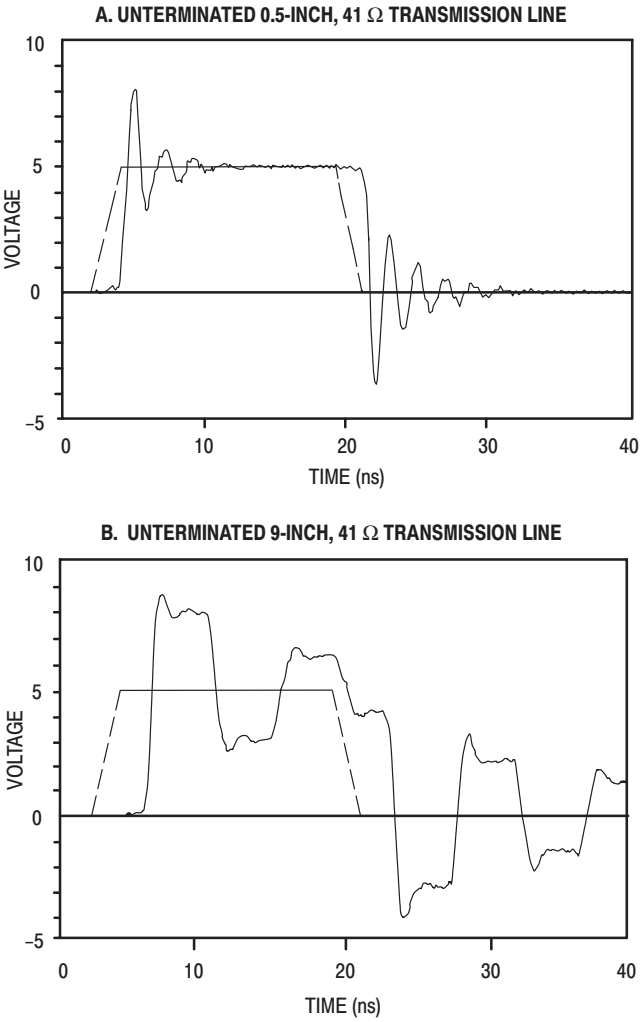


**Figure 4. SPICE Simulation Results of 'Short' and 'Long' Transmission Lines. Simulations Were Run with Typical Parameters @ 25°C and $V_{CC}$ = 5.0 V**

Since clock lines are only driven from a single location, they lend themselves to termination more easily than bus lines which are commonly driven from multiple locations. Termination of bus lines with multiple drivers is a complicated manner which will not be addressed in this article. The most common types of termination in digital systems are shown in Figure 5. Since no single termination scheme is optimal in all cases, the tradeoffs involving the use of each will be discussed, and recommendations specific to clock drivers will be made. Reference 2 is a comprehensive and practical treatment of transmission line theory and analysis of CMOS signals, and is recommended reading for those who want to gain a better understanding of transmission lines. Figure 6 shows SPICE simulated waveforms of the different termination schemes to be discussed. The driving device in the simulations was the MC88914 output buffer; in all simulations it drove a 9 inch 41 Ω transmission line. The simulations were run using typical model parameters at 25°C and $V_{CC}$ = 5 V.

Series termination, depicted in Figure 5b, is recommended if the load is lumped at the end of the trace and the output impedance of the driving device is less than the loaded characteristic impedance of the trace, or when a minimum number of components is required. The main problem with

series termination occurs when the driving device has different output impedance values in the low and high states, which is a problem in TTL and some CMOS devices. A well designed CMOS clock driver should have nearly equal output impedances in the high and low states, avoiding this problem. An additional advantage is that series termination does not create a DC current path, thus the $V_{OL}$ and $V_{OH}$ levels are not degraded. The SPICE generated waveforms of series termination in Figure 6a show that series termination effectively masks the transmission line effects exhibited in Figure 4. If each clock output is driving only one device, series termination would be recommended, but this is not a realistic case in most systems, so series termination is not generally recommended for termination of clock lines.

Parallel termination utilizes a single resistor tied to ground or $V_{CC}$ whose value is equal to the characteristic impedance of the line. Its major disadvantage is the DC current path it creates when the driver is in the high state (if the resistor is tied to ground). This causes excessive power dissipation and $V_{OH}$ level degradation. Since a clock driver output is always switching, the DC current draw argument loses some credibility at higher frequencies because the AC switching current becomes a major component of the overall current. Therefore the main consideration in parallel termination is how much $V_{OH}$ degradation can be tolerated by the receiving devices. Figure 6b demonstrates that this termination technique is effective in minimizing the switching noise, but Thevenin termination has some advantages over parallel termination.

Thevenin termination utilizes one resistor tied to ground and a second tied to $V_{CC}$. An important consideration when using this type of termination is choosing the resistor values to avoid settling of the voltage between the high and low logic levels of the receiving device.[2] TTL designers commonly use a 220/330 resistor value ratio, but CMOS is a little tricky because the switch point is at $V_{CC}/2$. With a 1:1 resistor ratio a failure at the driver output would cause the line to settle at 2.5 V, causing system debug problems and also potential damage to the receiving devices.

In Thevenin termination, the parallel equivalent value of the two resistors should be equal to the characteristic impedance of the line. A DC path does exist in both the high and low states, but it is not as bad as parallel termination because the resistance in the Thevenin DC path is at least 2 times greater.

Figure 6c shows the termination waveforms, which exhibit characteristics similar to parallel termination, but with less $V_{OH}$ degradation. The only real advantage of parallel over Thevenin is less resistors (1/2 as many) and less space taken up on the board by the resistors. If this is not a factor, Thevenin termination is recommended over parallel.

AC termination, shown in Figure 5e, normally utilizes a resistor and capacitor in series to ground. The capacitor blocks DC current flow, but allows the AC signal to flow to ground during switching. The RC time constant of the resistor and capacitor must be greater than twice the loaded line delay. AC termination is recommended because of its low power dissipation and also because of the availability of the resistor and capacitor in single-in-line packages (SIP). A pullup resistor to $V_{CC}$ is sometimes added to set the DC level at a certain point because of the failure condition described in regards to Thevenin termination. As discussed earlier, the argument of lower DC current is less convincing at high frequencies. The AC terminated waveform walks out slightly toward the end of a high-to-low or low-to-high transition as seen in Figure 6d, making it slightly less desirable than Thevenin termination.

Thevenin and AC termination are the two recommended termination schemes for clock lines, but it depends on what frequency the clock is running at when making a decision between these types of termination. Although hard data is not provided to back this statement up, it is a safe assumption that at frequencies of 25 MHz and below AC is the best choice. If the system frequency could reach 40 MHz and beyond, Thevenin becomes the better choice.

## ADDITIONAL CONSIDERATIONS WHEN TERMINATING CLOCK LINES

The results presented might imply that terminating the clock lines will completely solve noise problems, but termination can cause secondary problems with some logic devices. Termination acts to reduce the noise seen at the receiver, but that noise actually is seen as additional current and noise at the output of the driving device. If the internal and input logic on the source device is not sufficiently decoupled on chip from the high current outputs, internal threshold problems can occur. This phenomenon is commonly known as ‘dynamic threshold.’ It is usually evidenced by glitches appearing on the outputs of a fast, high current drive logic device as it switches high or low. This is most severe on ‘ACT’ devices which have high current and high slew rate CMOS outputs along with TTL inputs which have low noise immunity. This problem can be minimized by decoupling the internal ground and $V_{CC}$ supplies on-chip and in the package. This decoupling is accomplished by having separate ‘quiet’ ground and $V_{CC}$ pads on chip which supply the input circuitry’s ground and $V_{CC}$ references. These pads are then tied to extra ’quiet’ ground and ‘quiet’ $V_{CC}$ pins on the package, or to special ‘split leads’ which resemble a tuning fork and utilize the leadframe inductance to accomplish the decoupling. When choosing a clock source, make sure that the part has one of these decoupling schemes.

**References**

1. Blood, William R., *MECL System Design Handbook*, Motorola Inc., 1983.
2. Application Note AN1051, *Transmission Line Effects in PCB Applications*, Motorola Inc., 1990.
3. *Motorola FACT Data Book* DL138, Motorola Inc., 1990.

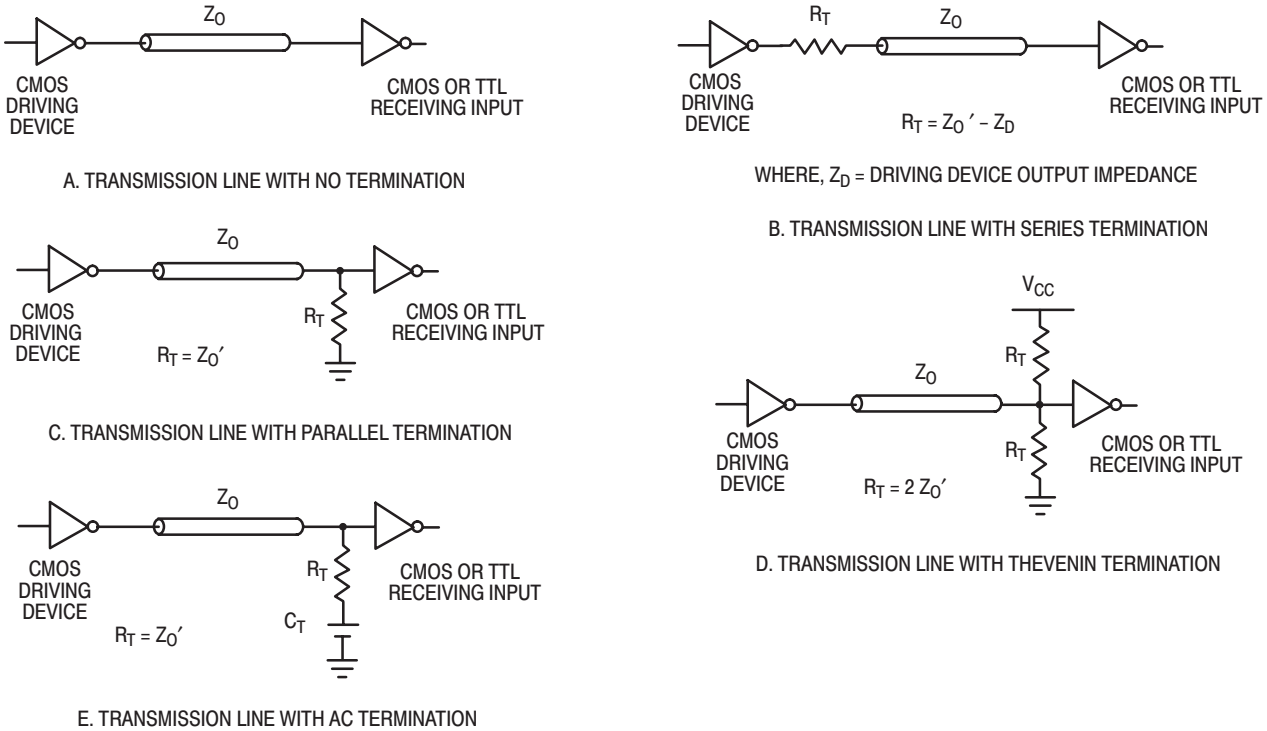


**Figure 5. Schematic Representation of Common Termination Techniques**

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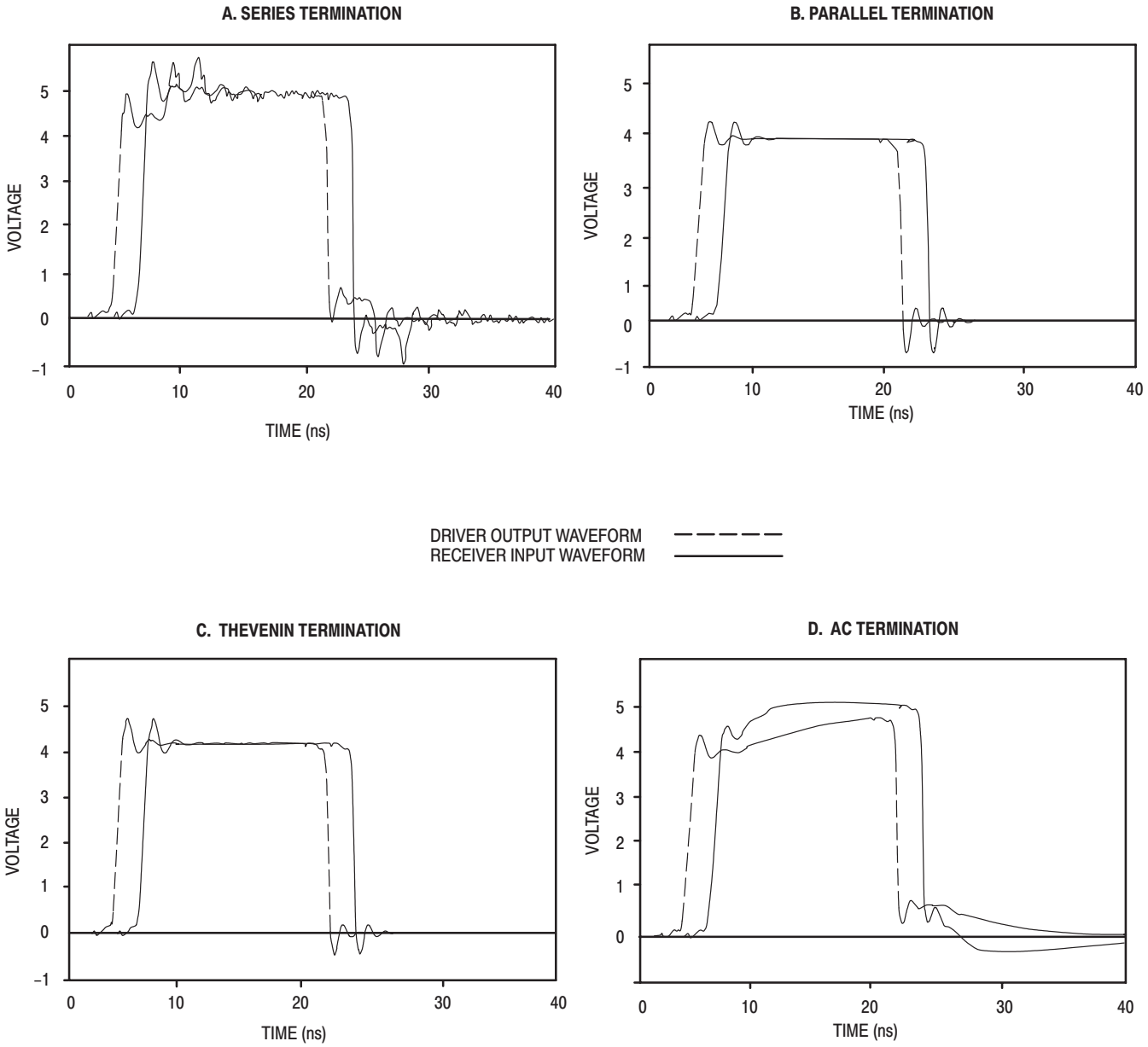


**Figure 6. SPICE Simulation Results for Various Terminations of a 9-Inch 41 Ω Transmission Line. Simulations Were Run with Typical Model Parameters @ 25°C and $V_{CC}$ = 5.0 V**

**Order Number: AN1405/D**
**Rev 1, 09/2001**

**AN1405**

# ECL Clock Distribution Techniques

**Prepared by: Todd Pearson**
**ECL Applications Engineering**

## Abstract

This application note provides information on system design using ECL logic technologies for reducing system clock skew over the alternative CMOS and TTL technologies.

## INTRODUCTION

The ever increasing performance requirements of today's systems has placed an even greater emphasis on the design of low skew clock generation and distribution networks. Clock skew, the difference in time between "simultaneous" clock transitions within a system, is a major component of the constraints which form the upper bound for the system clock frequency. Reductions in system clock skew allow designers to increase the performance of their designs without having to resort to more complicated architectures or more costly, faster logic. ECL logic technologies offer a number of advantages for reducing system clock skew over the alternative CMOS and TTL technologies.

## SKEW DEFINITIONS

The skew introduced by logic devices can be divided into three parts: duty cycle skew, output-to-output skew and part-to-part skew. Depending on the specific application, each of the three components can be of equal or overriding importance.

### Duty Cycle Skew

The duty cycle skew is a measure of the difference between the $T_{PLH}$ and $T_{PHL}$ propagation delays (Figure 1). Because differences in $T_{PLH}$ and $T_{PHL}$ will result in pulse width distortion the duty cycle skew is sometimes referred to as pulse skew. Duty cycle skew is important in applications where timing operations occur on both edges or when the duty cycle of the clock signal is critical. The later is a common requirement when driving the clock inputs of advanced microprocessors.

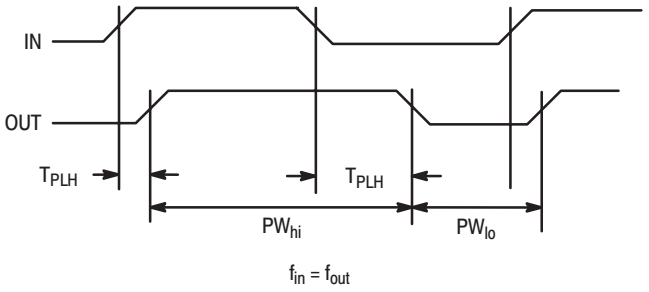


**Figure 1. Duty Cycle Skew**

### Output-to-Output Skew

Output-to-output skew is defined as the difference between the propagation delays of all the outputs of a device. A key constraint on this measurement is the requirement that the output transitions are identical, therefore if the skew between all edges produced by a device is important the output-to-output skew would need to be added to the duty cycle skew to get the total system skew. Typically the output-to-output skew will be smaller than the duty cycle skew for TTL and CMOS devices. Because of the near zero duty cycle skew of a differential ECL device the output-to-output skew will generally be larger. The output-to-output skew is important in systems where either a single device can provide all of the necessary clocks or for the first level device of a nested clock distribution tree. In these two situations the only parameter of importance will be the relative position of each output with respect to the other outputs on that die. Since these outputs will all see the same environmental and process conditions the skew will be significantly less than the propagation delay windows specified in the standard device data sheet.

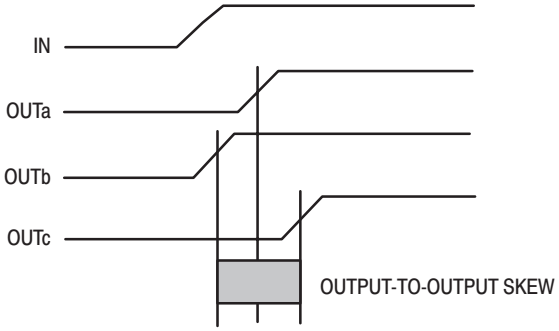


**Figure 2. Output-to-Output Skew**

### Part-to-Part Skew

The part-to-part skew specification is by far the most difficult performance aspect of a device to minimize. Because the part-to-part skew is dependent on both process variations and variations in the environment the resultant specification is significantly larger than for the other two components of skew. Many times a vendor will provide subsets of part-to-part skew specifications based on non-varying environmental conditions. Care should be taken in reading data sheets to fully understand the conditions under which the specified limits are guaranteed. If the part-to-part skew is specified and is different than the specified propagation delay window for the device one can be assured there are constraints on the part-to-part skew specification.

Power supply and temperature variations are major contributors to variations in propagation delays of silicon devices. Constraints on these two parameters are commonly seen in part-to-part skew specifications. Although there are situations where the power supply variations could be ignored, it is difficult for this author to perceive of a realistic system whose devices are all under identical thermal conditions. Hot spots on boards

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or cabinets, interruption in air flow and variations in IC density of a board all lead to thermal gradients within a system. These thermal gradients will guarantee that devices in various parts of the system are under different junction temperature conditions. Although it is unlikely that a designer will need the entire commercial temperature range, a portion of this range will need to be considered. Therefore, a part-to-part skew specified for a single temperature is of little use, especially if the temperature coefficient of the propagation delay is relatively large.

For designs whose clock distribution networks lie on a single board which utilizes power and ground planes an assumption of non-varying power supplies would be a valid assumption and a specification limit for a single power supply would be valuable. If, however, various pieces of the total distribution tree will be on different boards within a system there is a very real possibility that each device will see different power supply levels. In this case a specification limit for a fixed $V_{CC}$ will be inadequate for the design of the system. Ideally the data sheets for clock distribution devices should include information which will allow designers to tailor the skew specifications of the device to their application environment.

## SYSTEM ADVANTAGES OF ECL

### Skew Reductions

ECL devices provide superior performance in all three areas of skew over their TTL or CMOS competitors. A skew reducing mechanism common to all skew parameters is the faster propagation delays of ECL devices. Since, to some extent, all skew represent a percentage of the typical delays faster delays will usually mean smaller skews. ECL devices, especially clock distribution devices, can be operated in either single-ended or differential modes. To minimize the skew of these devices the differential mode of operation should be used, however even in the single-ended mode the skew performance will be significantly better than for CMOS or TTL drivers.

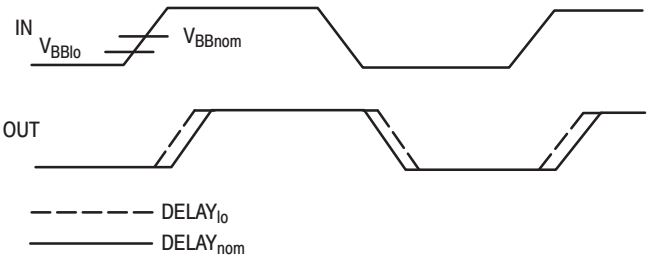


**Figure 3. $V_{BB}$ Induced Duty Cycle Skew**

ECL output buffers inherently show very little difference between $T_{PLH}$ and $T_{PHL}$ delays. What differences one does see are due mainly to switching reference levels which are not ideally centered in the input swing (see Figure 3). For worst case switching reference levels the pulse skew of an ECL device will still be less than 300 ps. If the ECL device is used differentially the variation in the switching reference will not impact the duty cycle skew as it is not used. In this case the pulse skew will be less than 50 ps and can generally be ignored in all but the highest performance designs. The problem of generating clocks which are capable of meeting the duty cycle requirements of the most advanced microprocessors, would be a trivial task if differential ECL compatible clock inputs were used. TTL and CMOS clock drivers on the other hand have inherent differences between the $T_{PLH}$ and $T_{PHL}$ delays in addition to the problems with non-centered switching thresholds. In devices specifically designed to minimize this parameter it generally cannot be guaranteed to anything less than 1ns.

The major contributors to output-to-output skew is IC layout and package choice. Differences in internal paths and paths through the package generally can be minimized regardless of the silicon technology utilized at the die level, therefore ECL devices offer less of an advantage in this area than for other skew parameters. CMOS and TTL output performance is tied closely to the power supply levels and the stability of the power busses within the chip. Clock distribution trees by definition always switch simultaneously, thus creating significant disturbances on the internal power busses. To alleviate this problem multiple power and ground pins are utilized on TTL and CMOS clock distribution devices. However even with this strategy TTL and CMOS clock distribution devices are limited to 500 ps – 700 ps output-to-output skew guarantees. With differential ECL outputs very little if any noise is generated and coupled onto the internal power supplies. This coupled with the faster propagation delays of the output buffers produces output-to-output skews on ECL clock chips as low as 50 ps.

Two aspects of ECL clock devices will lead to significantly smaller part-to-part skews than their CMOS and TTL competitors: faster propagation delays and delay insensitivity to environmental variations. Variations in propagation delays with process are typically going to be based on a percentage of the typical delay of the device. Assuming this percentage is going to be approximately equivalent between ECL, TTL and CMOS processes, the faster the device the smaller the delay variations. Because state-of-the-art ECL devices are at least 5 times faster than TTL and CMOS devices, the expected delay variation would be one fifth those of CMOS and TTL devices without even considering environmental dependencies.

The propagation delays of an ECL device are insensitive to variations in power supply while CMOS and TTL device propagation delays vary significantly with changes in this parameter. Across temperature the percentage variation for all technologies is comparable, however, again the faster propagation delays of ECL will reduce the magnitude of the variation. Figure 4 on the following page represents normalized propagation delay versus temperature and power supply for the three technologies.

### Low Impedance Line Driving

The clock requirements of today's systems necessitate an almost exclusive use of controlled impedance interconnect. In the past this requirement was unique to the performance levels associated with ECL technologies, and in fact precluded its use in all but the highest performance systems. However the high performance CMOS and TTL clock distribution chips now require care in the design and layout of PC boards to optimize their performance, with this criteria established the migration from these technologies to ECL is simplified. In fact, the difficulties involved in designing with these "slower" technologies in a controlled impedance environment may even enhance the potential of using ECL devices as they are ideally suited to the task.

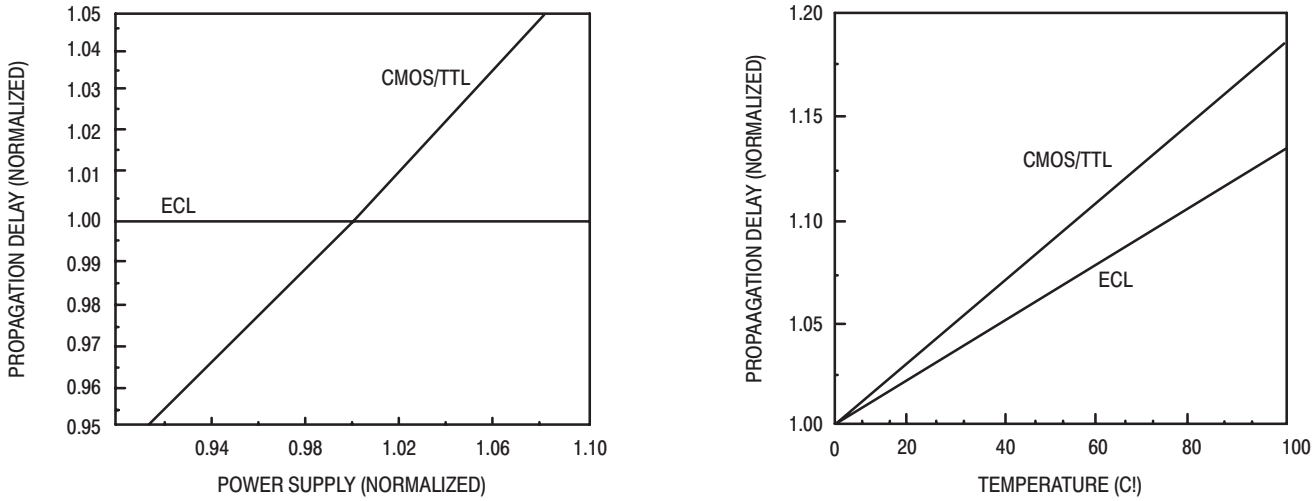


**Figure 4. $T_{PD}$ vs Environmental Condition Comparison**

The low impedance outputs and high impedance inputs of an ECL device are ideal for driving 50 Ω to 130 Ω controlled impedance transmission lines. The specified driving impedance of ECL is 50 Ω, however this value is used only for convenience sake due to the 50 Ω impedance of most commonly used measurement equipment. Utilizing higher impedance lines will reduce the power dissipated by the termination resistors and thus should be considered in power sensitive designs. The major drawback of higher impedance lines (delays more dependent on capacitive loading) may not be an issue in the point to point interconnect scheme generally used in low skew clock distribution designs.

**Differential Interconnect**

The device skew minimization aspects of differential ECL have already been discussed however there are other system level advantages that should be mentioned. Whenever clock lines are distributed over long distances the losses in the line and the variations in power supply upset the ideal relationship between input voltages and switching thresholds. Because differential interconnect "carries" the switching threshold information from the source to the load the relationship between the two is less likely to be changed. In addition for long lines the smaller swings of an ECL device produce much lower levels of cross-talk between adjacent lines and minimizes EMI radiation from the PC board.

There is a cost associated with fully differential ECL, more pins for equivalent functions and more interconnect to be laid on a typically already crowded PC board. The first issue is really a non-issue for clock distribution devices. The output-to-output and duty cycle skew are very much dependent on quiet internal power supplies. Therefore the pins sacrificed for the complimentary outputs would otherwise have to be used as power supply pins, thus functionality is actually gained for an equivalent pin count as the inversion function is also available on a differential device. The presence of the inverted signal could be invaluable for a design which clocks both off the positive and negative edges. Figure 5 shows a method of obtaining very low skew (<50 ps) 180° shifted two phase clocks.

It is true that differential interconnect requires more signals to be routed on the PC board. Fortunately with the wide data and address buses of today's designs the clock lines represent a small fraction of the total interconnect. The final choice as to whether or not to use differential interconnect lies in the level of skew performance necessary for the design. It should be noted that although single-ended ECL provides less attractive skew performance than differential ECL, it does provide significantly better performance than equivalent CMOS and TTL functions.

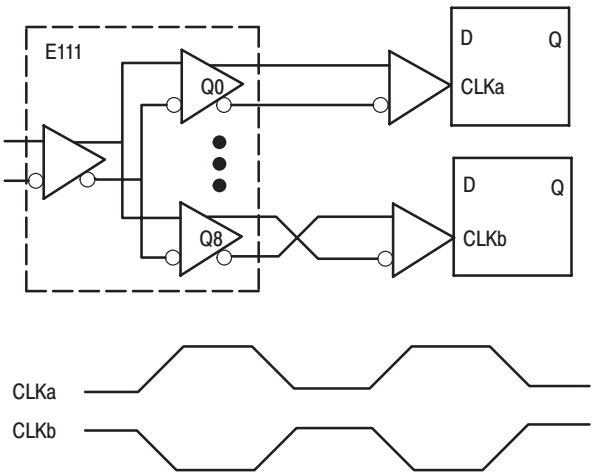


**Figure 5. 180° Shifted Two Phase Clocks**

## USING ECL WITH POSITIVE SUPPLIES

It is hard to argue with the clock distribution advantages of ECL presented thus far, but it may be argued that except for all ECL designs it is too costly to include ECL devices in the distribution tree. This claim is based on the assumption that at least two extra power supplies are required; the negative $V_{EE}$ supply and the negative $V_{TT}$ termination voltage. Fortunately both these assumptions are false. PECL (Positive ECL) is an acronym which describes using ECL devices with a positive rather than negative power supply. It is important to understand that all ECL devices are also PECL devices. By using ECL devices as PECL devices on a +5 volt supply and incorporating termination techniques which do not require a separate termination voltage (series termination, thevenin equivalent) ECL can be incorporated in a CMOS or TTL design with no added cost.

The reason for the choice of negative power supplies as standard for ECL is due to the fact that all of the output levels and internal switching bias levels are referenced to the $V_{CC}$ rail. It is generally easier to keep the grounds quieter and equal potential throughout a system than it is with a power supply. Because the DC parameters are referenced to the $V_{CC}$ rail any disturbances or voltage drops seen on $V_{CC}$ will translate 1:1 to the output and internal reference levels. For this reason when communicating with PECL between two boards it is recommended that only differential interconnect be used. By using differential interconnect $V_{CC}$ variations within the specified range will not in any way affect the performance of the device.

Finally mentioning ECL to a CMOS designer invariably conjures up visions of space heaters as their perception of ECL is high power. Although it is true that the static power of ECL is higher than for CMOS the dynamic power differences between the technologies narrows as the frequency increases. As can be seen in Figure 6 at frequencies as low as 20 MHz the per gate power of ECL is actually less than for CMOS. Since clock distribution devices are never static it does not make sense to compare the power dissipation of the two technologies in a static environment.

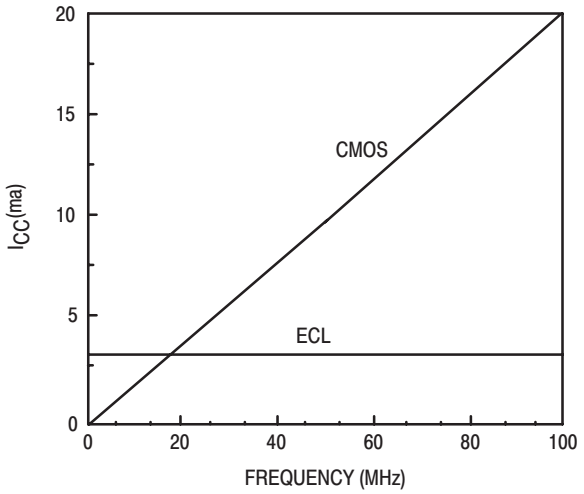


**Figure 6. ICC/Gate vs Frequency Comparison**

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## MIXED SIGNAL CLOCK DISTRIBUTION

### ECL Clock Distribution Networks

Clock distribution in a ECL system is a relatively trivial matter. Figure 7 illustrates a two level clock distribution tree which produces nine differential ECL clocks on six different cards. The ECLinPS E211 device gives the flexibility of disabling each of the cards individually. In addition the synchronous registered enables will disable the device only when the clock is already in the LOW state, thus avoiding the problem of generating runt pulses when an asynchronous disable is used. The device also provides a muxed clock input for incorporating a high speed system clock and a lower speed test or scan clock within the same distribution tree. The ECLinPS E111 device is used to receive the signals from the backplane and distribute it on the card. The worst case skew between all 54 clocks in this situation would be 275 ps assuming that all the loads and signal traces are equalized.

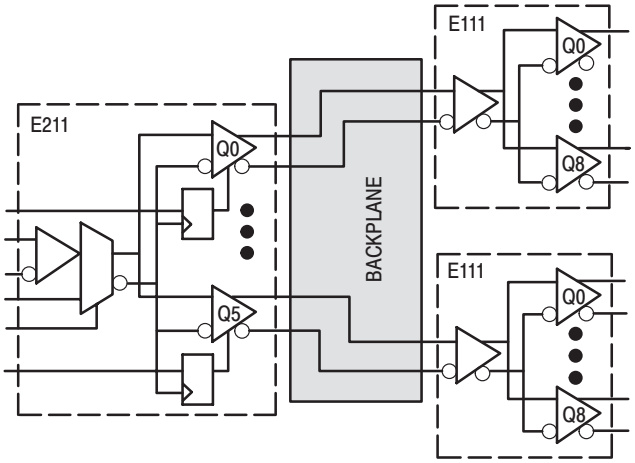


**Figure 7. ECL Clock Distribution Tree**

### Mixed Technology Distribution Networks

Building clock networks in TTL and CMOS systems can be a little more complicated as there are more alternatives available. For simple one level distribution trees fanout devices like the MECL 10H645 1:9 TTL to TTL fanout tree can be used. However as the number of levels of fanout increases the addition of ECL devices in an other wise TTL or CMOS system becomes attractive. In Figure 8 on the next page an E111 device is combined with a MECL H641 device to produce 81 TTL level clocks. Analyzing the skew between the 81 clocks yields a worst case skew, allowing for the full temperature and $V_{CC}$ range variation, of 1.25 ns. Under ideal situations, no variation in temperature or $V_{CC}$ supply, the skew would be only 750 ps. When compared with distribution trees utilizing only TTL or CMOS technologies these numbers represent ≈50% improvement, more if the environmental conditions vary to any degree. For a 50 MHz clock the total skew between the 81 TTL clocks is less than 6.5% of the clock period, thus providing the designer extra margin for layout induced skew to meet the overall skew budget of the design.

Many designers have already realized the benefits of ECL clock distribution trees and thus are implementing them in their designs. Furthermore where they have the capability, i.e. ASICs, they are building their VLSI circuits with ECL compatible clock inputs. Unfortunately other standard VLSI circuits such as microprocessors, microprocessor support chips and memory still cling to TTL or CMOS clock inputs. As a result many systems need both ECL and TTL clocks within the same system. Unlike the situation outlined in Figure 8 the ECL levels are not merely intermediate signals but rather are driving the clock inputs of the logic. As a result the ECL edges need to be matched with the TTL edges as pictured in Figure 9.

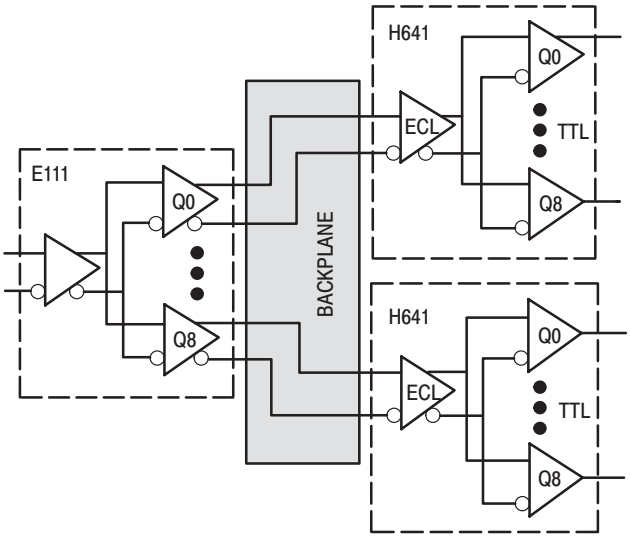


**Figure 8. ECL to TTL Clock Distribution**

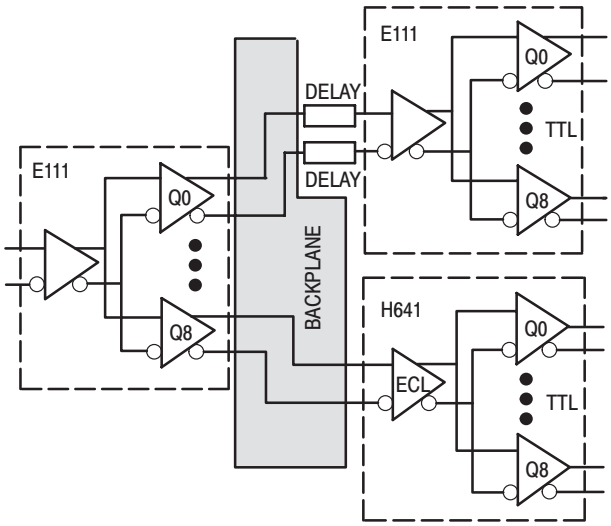


**Figure 9. Mixed ECL and TTL Distribution**

An ECL clock driver will be significantly faster than a TTL or CMOS equivalent function. Therefore to de-skew the ECL and TTL signals of Figure 9 a delay needs to be added to the input of the ECL device. Because a dynamic delay adjust would not lend itself to most production machines a static delay would be used. The value of the delay element would be a best guess estimate of the differences in the two propagation delays. It is highly unlikely that the temperature coefficients of the propagation delays of the ECL devices, TTL devices and delay devices would be equal. Although these problems will add skew to the system, the resultant total skew of the distribution network will be less than if no ECL chips were used.

**PLL Based Clock Drivers**

A potential solution for the problem outlined in Figure 9 is in the use of phase locked loop based clock distribution chips. Because these devices feedback an output and lock it to a reference clock input the delay differences between the various technology output buffers will be eliminated. One might believe that with all of the euphoria surrounding the performance of PLL based clock distribution devices that the need for any ECL in the distribution tree will be eliminated. However when analyzed further the opposite appears to be the case.

For a single board design with a one level distribution system there obviously is no need for ECL. When, however, a multiple board system is required where nested levels of devices are needed ECL once again becomes useful. One major aspect of part-to-part skew for PLL based clock chips often overlooked is the dependence on the skew of the various reference clocks being locked to. As can be seen in Figure 10 the specified part-to-part skew of the device would necessarily need to be added to the reference clock skew to get the overall skew of the clock tree. From the arguments presented earlier this skew will be minimized if the reference clock is distributed in ECL. It has not been shown as of yet where a PLL based ECL clock distribution chip can provide the skew performance of the simple fanout buffer. From a system standpoint the buffer type circuits are much easier to design with and thus given equivalent performance would represent the best alternative. The extra features provided by PLL based chips could all be realized if they were used in only the final stage of the distribution tree.

The MPC973 is a PLL based clock driver which features differential PECL reference clock inputs. When combined with the very low skew MC10E111 fanout buffer, very low skew clock trees can be realized for multiprocessor MPP designs. There will be a family of devices featuring various technology compatible inputs and outputs to allow for the building of precisely aligned clock trees based on either ECL, TTL, CMOS or differential GTL (or a mixture of all four) compatible levels.

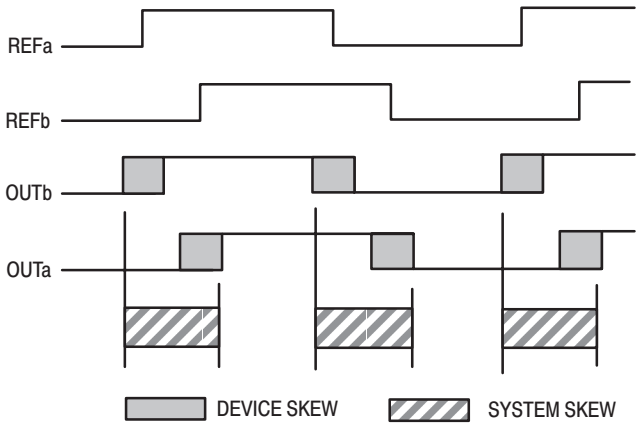


**Figure 10. System Skew For PLL Clock Distribution**

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## Conclusion

The best way to maximize the performance of any synchronous system is to spend the entire clock period performing value added operations. Obviously any portion of the clock period spent idle due to clock skew limits the potential performance of the system. Using ECL technology devices in clock distribution networks will minimize all aspects of skew and thus maximize the performance of a system. Unfortunately the VLSI world is not yet ECL clock based so that the benefits of a totally ECL based distribution tree cannot be realized for many systems. However there are methods of incorporating ECL into the intermediate levels of the tree to significantly reduce the overall skew. In addition the system designers can utilize their new found knowledge to incorporate ECL compatible clocks on those VLSI chips of which they have control while at the same time pressuring other VLSI vendors in doing the same so that future designs can enjoy fully the advantages of distributing clocks with ECL.

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**AN1406**

# Designing With PECL (ECL at +5.0 V)

## The High Speed Solution for the CMOS/TTL Designer

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### ABSTRACT

This application note provides detailed information on designing with Positive Emitter Coupled Logic (PECL) devices.

### INTRODUCTION

PECL, or Positive Emitter Coupled Logic, is nothing more than standard ECL devices run off of a positive power supply. Because ECL, and therefore PECL, has long been the “black magic” of the logic world many misconceptions and falsehoods have arisen concerning its use. However, many system problems which are difficult to address with TTL or CMOS technologies are ideally suited to the strengths of ECL. By breaking through the wall of misinformation concerning the use of ECL, the TTL and CMOS designers can arm themselves with a powerful weapon to attack the most difficult of high speed problems.

It has long been accepted that ECL devices provide the ultimate in logic speed; it is equally well known that the price for this speed is a greater need for attention to detail in the design and layout of the system PC boards. Because this requirement stems only from the speed performance aspect of ECL devices, as the speed performance of any logic technology increases these same requirements will hold. As can be seen in Table 1 the current state–of–the–art TTL and CMOS logic families have attained performance levels which require controlled impedance interconnect for even relatively short distances between source and load. As a result system designers who are using state–of–the–art TTL or CMOS logic are already forced to deal with the special requirements of high speed logic; thus it is a relatively small step to extend their thinking from a TTL and CMOS bias to include ECL devices where their special characteristics will simplify the design task.

**Table 1. Relative Logic Speeds**

| Logic Family | Typical Output Rise/Fall | Maximum Open Line Length ($L_{max}$)* |
|---|---|---|
| 10KH | 1.0 ns | 3” |
| ECLinPS | 400 ps | 1” |
| FAST | 2.0 ns | 6” |
| FACT | 1.5 ns | 4” |

* Approximate for stripline interconnect ($L_{max} = T_r/2T_{pd}$)

### SYSTEM ADVANTAGES OF ECL

The most obvious area to incorporate ECL into an otherwise CMOS/TTL design would be for a subsystem which requires very fast data or signal processing. Although this is the most obvious it may also be the least common. Because of the need for translation between ECL and CMOS/TTL technologies the performance gain must be greater than the overhead required to translate back and forth between technologies. With typical delays of six to seven nanoseconds for translating between technologies, a significant portion of the logic would need to be realized using ECL for the overall system performance to improve. However, for very high speed subsystem requirements ECL may very well provide the best system solution.

#### Transmission Line Driving

Many of the inherent features of an ECL device make it ideal for driving long, controlled impedance lines. The low impedance of the open emitter outputs and high input impedance of any standard ECL device make it ideally suited for driving controlled impedance lines. Although designed to drive 50 Ω lines an ECL device is equally adept at driving lines of impedances of up to 130 Ω without significant changes in the AC characteristics of the device. Although some of the newer CMOS/TTL families have the ability to drive 50 Ω lines many require special driver circuits to supply the necessary currents to drive low impedance transmission interconnect. In addition the large output swings and relatively fast output slew rates of today’s high performance CMOS/TTL devices exacerbate the problems of crosstalk and EMI radiation. The problems of crosstalk and EMI radiation, along with common mode noise and signal amplitude losses, can be alleviated to a great degree with the use of differential interconnect. Because of their architectures, neither CMOS nor TTL devices are capable of differential communication. The differential amplifier input structure and complimentary outputs of ECL devices make them perfectly suited for differential applications. As a result, for systems requiring signal transmission between several boards, across relatively large distances, ECL devices provide the CMOS/TTL designer a means of ensuring reliable transmission while minimizing EMI radiation and crosstalk.

Figure 1 shows a typical application in which the long line driving, high bandwidth capabilities of ECL can be utilized. The majority of the data processing is done on wide bit width words with a clock cycle commensurate with the bandwidth capabilities of CMOS and TTL logic. The parallel data is then serialized into a high bandwidth data stream, a bandwidth which requires ECL technologies, for transmission across a long line to another box or machine. The signal is received differentially and converted back to relatively low speed parallel data where it can be processed further in CMOS/TTL logic. By taking advantage of the bandwidth and line driving capabilities of ECL the system minimizes the number of lines required for interconnecting the subsystems without sacrificing the overall performance. Furthermore by taking advantage of PECL this application can be realized with a single five volt power supply. The configuration of Figure 1 illustrates a situation where the mixing of logic

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technologies can produce a design which maximizes the overall performance while managing power dissipation and minimizing cost.

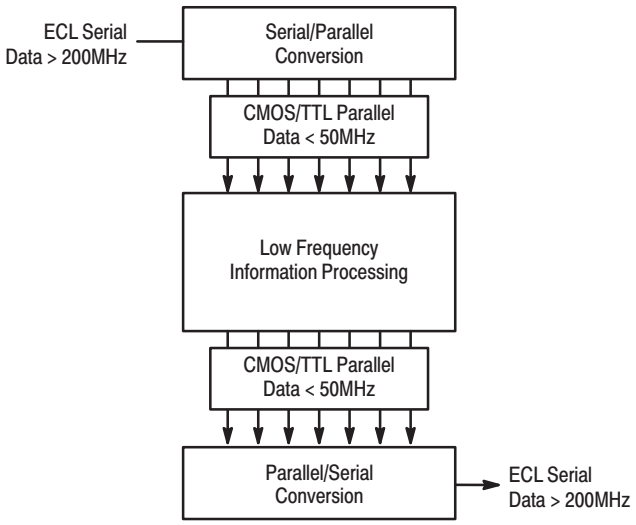



**Figure 1. Typical Use of ECL's High Bandwidth, Line Driving Capabilities**

**Clock Distribution**

Perhaps the most attractive area for ECL in CMOS/ TTL designs is in clock distribution. The ever increasing performance capabilities of today's designs has placed an even greater emphasis on the design of low skew clock generation and distribution networks. Clock skew, the difference in time between "simultaneous" clock transitions throughout an entire system, is a major component of the constraints which form the upper bound for the system clock frequency. Reductions in system clock skew allow designers to increase the performance of their designs without having to resort to more complicated architectures or costly, faster logic. ECL logic has the capability of significantly reducing the clock skew of a system over an equivalent design utilizing CMOS or TTL technologies.

The skew introduced by a logic device can be broken up into three areas; the part–to–part skew, the within–part skew and the rise–to–fall skew. The part–to–part skew is defined as the differences in propagation delays between any two devices while the within–device skew is the difference between the propagation delays of similar paths for a single device. The final portion of the device skew is the rise–to–fall skew or simply the differences in propagation delay between a rising input and a failing input on the same gate. The within–device skew and the rise–to–fall skew combine with delay variations due to environmental conditions and processing to comprise the part–to–part skew. The part–to–part skew is defined by the propagation delay window described in the device data sheets.

Careful attention to die layout and package choice will minimize within–device skew. Although this minimization is independent of technology, there are other characteristics of ECL which will further reduce the skew of a device. Unlike their CMOS/TTL counterparts, ECL devices are relatively insensitive to variations in supply voltage and temperature. Propagation delay variations with environmental conditions must be accounted for in the specification windows of a device. As a result because of ECLs AC stability the delay windows for a device will inherently be smaller than similar CMOS or TTL functions.

The virtues of differential interconnect in line driving have already been addressed, however the benefits of differential interconnect are even more pronounced in clock distribution. The propagation delay of a signal through a device is intimately tied to the switching threshold of that device. Any deviations of the threshold from the center of the input voltage swing will increase or decrease the delay of the signal through the device. This difference will manifest itself as rise–to–fall skew in the device. The threshold levels for both CMOS and TTL devices are a function of processing, layout, temperature and other factors which are beyond the control of the system level designer. Because of the variability of these switching references, specification limits must be relaxed to guarantee acceptable manufacturing yields. The level of relaxation of these specifications increases with increasing logic depth. As the depth of the logic within a device increases the input signal will switch against an increasing number of reference levels; each encounter will add skew when the reference level is not perfectly centered. These relaxed timing windows add directly to the overall system skew. Differential ECL, both internal and external to the die, alleviates this threshold sensitivity as a DC switching reference is no longer required. Without the need for a switching reference the delay windows, and thus system skew, can be significantly reduced while maintaining acceptable manufacturing yields.

What does this mean to the CMOS/TTL designer? It means that CMOS/TTL designers can build their clock generation card and backplane clock distribution using ECL. Designers will not only realize the benefits of driving long lines with ECL but will also be able to realize clock distribution networks with skew specs unheard of in the CMOS/TTL world. Many specialized functions for clock distribution are available from Motorola (MC10/100E111, MC10/100E211, MC10/100EL11). Care must be taken that all of the skew gained using ECL for clock distribution is not lost in the process of translating into CMOS/TTL levels. To alleviate this problem the MC10/100H646 can be used to translate and fanout a differential ECL input signal into TTL levels. In this way all of the fanout on the backplane can be done in ECL while the fanout on each card can be done in the CMOS/TTL levels necessary to drive the logic.

Figure 2 illustrates the use of specialized fanout buffers to design a CMOS/TTL clock distribution network with minimal skew. With 50ps output–to–output skew of the MC10/100E111 and 1ns part–to–part skew available on the MC10/100H646 or MC10/100H641, a total of 72 or 81 TTL clocks, respectively, can be generated with a worst case skew between all outputs of only 1.05 ns. A similar distribution tree using octal CMOS or TTL buffers would result in worst case skews of more than 6ns. This 5 ns improvement in skew equates to about 50% of the up/down time of a 50MHz clock cycle. It is not difficult to imagine situations where an extra 50% of time to perform necessary operations would be either beneficial or even a life saver. For more information about using ECL for clock distribution, refer to application note AN1405/D – ECL Clock Distribution Techniques.

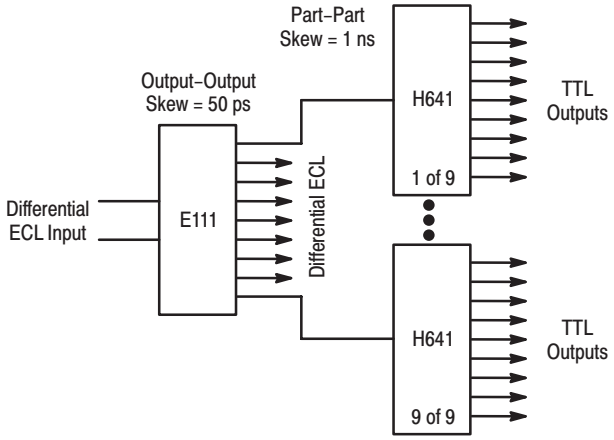



**Figure 2. Low Skew Clock Fanout Tree**

## PECL VERSUS ECL

Nobody will argue that the benefits presented thus far are not attractive, however the argument will be made that the benefits are not enough to justify the requirements of including ECL devices in a predominantly CMOS/TTL design. After all the inclusion of ECL requires two additional negative voltage supplies; $V_{EE}$ and the terminating voltage $V_{TT}$. Fortunately this is where the advantages of PECL come into play. By using ECL devices on a positive five volt CMOS/TTL power supply and using specialized termination techniques ECL logic can be incorporated into CMOS/TTL designs without the need for additional power supplies. What about power dissipation you ask, although it is true that in a DC state ECL will typically dissipate more power than a CMOS/TTL counterpart, in applications which operate continually at frequency, i.e.. clock distribution, the disparity between ECL and CMOS/TTL power dissipation is reduced. The power dissipation of an ECL device remains constant with frequency while the power of a CMOS/TTL device will increase with frequency. As frequencies approach 50MHz the difference between the power dissipation of a CMOS or TTL gate and an ECL gate will be minimal. 50MHz clock speeds are becoming fairly common in CMOS/TTL based designs as today's high performance MPUs are fast approaching these speeds. In addition, because ECL output swings are significantly less than those of CMOS and TTL the power dissipated in the load will be significantly less under continuous AC conditions.

It is clear that PECL can be a powerful design tool for CMOS/TTL designers, but where can one get these PECL devices. Perhaps the most confusing aspect of PECL is the misconception that a PECL device is a special adaptation of an ECL device. In reality *every* ECL device is also a PECL device; there is nothing magical about the negative voltage supply used for ECL devices. The only real requirement of the power supplies is that the potential difference described in the device data sheets appears across the upper and lower power supply rails ($V_{CC}$ and $V_{EE}$ respectively). A potential stumbling block arises in the specified $V_{EE}$ levels for the various ECL families. The 10 H and 100 K families specify parametric values for potential differences between $V_{CC}$ and $V_{EE}$ of 4.94 V to 5.46 V and 4.2 V to 4.8 V respectively; this poses a problem for the CMOS/TTL designer who works with a typical $V_{CC}$ of 5.0V ±5%. However, because both of these ECL standards are voltage compensated both families will operate perfectly fine and meet all of the performance specifications when operated on standard CMOS/TTL power supplies. In fact, Motorola is extending the $V_{EE}$ specification ranges of many of their ECL families to be compatible with standard CMOS/TTL power supplies. Unfortunately earlier ECL families such as MECL 10 K™ are not voltage compensated and therefore any reduction in the potential difference between the two supplies will result in an increase in the $V_{OL}$ level, and thus a decreased noise margin. For the typical CMOS/TTL power supplies a 10 K device will experience an ≈50 mV increase in the $V_{OL}$ level. Designers should analyze whether this loss of noise margin could jeopardize their designs before implementing PECL formatted 10 K using 5.0 V ± 5% power supplies.

The traditional choice of a negative power supply for ECL is the result of the upper supply rail being used as the reference for the I/0 and internal switching bias levels of the technology. Since these critical parameters are referenced to the upper rail any noise on this rail will couple 1:1 onto them; the result will be reduced noise margins in the design. Because, in general, it is a simpler task to keep a ground rail relatively noise free, it is beneficial to use the ground rail as this reference. However when careful attention is paid to the power supply design, PECL can be used to optimize system performance. Once again the use of differential PECL will simplify the designer's task as the noise margins of the system will be doubled and any noise riding on the upper $V_{CC}$ rail will appear as common mode noise; common mode noise will be rejected by the differential receiver.

## MECL TO PECL DC LEVEL CONVERSION

Although using ECL on positive power supplies is feasible, as with any high speed design there are areas in which special attention should be placed. When using ECL devices with positive supplies the input output voltage levels need to be translated. This translation is a relatively simple task. Since these levels are referenced off of the most positive rail, $V_{CC}$, the following equation can be used to calculate the various specified DC levels for a PECL device:

$$\text{PECL Level} = V_{CCNEW} - |\text{Specification Level}|$$

As an example, the $V_{OHMAX}$ level for a 10H device operating with a $V_{CC}$ of 5.0 V at 25°C would be as follows:

$$\text{PECL Level} = 5.0\text{ V} - |-0.81\text{ V}|$$
$$\text{PECL Level} = (5.0 - 0.81)\text{V} = 4.19\text{ V}$$

The same procedure can be followed to calculate all of the DC levels, including $V_{BB}$ for any ECL device. Table 2, on page 660, outlines the various PECL levels for a $V_{CC}$ of 5.0V for both the 10H and 100K ECL standards. As mentioned earlier any changes in $V_{CC}$ will show up 1:1 on the output DC levels. Therefore any tolerance values for $V_{CC}$ can be transferred to the device I/0 levels by simply adding or subtracting the $V_{CC}$ tolerance values from those values provided in Table 2.

## PECL TERMINATION SCHEMES

PECL outputs can be terminated in all of the same ways standard ECL, this would be expected since an ECL and a PECL device are one in the same. Figure 3 illustrates the various output termination schemes utilized in typical ECL systems. For best performance the open line technique in Figure 3 would not be used except for very short interconnect between devices; the definition of short can be found in the various design guides for the different ECL families. In general

for the fastest performance and the ability to drive distributive loads the parallel termination techniques are the best choice. However occasions may arise where a long uncontrolled or variable impedance line may need to be driven; in this case the series termination technique would be appropriate. For a more thorough discourse on when and where to use the various termination techniques the reader is referred to the MECL System Design Handbook (HB205/D) and the design guide in the ECLinPS Databook (DL140/D). The parallel termination scheme of Figure 3 requires an extra $V_{TT}$ power supply for the impedance matching load resistor. In a system which is built mainly in CMOS/TTL this extra power supply requirement may prohibit the use of this technique. The other schemes of Figure 3 use only the existing positive supply and ground and thus may be more attractive for the CMOS/ TTL based machine.

**Table 2. ECL/PECL DC Level Conversion for $V_{CC}$ = 5.0V**

| | 10E Characteristics | | | | | | 100E Characteristics | | |
|---|---|---|---|---|---|---|---|---|---|
| | 0°C | | 25°C | | 85°C | | 0 to 85°C | | |
| Symbol | Min | Max | Min | Max | Min | Max | Min | Max | Unit |
| $V_{OH}$ | –1.02/3.98 | –0.84/4.16 | –0.98/4.02 | –0.81/4.19 | –0.92/4.08 | –0.735/4.265 | –1.025/3.975 | –0.880/4.120 | V |
| $V_{OL}$ | –1.95/3.05 | –1.63/3.37 | –1.95/3.05 | –1.63/3.37 | –1.95/3.05 | –1.600/3.400 | –1.810/3.190 | –1.620/3.380 | V |
| $V_{OHA}$ | — | — | — | — | — | — | — | –1.610/3.390 | V |
| $V_{OLA}$ | — | — | — | — | — | — | –1.035/3.965 | — | V |
| $V_{IH}$ | –1.17/3.83 | –0.84/4.16 | –1.13/3.87 | –0.81/4.19 | –1.07/3.93 | –0.735/4.265 | –1.165/3.835 | –0.880/4.120 | V |
| $V_{IL}$ | –1.95/3.05 | –1.48/3.52 | –1.95/3.05 | –1.48/3.52 | –1.95/3.05 | –1.450/3.550 | –1.810/3.190 | –1.475/3.525 | V |
| $V_{BB}$ | –1.38/3.62 | –1.27/3.73 | –1.35/3.65 | –1.25/3.75 | –1.31/3.69 | –1.190/3.810 | –1.380/3.620 | –1.260/3.740 | V |

**Parallel Termination Schemes**

Because the techniques using an extra $V_{TT}$ power supply consume significantly less power, as the number of PECL devices incorporated in the design increases the more attractive the $V_{TT}$ supply termination scheme becomes. Typically ECL is specified driving 50 Ω into a –2.0 V, therefore for PECL with a $V_{CC}$ supply different than ground the $V_{TT}$ terminating voltage will be $V_{CC}$ – 2.0 V. Ideally the $V_{TT}$ supply would track 1:1 with $V_{CC}$, however in theory this scenario is highly unlikely. To ensure proper operation of a PECL device within the system the tolerances of the $V_{TT}$ and the $V_{CC}$ supplies should be considered. Assume for instance that the nominal case is for a 50 Ω load ($R_t$) into a +3.0 V supply; for a 10H compatible device with a $V_{OHmax}$ of –0.81 V and a realistic $V_{OLmin}$ of –1 .85 V the following can be derived:

$I_{OHmax} = (V_{OHmax} – V_{TT})/R_t$
$I_{OHmax} = (\{5.0 – 0.81\} – 3.0)/50 = 23.8$ mA
$I_{OLmin} = (V_{OLmin} – V_{TT})/R_t$
$I_{OLmin} = (\{5.0 – 1.85\} – 3.0)/50 = 3.0$ mA

If +5% supplies are assumed a $V_{CC}$ of $V_{CCnom}$ –5% and a $V_{TT}$ of $V_{TTnom}$ +5% will represent the worst case. Under these conditions, the following output currents will result:

$I_{OHmax} = (\{4.75 – 0.81\} – 3.15)/50 = 15.8$ mA
$I_{OLmin} = (\{4.75 – 1.85\} – 3.15)/50 = 0$ mA

Using the other extremes for the supply voltages yields:

$I_{OHmax} = 31.8$ mA
$I_{OLmin} = 11$ mA

The changes in the $I_{OH}$ currents will affect the DC $V_{OH}$ levels by ≈±40mV at the two extremes. However in the vast majority of cases the DC levels for ECL devices are well centered in their specification windows, thus this variation will simply move the level within the valid specification window and no loss of worst case noise margin will be seen. The $I_{OL}$ situation on the other hand does pose a potential AC problem. In the worst case situation the output emitter follower could move into the cutoff state. The output emitter followers of ECL devices are designed to be in the conducting “on” state at all times. If cutoff, the delay of the device will be increased due to the extra time required to pull the output emitter follower out of the cutoff state. Again this situation will arise only under a number of simultaneous worst case situations and therefore is highly unlikely to occur, but because of the potential it should not be overlooked.

**Thevenin Equivalent Termination Schemes**

The Thevenin equivalent parallel termination technique of Figure 3 is likely the most attractive scheme for the CMOS/TTL designer who is using a small amount of ECL. As mentioned earlier this technique will consume more power, however the absence of an additional power supply will more than compensate for the extra power consumption. In addition, this extra power is consumed entirely in the external resistors and thus will not affect the reliability of the IC. As is the case with standard parallel termination, the tolerances of the $V_{TT}$ and $V_{CC}$ supplies should be addressed in the design phase. The following equations provide a means of determining the two resistor values and the resulting equivalent $V_{TT}$ terminating voltage.

$R1 = R2\ (\{V_{CC} – V_{TT}\}/\{V_{TT} – V_{EE}\})$
$R2 = Z_O\ (\{V_{CC} – V_{EE}\}/\{V_{CC} – V_{TT}\})$
$V_{TT} = V_{CC}\ (R2/\{R1 + R2\})$

For the typical setup:

$V_{CC}$ = 5.0 V; $V_{EE}$ = GND; $V_{TT}$ = 3.0 V; and $Z_O$ = 50 Ω

$R2 = 50\ (\{5 – 0\}/\{5–3\}) = 125$ Ω
$R1 = 125\ (\{5–3\}/\{3–0\}) = 83.3$ Ω

checking for $V_{TT}$

$V_{TT} = 5\ (125/\{125 – 83.3\}) = 3.0$ V

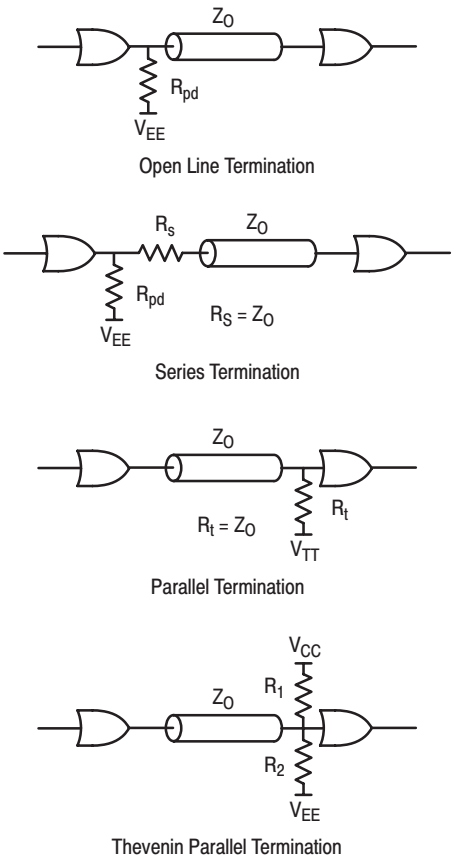



**Figure 3. Termination Techniques for ECL/PECL Devices**

Because of the resistor divider network used to generate $V_{TT}$ the variation in V will be intimately tied to the variation in $V_{CC}$. Differentiating the equation for $V_{TT}$ with respect to $V_{CC}$ yields:

$$dV_{TT}/dV_{CC} = R2/(R1 + R2)\ dV_{CC}$$

Again for the nominal case this equation reduces to:

$$\Delta V_{TT} = 0.6\ \Delta V_{CC}$$

So that for $\Delta V_{CC} = \pm 5\% = \pm 0.25$ V, $\Delta V_{TT} = \pm 0.15$ V.

As mentioned previously the real potential for problems will be if the $V_{OL}$ level can potentially put the output emitter follower into cutoff. Because of the relationship between the $V_{CC}$ and $V_{TT}$ levels the only situation which could present a problem will be for the lowest value of $V_{CC}$. Applying the equation for $I_{OLmin}$ under this condition yields:

$$I_{OLmin} = (\{V_{OLmin} - V_{TT}\}/R_t$$
$$I_{OLmin} = (\{4.75 - 1.85\} - 2.85)/50 = 1.0\ \text{mA}$$

From this analysis it appears that there is no potential for the output emitter follower to be cutoff. This would suggest that the Thevenin equivalent termination scheme is actually a better design to compensate for changes in $V_{CC}$ due to the fact that these changes will affect $V_{TT}$, although not 1:1 as would be ideal, in the same way. To make the design even more immune to potential output emitter follower cutoff the designer can design for nominal operation for the worst case situation. Since the designer has the flexibility of choosing the $V_{TT}$ level via the selection of the R1 and R2 resistors the following procedure can be followed.

Let $V_{CC} = 4.75$ V and $V_{TT} = V_{CC} - 2.0$ V $= 2.75$ V

Therefore:

$R2 = 119\ \Omega$ and $R1 = 86\ \Omega$ thus:

$I_{OHmax} = 23$ mA and $I_{OLmin} = 3.0$ mA

Plugging in these values for the equations at the other extreme for $V_{CC} = 5.25$ V yields:

$V_{TT} = 3.05$ V, $I_{OHmax} = 28$ mA and $I_{OLmin} = 5.2$ mA

Although the output currents are slightly higher than nominal, the potential for performance degradation is much less and the results of any degradation present will be significantly less dramatic than would be the case when the output emitter follower is cutoff. Again in most cases the component manufactures will provide devices with typical output levels; typical levels significantly reduces any chance of problems. However it is important that the system designer is aware of where any potential problems may come from so they can be dealt with during the initial design.

**Differential ECL Termination**

Differential ECL outputs can be terminated using two different strategies. The first strategy is to simply treat the complimentary outputs as independent lines and terminate them as previously discussed. For simple interconnect between devices on a single board or short distances across the backplane this is the most common method used. For interconnect across larger distances or where a controlled impedance backplane is not available the differential outputs can be distributed via twisted pair of ribbon cable (use of ribbon cable assumes every other wire is a ground so that a characteristics impedance will arise). Figure 4 illustrates common termination techniques for twisted pair/ribbon cable applications. Notice that Thevenin equivalent termination techniques can be extended to twisted pair and ribbon cable applications as pictured in Figure 4. However for twisted pair/ribbon cable applications the standard termination technique picture in Figure 4 is somewhat simpler and also does not require a separate termination voltage supply. If however the Thevenin techniques are necessary for a particular application the following equations can be used:

$$R1 = R2 = Z_O/2$$
$$R3 = R1\ (V_{TT} - V_{EE})/(V_{OH} + V_{OL} - 2V_{TT})$$
$$V_{TT} = (R3\{V_{OH} + V_{OL}\} + R1\{V_{EE}\})/(R1 + 2R3)$$

where $V_{OH}$, $V_{OL}$, $V_{EE}$ and $V_{TT}$ are PECL voltage levels.

Plugging in the various values for $V_{CC}$ will show that the $V_{TT}$ tracks with $V_{CC}$ at a rate of approximately 0.7:1. Although this rate is approaching ideal it would still behoove the system designer to ensure there are no potential situations where the output emitter follower could become cutoff. The calculations are similar to those performed previously and will not be repeated. The same equations with the change $R1 = R2 = Z_O$ can be used to calculate a "Y" termination for differential outputs into separate microstrip, strip or coaxial cables.

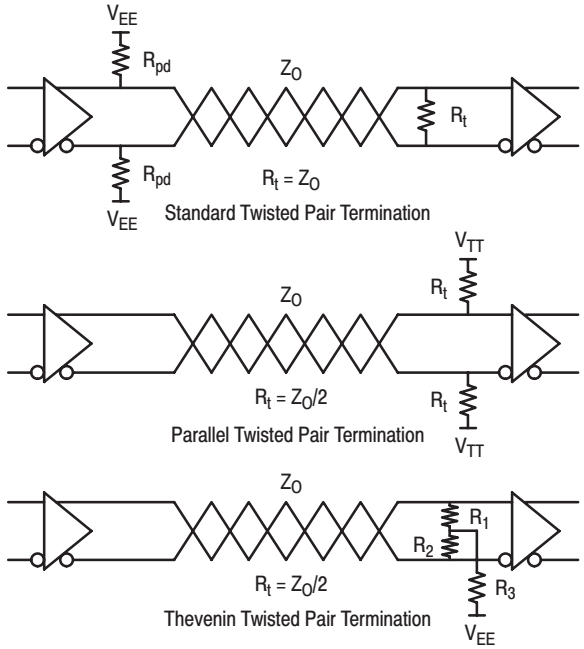



**Figure 4. Twisted Pair Termination Techniques**

## NOISE AND POWER SUPPLY DISTRIBUTION

Since ECL devices are top rail referenced it is imperative that the $V_{CC}$ rail be kept as noise free and variation free as possible. To minimize the $V_{CC}$ noise of a system liberal bypassing techniques should be employed. Placing a bypass capacitor of 0.01μF to 0.1 μF on the $V_{CC}$ pin of every device will help to ensure a noise free $V_{CC}$ supply. In addition when using PECL in a system populated heavily with CMOS and TTL logic the two power supply planes should be isolated as much as possible. This technique will help to keep the large current spike noise typically seen in CMOS and TTL drivers from coupling into the ECL devices. The ideal situation would be multiple power planes; two dedicated to the PECL $V_{CC}$ and ground and the other two to the CMOS/TTL $V_{CC}$ and ground. However if these extra planes are not feasible due to board cost or board thickness constraints common planes with divided subplanes can be used (Figure 5 on page 663). In either case the planes or sub planes should be connected to the system power via separate paths. Use of separate pins of the board connectors is one example of connecting to the system supplies.

For single supply translators or dual supply translators which share common power pins the package pins should be connected to the ECL $V_{CC}$ and ground planes to ensure the noise introduced to the part through the power plane is minimal. For translating devices with separate TTL and ECL power supply pins, the pins should be tied to the appropriate power planes.

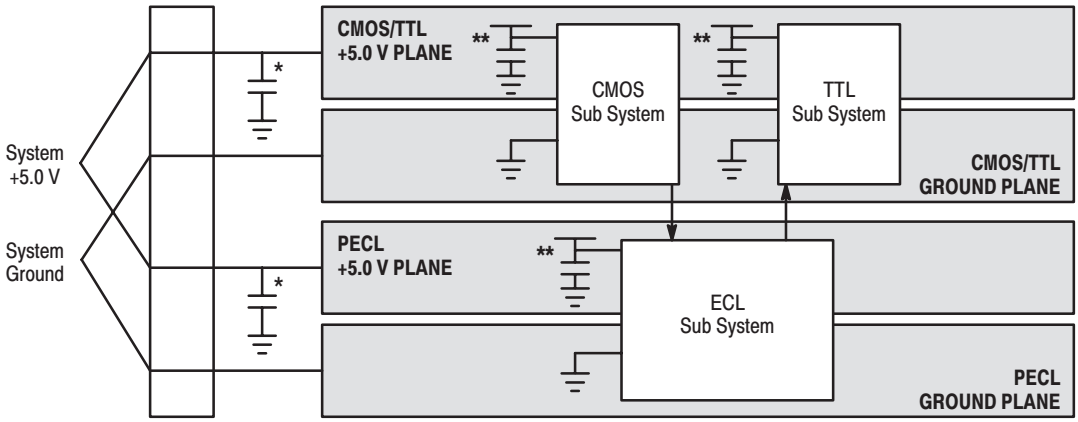
Another concern is the interconnect between two cards with separate connections to the $V_{CC}$ supply. If the two boards are at the opposite extremes of the $V_{CC}$ tolerance, with the driver being at the higher limit and the receiver at the lower limit, there is potential for soft saturation of the receiver input. Soft saturation will manifest itself as degradation in AC performance. Although this scenario is unlikely, again the potential should be examined. For situations where this potential exists there are devices available which are less susceptible to the saturation problem. This variation in $V_{CC}$ between boards will also lead to variations in the input switching references. This variation will lead to switching references which are not ideally centered in the input swing and cause rise/fall skew within the receiving device. Obviously the later skew problem can be eliminated by employing differential interconnect between boards.

When using PECL to drive signals across a backplane, situations may arise where the driver and the receiver are on different power supplies. A potential problem exists if the receiver is powered down independent of the driver. Figure 6, on page 663, represents a generic driver/receiver pair. A current path exists through the receiver's $V_{CC}$ plane when the receiver is powered–down and the driver is powered–on, as shown in Figure 6. If the receiver has ESD protection, the current will flow though the ESD diode to $V_{CC}$. If the receiver has NO ESD protection, the current will flow through the input transistor and emitter–follower base–collector junctions to $V_{CC}$. The amount of current flow, in either case, will be enough to damage both the driver and receiver devices. Either of these situations could lead to degradation of the reliability of the devices. Because different devices have different ESD protection schemes, and input architectures, the extent of the potential problem will vary from device to device.

Another issue that arises in driving backplanes is situations where the input signals to the receiver are lost and present an open input condition. Many differential input devices will become unstable in this situation, however, most of the newer designs, and some of the older designs, incorporate internal clamp circuitry to guarantee stable outputs under open input conditions. All of the ECLinPS (except for the E111), ECLinPS Lite, and H600 devices, along with the MC10125, 10H125 and 10114 will maintain stable outputs under open input conditions.

## CONCLUSION

The use of ECL logic has always been surrounded by clouds of misinformation; none of those clouds have been thicker than the one concerning PECL. By breaking through this cloud of misinformation the traditional CMOS/TTL designers can approach system problems armed with a complete set of tools. For areas within their designs which require very high speed, the driving of long, low impedance lines or the distribution of very low skew clocks, designers can take advantage of the built in features of ECL. By incorporating this ECL logic using PECL methodologies this inclusion need not require the addition of more power supplies to unnecessarily drive up the cost of their systems. By following the simple guidelines presented here CMOS/TTL designers can truly optimize their designs by utilizing ECL logic in areas in which they are ideally suited. Thus bringing to market products which offer the ultimate in performance at the lowest possible cost.




* Low frequency bypass at the board input
** High frequency bypass at the individual device level

**Figure 5. Power Plane Isolation in Mixed Logic Systems**

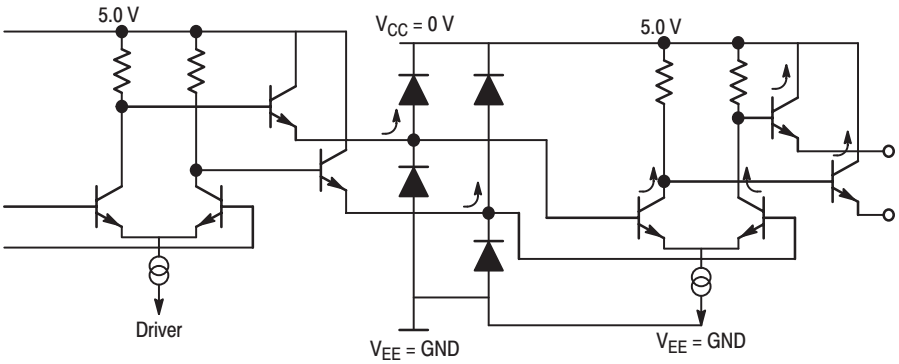



**Figure 6. Generic Driver/Receiver Pair**

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**Order Number: AN1545/D**
**Rev 1, 08/2001**

**AN1545**

# Thermal Data for MPC Clock Drivers

**Prepared by: Todd Pearson**
**Applications Engineering**

## INTRODUCTION

This application note provides general information on thermal and related reliability issues with respect to the MPC family of clock driver products. In addition, methods are presented to estimate power dissipation and junction temperatures for the MPC product family.

### Package Choice

The Motorola Timing Solutions products are offered in a variety of surface mount plastic packages. These packages include the 16 and 20 lead SOIC, 20 and 28 lead PLCC and the 32 and 52 lead TQFP packages. The bulk of the newer products are being introduced in the SOIC and TQFP packages with the PLCC being used for the older mature products.

The surface mount plastic packages were selected as the optimum combination of performance, physical size and thermal handling in a low cost standard package. While more exotic packages exist to improve the thermal and electrical performance the cost of these are prohibitive for many applications.

### Long Term Failure Mechanisms in Plastic Packages

When analyzing a design for its long term reliability it is important that the dominant failure mechanisms are well understood. Although today's plastic packages are as reliable as ceramic packages under most environmental conditions, as the junction temperature increases a failure mode unique to plastic packages becomes a significant factor in the long term reliability of the device.

Modern plastic package assembly utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. Because plastic packages use injection molding the bond wires used must be extremely ductile to keep from breaking or being pulled from the bond pad during the injection process. Gold wire has far better ductility than aluminum wire and therefore is used in the process of plastic packaging. Aluminum is the metal used in the majority of low cost digital IC processes for transistor and bond wire interconnect. As the temperature of the silicon (junction temperature) increases an intermetallic forms between the gold and aluminum interface. This intermetallic formation results in a significant increase in the impedance of the wire bond and can lead to performance failure of the affected pin. With this relationship between intermetallic formation and junction temperature established, it is incumbent on the designer to ensure that the junction temperature for which a device will operate is consistent with the long term reliability goals of the system.

Reliability studies were performed at elevated ambient temperatures (125°C) from which an arrhenius equation relating junction temperature to bond failure was established. The application of the equation yields Table 1. This table relates the junction temperature of a device in a plastic package to the continuous operating time before 0.1% bond failure (1 failure per 1000 bonds). Note that this equation only holds for continuous elevated junction temperature levels, as the curve is quite steep if a system cycles through a temperature range but spends a relatively short amount of time at the extreme the numbers provided in this table will grossly underestimate the lifetime of the device based solely on the worst case junction temperature seen.

**Table 1. Package Junction Temperatures**

| Junction Temperature (°C) | Time (Hours) | Time (Years) |
|---|---|---|
| 80 | 1,032,200 | 117.8 |
| 90 | 419,300 | 47.9 |
| 100 | 178,700 | 20.4 |
| 110 | 79,600 | 9.1 |
| 120 | 37,000 | 4.2 |
| 130 | 17,800 | 2.0 |
| 140 | 8,900 | 1.0 |

The Motorola Timing solutions products are designed with chip power levels that permit acceptable reliability levels, in most systems, under conventional 500lfpm (2.5m/s) airflow. However because of their flexibility and programmability there may be some situations where special thermal considerations may be required.

### Thermal Management

In any system design proper thermal management is essential to establish the appropriate trade–off between performance, density, reliability and cost. In particular the designer should be aware of the reliability implication of continuously operating semiconductor devices at high junction temperatures.

The increasing popularity of plastic, small outline surface mount packages is putting a greater emphasis on the need for better thermal management of a system. This is due to the fact that the newer SMD packages generally require less board space than their first generation brethren. Thus designs incorporating the latest generation SMD packaging technologies have a higher thermal density. To optimize the thermal management of a system it is imperative that the user understand all of the variables which contribute to the junction temperature of the device.

The variables involved in determining the junction temperature of a device are both supplier and user defined. The supplier, through lead frame design, mold compounds, die size and die attach can positively impact the thermal resistance and thus, the junction temperature of a device. Motorola continually experiments with new package designs and assembly techniques in an attempt to further enhance the thermal performance of its products.

It can be argued that the user has the greatest control of the variables which commonly impact the thermal performance of a device. Ambient temperature, air flow and related cooling techniques are the obvious user controlled variables, however

PCB substrate material, layout density, amount of exposed copper and weight of copper used in the power planes can all have significant impacts on the thermal performance of a system.

PCB substrates all have different thermal characteristics, these characteristics should be considered when exploring the PCB alternatives. Users should also account for the different power dissipation of the different devices in their systems and space them accordingly. In this way the heat load is spread across a larger area and “hot spots” do not appear in the layout. Copper interconnect and power planes act as heat radiators, therefore significant thermal dissipation can be achieved by paying special attention to the copper elements of a PCB. The thermal resistance of copper (package leadframes are made from copper) is significantly lower than that of the epoxy used for the body of plastic packages. As a result the dominant mode of heat flow out of a package is through the leads. By employing techniques at the board level to enhance the transfer of this heat from the package leads to the PCB one can reduce the effective thermal resistance of the plastic package. Copper interconnect traces on the top layer of the PCB are excellent radiators for transferring heat to the ambient air, especially if these traces are exposed to even moderate air flow. In addition using thick copper power planes not only reduces the electrical resistance but also enhances their thermal carrying capabilities. The power planes can be thermally enhanced further by employing special edge connectors which draw the heat from the planes and again dissipate it into the ambient. Finally, the use of thermal conductive epoxies between the underneath of a device and thermal vias to a power plane can accelerate the transfer of heat from the device to the PCB where once again it can more easily be passed to the ambient.

The advent of small outline SMD packaging and the industry push towards smaller, denser designs makes it incumbent on the designer to provide for the removal of thermal energy from the system. Users should be aware that they control many of the variables which impact the junction temperatures and, thus, to some extent, the long term reliability of their designs.

**Calculating Junction Temperature**

Since the reliability of a device is directly related to junction temperature and that temperature cannot be measured directly there needs to be a means of calculating the approximate junction temperature from measurable parameters. There are two equations which can be used:

$$T_J = T_A + PD\theta_{JA} \text{ or } T_J = T_C + PD\theta_{JC}$$

where:
$T_J$ = Junction Temperature
$T_A$ = Ambient Temperature (°C)
$T_C$ = Case Temperature (°C)
PD = Internal Power Dissipation of the Device (W)
$\theta_{JA}$ = Avg Pkg Thermal Resistance (Junction – Ambient)
$\theta_{JC}$ = Avg Pkg Thermal Resistance (Junction – Case)

The $\theta_{JC}$ numbers are determined by submerging a device in a liquid bath and measuring the temperature rise of the bath, it therefore represents an average case temperature. The difficulty in using this method arises in the determination of the case temperature in an actual system The case temperature is a function of the location on the package at which the temperature is measured. Therefore, to use the $\theta_{JC}$ method the case temperature would have to be measured at several different points and averaged to represent the $T_C$ of the device. This in practice could prove difficult and relatively inaccurate. To alleviate this problem manufacturers will sometimes provide a $\theta_{Jref}$ value for a package. This number represents the thermal resistance between the die and a specific spot on the package (usually the top dead center). This measure of thermal resistance typically has a much wider standard deviation than the standard resistance parameters and therefore is sometimes avoided, however it is the most easily measured parameter from which junction temperatures can be calculated.

The $\theta_{JA}$ method of estimating junction temperature is the most widely used. To use this method one need only measure the ambient air temperature in the vicinity of the device in question and calculate the internal power dissipation of that device. The total power dissipation in a device is made up of two parts; the static power and the dynamic power. The two components can be calculated separately and then added together. Another source of power is the termination power as clock drivers are generally used to drive terminated transmission lines. For an ECL output this can be significant however for CMOS outputs the termination load current is pulled through very little voltage (the output HIGH and LOW voltages are very near the rail) so that most of the power is dissipated in the actual load. With this in mind we will address calculating power for ECL and CMOS/BiCMOS separately.

Because clock drivers generally drive transmission lines we will not assume any lumped capacitive load at the outputs. Lumped capacitive loads on outputs add significantly to the power dissipated on chip, when however the capacitive loads are at the the end of transmission lines they are buffered from the driving device and thus do not add to the power dissipation above that attributed to driving the transmission line. Note that for the purpose of power dissipation calculations it is not equivalent to calculate the distributed capacitance of a transmission line and treat it as a lumped load at the output of the device. This technique will significantly overestimate the calculated power of a device.

**Calculating Power Dissipation in CMOS/BiCMOS Devices**

The total power dissipated in a device can be represented as follows:

$$P_D = I_{CC}(\text{static})*V_{CC} + I_{CC}(\text{dynamic})*V_{CC} + n(I_{OH}*(V_{CC} - V_{OH}) + I_{OL}*(V_{OL}))/2$$

In general rather than using dynamic $I_{CC}$ numbers the dynamic power is calculated using power dissipation capacitance numbers ($C_{PD}$). Using $C_{PD}$ numbers the above equation becomes:

$$P_D = I_{CC}(\text{static})*V_{CC} + C_{PD}*V_{CC}^2*f + n(I_{OH}*(V_{CC} - V_{OH}) + I_{OL}*(V_{OL}))/2$$

As mentioned previously since the output logic levels are very nearly rail to rail, the third part of the above equation can be ignored. Note that although this assumption may be true for series terminated lines it may not be true for parallel termination where the relatively large DC currents will drive the output voltage levels away from the rails. If we assume series termination then the equation reduces to the following:

$$P_D = I_{CC}(\text{static})*V_{CC} + C_{PD}*V_{CC}^2*f$$

The dynamic dissipation may be a function of the number of outputs switching, if this is the case a CPD number may be provided for each output buffer. In this case the equation would expand to:

$P_D = I_{CC}(static)*V_{CC} + C_{PD}(internal)*V_{CC}^2*f + C_{PD}(output)*V_{CC}^2*f*n$

where n = number of outputs at the given frequency f.

Finally for a CMOS device the $I_{CC}(static) = 0$ and for a BiCMOS device which utilizes ECL gates internal the $C_{PD}(internal) = 0$ so that the equations reduce to:

$CMOS\ P_D = C_{PD}(internal)*V_{CC}^2*f + C_{PD}(output)*V_{CC}^2*f*n$

$BiCMOS\ P_D = I_{CC}(static)*V_{CC} + C_{PD}(output)*V_{CC}^2*f*n$

**Calculating Power Dissipation in ECL Devices**

Starting from the same basic equation:

$P_D = I_{CC}(static)*V_{CC} + I_{CC}(dynamic)*V_{CC} + n(I_{OH}*(V_{CC} – V_{OH}) + I_{OL}*(V_{CC} – V_{OL}))/2$

For ECL devices the the static current is equal to the dynamic current ($I_{CC}$ is independent of frequency) therefore the equation reduces to:

$P_D = I_{CC}*V_{CC} + n(I_{OH}*(V_{CC} – V_{OH}) + I_{OL}*(V_{CC} – V_{OL}))/2$

The above equation assumes a 50% duty cycle on a single ended output and thus takes the average of the high state and low state power dissipation. For differential outputs it is simpler to calculate the power per output pairs. Since the pairs are always in complementary states the output power for the pair is simply the addition of the low state and high state power consumption. The only time one will see a difference between a single ended and differential output calculation is under worst case conditions. For say an 18 single ended output device the worst case condition would be for all 18 to be in the worst case logic state for power dissipation purposes. For a device on the other hand with 9 pairs of complimentary outputs (18 total) only 9 of the outputs can be in the worst case condition at a time so that the worst case power dissipation of a complimentary output device will be less than a device with an equivalent number of single ended outputs.

The only issue left is determining $I_{OL}$ and $I_{OH}$. These values are a function of the termination technique and the pull down voltage used. The currents are easily calculated based on the $V_{OH}/V_{OL}$ levels the pull down resistance and the pull down voltage used. For a standard termination of 50Ω to a voltage of 2.0V below $V_{CC}$:

$I_{OH} = (V_{CC} – 0.98) – (V_{CC} – 2.0)/50 = 20.4\ mA$

$I_{OL} = (V_{CC} – 1.7) – (V_{CC} – 2.0)/50 = 6.0\ mA$

**Thermal Resistance of Plastic Packages**

With the power estimates calculated the $\theta_{JA}$ of the appropriate package is the only required parameter left to estimate the junction temperature of a device. The $\theta_{JA}$ number for a package is expressed in °C per Watt (°C/W) and is used to determine the temperature elevation of the die (junction) over the external ambient temperature. Standard lab measurements of this parameter for the various timing solution packages are provided in the graphs of figure 1 through figure 3.

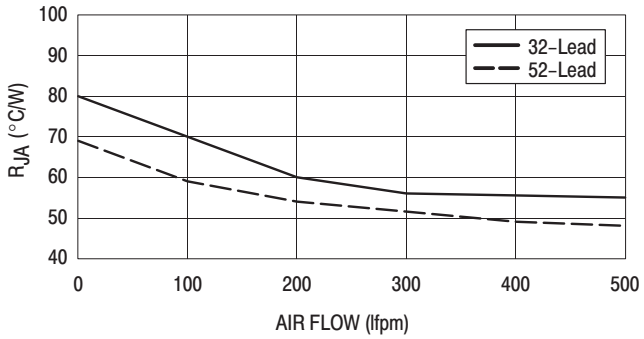


**Figure 1. Thermal Resistance of the TQFP Packages**

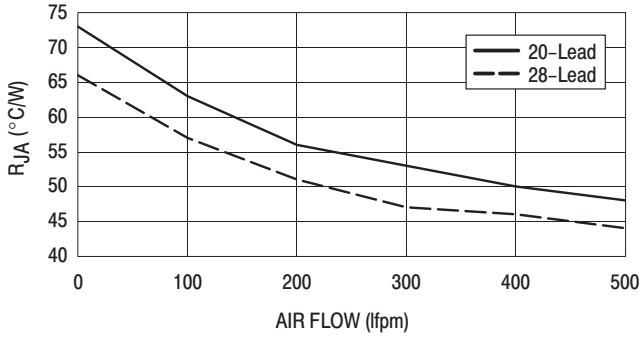


**Figure 2. Thermal Resistance of the PLCC Packages**

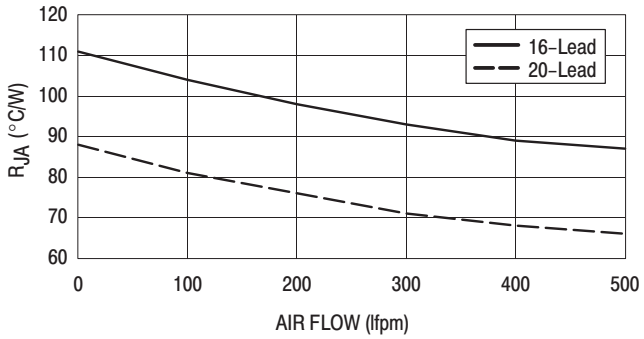


**Figure 3. Thermal Resistance of the SOIC Packages**

**Junction Temperature Calculation Example**

As an example the junction temperature of the MPC951 will be calculated. The static $I_{CC}$ of the MPC951 is 95mA and the $C_{PD}$ per output is 25pf. From these numbers the following results:

$P_D = 95\ mA*3.3\ V + 3.3\ V*3.3\ V*25\ pf*f*n = 315\ mW + 2.72\ e{-}10*f*n$

Assume we will configure all 9 outputs to the same frequency, the curve in figure 4 shows the power dissipation vs frequency for the MPC951.

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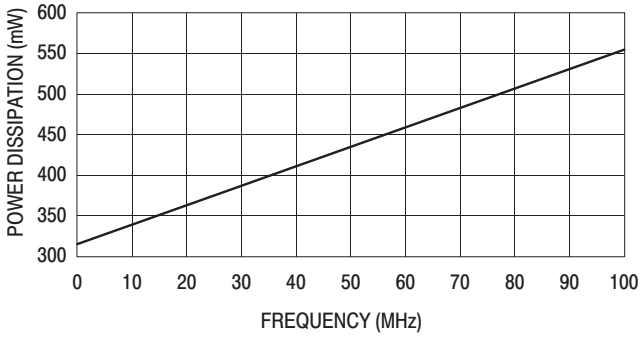


**Figure 4. MPC951 Junction Temperature Calculation**

Assume that one is building a design with all nine outputs operating at 66MHz. From the graph this corresponds to a power dissipation of 470 mW. The MPC951 is packaged in the 32lead TQFP; from the $\theta_{JA}$ chart (assume zero air flow) the thermal resistance of the package is 97°C/W. Plugging these into the $T_J$ equation yields the following:

$T_J = T_A + 80°C/W*0.470\ W = T_A + 38°C$.

For a worst case ambient temperature of 70°C the resulting junction temperature would be 108°C. From the MTBF table this would correspond to a lifetime of greater than nine years, a lifetime which is well within the requirements of most systems. If however the user needed a little higher performance of 100MHz on the outputs the $T_J$ would be:

$T_J = T_A + 80°C/W*0.555W = T_A + 44°C$

Under these conditions the worst case junction temperature would be 114°C and the worst case lifetime would be approaching 4 years. This may not be a satisfactory lifetime and the user would have to do some thermal management to reduce the junction temperature. Obvious enhancements would be providing airflow or perhaps reducing the maximum ambient specifications. If airflow was added (200lfpm) the junction temperature would reduce to:

$T_J = T_A + 60°C/W * 0.555W = T_A + 33°C$

This drops the junction temperature down into the same range as the 66 MHz output case.

The second example will use an ECL output device; the MC100LVE111. The device has 9 differential output pairs and an $I_{CC}$ of 65mA. Assume that the outputs are terminated 50Ω to 2.0V below $V_{CC}$.

$P_D = 65\ mA * 3.3\ V + 9((0.98*1.02/50)+(1.7*0.3/50)) =$
$215\ mW + 270\ mW = 485\ mW$

The MC100LVE111 is packaged in the 28lead PLCC; from the $\theta_{JA}$ tables the $\theta_{JA}$ at 500lfpm is 45°C/W. This yield the following approximate junction temperature:

$T_J = T_A + 45°C/W*0.485\ W = T_A + 22°C$

For a maximum ambient of 70°C the LVE111 exhibits more than satisfactory long term reliability for most systems under standard operating conditions.

Note in both cases the most efficient way to lower the junction temperature is to reduce the ambient temperature of the system. Unit changes in ambient temperature result in unit changes in junction temperature no other parameter is this tightly coupled to junction temperature.

**Limitations to Junction Temperature Calculations**

The use of the previously described technique for estimating junction temperatures is intimately tied to the measured values of the $\theta_{JA}$ of the package. Since this parameter is a function of not only the package, but also the test fixture the results may not be applicable for every environmental condition. As mentioned previously the $\theta_{JA}$ of a package in a system could be somewhat higher or lower depending on the thermal design of the board.

In addition the reliability numbers derived for the intermetallic formation assumes constant usage at the specific conditions. In the real world devices will not be exposed to worst case conditions continuously but rather will cycle between the worst case and a lower junction temperature. The MTBF table does not take into account this cycling so that simply calculating the worst case junction temperature and applying it to the table directly will significantly underestimate the long term reliability of the device. Because reliability and environmental conditions are statistical in nature it is important that statistical analysis be applied to any long term reliability studies done on the clock driver products.

# AN1934

# Effects of Skew and Jitter on Clock Tree Design

**Prepared by: Don Aldridge and Tom Borr**
**September, 2001**

## ABSTRACT

This application note discusses the parametrics of skew and jitter as these terms apply to PLL clock drivers and clock buffers. The application note covers the definition of the various types of skew and jitter, the measurement techniques and values associated with these parameters, and concludes with an example clock tree design and analysis of the skew and jitter.

## INTRODUCTION

At first glance, clock distribution trees are relatively simple. As shown in Figure 1, a typical clock distribution tree consists of a clock source and a series of clock distribution buffers that deliver multiple copies of the clock source to many locations in an electronic system. The clock source may be a crystal oscillator (Figure 1) or an external clock source. This clock source may be at the desired frequency or may need to be translated to the desired frequency or frequencies as part of the clock tree circuitry. The clock tree will consist of some combination of PLL clock drivers and/or fanout buffers providing multiple outputs. The clock tree may consist of several devices or be composed of a single integrated circuit. Individual clock outputs deliver the clock signal to various locations on a PC board.

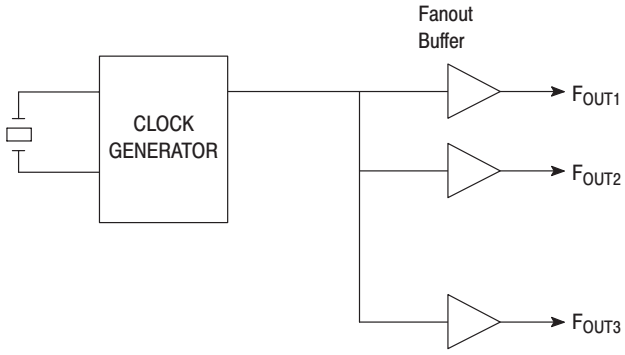


**Figure 1. Typical Clock Distribution Tree**

After a more detailed look at the requirements of the clock system and the data sheet specifications of the devices used to implement the clock tree, the design appears a bit more complicated and requires a more detailed analysis. The specifications that are most important for this type of analysis are usually found in the AC parameter portion of the clock driver data sheet and consist of parameters such as propagation delay, skew, and jitter.

This application note discusses these parameters by reviewing the definition, the measurement techniques, and their effects on system performance. The application note concludes with the analysis of a typical clock distribution tree based upon these parameters.

### Standards for Skew, Jitter Definitions, and Notations

The reference used to determine the standards for skew, jitter definitions, and notations for this application note are the EIA specification EIA/JESD65. This EIA specification documents the current industry standard for these parameters. This document is available in a downloadable PDF format at the web site of http://www.jedec.org/.

### Clock Driver Devices

Clock driver devices consist of both clock fanout buffers and PLL based clock generators. Typical fanout buffers are shown in Figure 2 and consist of an input buffer driving many outputs though individual output buffers. The specific devices shown are the MPC942C and MPC942P which offer 18 LVCMOS outputs and have either a LVCMOS input or a LVPECL input. Some fanout buffers have an optional internal divider network to produce an input clock divided by two. A Phase Lock Loop device is shown in Figure 4 and may or may not have built–in fanout buffers. It is not the intention of this application note to explain all of the fundamentals of a PLL; however, a quick review of the components is covered.

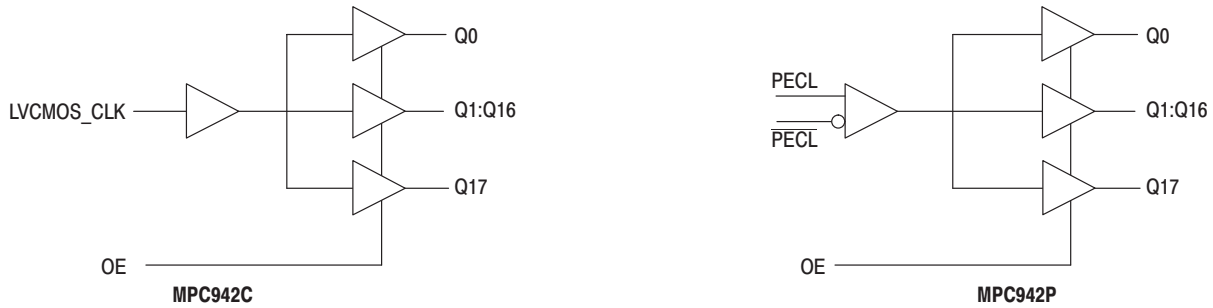


**Figure 2. Fanout Buffer**

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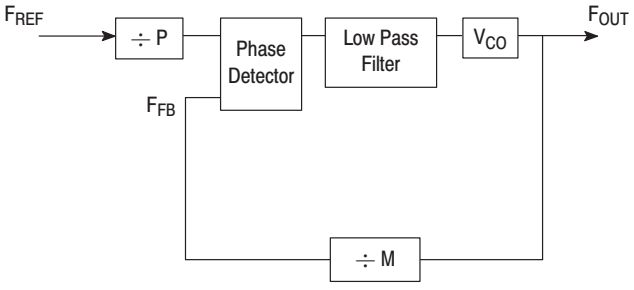
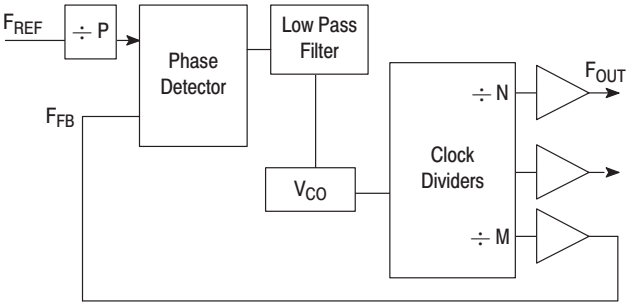
A basic PLL clock architecture (Figure 3) consists of a phase detector, a low pass filter, a $V_{CO,}$ and (in this diagram) two divider networks. Both dividers are at the inputs of the phase detector. The input to the clock driver, or the reference frequency, may be external or sourced from a crystal oscillator that is included as part of the clock driver architecture. This input frequency may be divided by an optional P divider block and then applied to the input of the phase detector. The phase detector produces a correction signal based upon the difference in phase in its two inputs. The correction signal or the output of the phase detector is filtered and applied to the input of the voltage controlled oscillator; $V_{CO}$. The output of the $V_{CO}$ is applied to the M divider and becomes feedback and the second of the two inputs to the phase detector. When the loop is in "lock," the two inputs to the phase detector are the same frequency and the same phase. The output frequency, or $F_{OUT,}$ is the reference frequency divided by P and then multiplied by M and will continually track the reference frequency.

With a few additions to the basic PLL clock architecture, we can create a multi–frequency and multi–clock distribution device as shown in Figure 4. The more complex divider network shown provides the M divide value for the feedback path to the input of the phase detector and, also, the N divider divides down the $V_{CO}$ frequency to the desired system frequency or frequencies. Multiple outputs from the clock divider may provide for the generation of multiple frequencies. Note that fanout buffers are included for each output to provide the required system clock drive. Also note that an equivalent fanout buffer is included for the feedback path. The feedback connection for the PLL is external to the device and thus equalizes the delay through the main clock outputs. As is discussed later, the external feedback path may also include compensating trace delay which allows the phase of $F_{OUT}$ clock to be advanced forward or backward with respect to the input clock.




$F_{OUT} = (F_{REF} / P) * M$

**Figure 3. Basic PLL**




$F_{OUT} = (F_{REF} / P) * (M/N)$

**Figure 4. PLL Based Clock Driver**

**Clock Driver Parametrics**

The clock driver parameters that are of interest in this application note are Buffer Propagation Delay, Zero Reference Delay, Skew, Jitter, and PLL Bandwidth and Jitter. These parameters are typically found in the AC parameter portion of a clock driver data sheet.

Fanout buffers have output skew, jitter, and propagation delay. PLL clock driver devices are characterized with jitter, output skew, and an effective input to output propagation delay called Zero Reference Phase Delay. In a clock tree design, the parameters that complicate the analysis is skew between the outputs of a clock fanout buffer and edge or frequency jitter. Jitter commonly is generated in the very early stages of a clock tree and potentially at each stage of the clock tree. These jitter sources may or may not be cumulative and be passed to the outputs.

**Buffer Propagation Delay**

Clock distribution buffers have a propagation delay from input to output. Typical values for this delay are in the order of a few nanoseconds. Data sheet specifications may be given for a single propagation delay or as separate values given for a low to high edge; versus a high to low edge. The low to high edge value and the high to low edge value should be very similar but not necessarily the same. The notation for propagation delay is $t_{pd}$. Also the notations of $t_{plh}$ and $t_{phl}$ are used to indicate the propagation delay for a low to high transition and a high to low transition of a waveform, respectively.

**Reference Zero Delay**

Reference Zero Delay is the JEDEC term for the effective PLL buffer delay. This parameter is also referred to as Static Phase Offset (or SPO). The JEDEC notation is $t_{(\phi)}$. The value of SPO is defined as the average difference in phase between the input reference clock and the feedback input signal, when the PLL is locked. The value of the Reference Zero Delay can be compensated for by including PC board trace delay in the feedback path of the PLL. Specially constructed PLL clock drivers called Zero–delay Buffers make use of this occurance and can produce a clock edge at the output that is exactly in phase with the input.

**Skew**

Clock fanout buffers and PLL clock drivers with built–in fanout buffers offer multiple outputs. These clock outputs are routed across a PC board to various devices. A typical fanout buffer may have as many as 18 to 20 clock outputs. Typically, these

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outputs are designed to drive a 50 ohm cable or a 50 ohm PC board trace. Ideally, all of the outputs are timed such that clock edges on each output switch at exactly the same time. However, real life devices do not. Small amounts of skew exist between the high to low or low to high transition on one output as compared to another output. For systems that require synchronization between data and clocks or multiple clocks on the PC board, this skew is a bad thing. Clock integrated circuit designers try to minimize the amount of skew in a device. However, skew does exist and the device data sheet usually specifies the amount of skew.

This output skew is typically defined in three ways: output–to–output, process, or part–to–part skew.

Output–to–output skew is defined as the skew between the various output edges on a single device. Process skew is defined as the skew between the same output pin on two different devices. Finally, the part–to–part skew is defined as the skew between any output on two different devices. Figure 5 illustrates output skew types for both single–ended and differential output waveforms. Typically, both output–to–output and part–to–part skew are specified on a data sheet. The JEDEC specification states that the skew values are to be determined with the outputs driving identical specified loads.

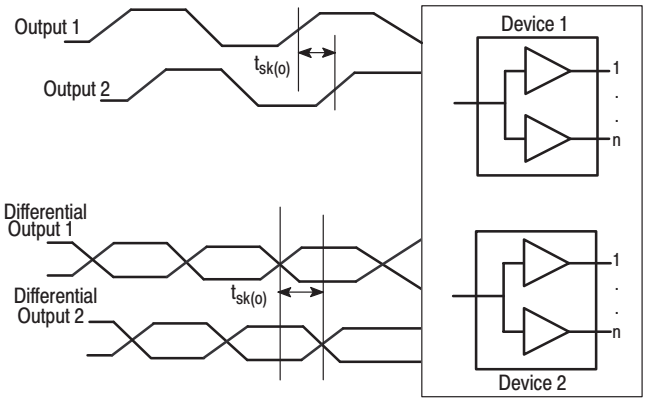


**Figure 5. Output–to–Output Skew**

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## Jitter

Jitter is a deviation of the edge location on the output of the clock buffer. As with skew, jitter is a bad thing and is usually measured in picoseconds. There are three categories of jitter that are of interest: cycle–to–cycle, period, and phase jitter.

Cycle–to–cycle jitter is the difference in the period of any two adjacent clock cycles. The difference is reported as an absolute value according to the JEDEC specification. However, quite often a ± value is used. The JEDEC symbol for cycle–to–cycle jitter is $t_{jit(cc)}$. Cycle–to–cycle is usually measured over some large sampling of cycles and specified as the maximum difference. Figure 6 shows the measurement and calculation of cycle–to–cycle jitter.

In PLL based systems, the value of the cycle–to–cycle jitter is usually small since the PLL does not quickly respond to changes on its input. Since cycle–to–cycle jitter is the difference in the period from one cycle to the next, this jitter is at the clock frequency. This jitter is also referred to as short term jitter.

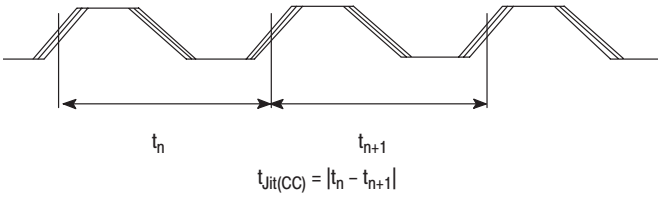


**Figure 6. Cycle–to–Cycle Jitter**

Clock integrated circuits have an inherent jitter generated within the device. In addition, external sources contribute to this jitter. Specifically, power supply noise may be a source of jitter in both PLL based and non–PLL based clock driver devices. Power supply design, power supply filtering, and board layout contributes to the overall jitter values measured on the output of the clock device.

The second type of jitter is period jitter, which is defined in the JEDEC specification as the deviation in cycle time of a signal with respect to an ideal period. Figure 7 shows the definition and calculation of period jitter. This jitter type is reported as an absolute maximum value as measured over a long time period. The JEDEC symbol for period jitter is $t_{jit(per)}$. The long time period varies from measurement system to measurement system. Typical time periods are 64 microseconds which, at a frequency of 100 MHz or so, yields many (6400) clock cycle period values. This type of jitter represents the random movement in the instantaneous output frequency or output period of the clock source.

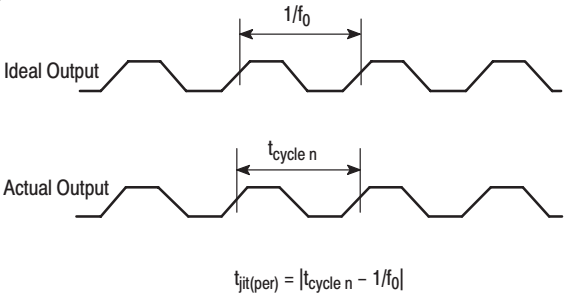


**Figure 7. Period Jitter**

The last jitter type covered is that of phase jitter. Phase jitter is associated with PLL based clock drivers. The JEDEC specification notation is $t_{jit(\phi)}$. This value represents the input to output jitter associated with a PLL clock driver. The value is given as an absolute value of the range or variation in the difference between the phase of the reference input and the phase of the feedback input to the integrated circuit. (See Figure 8)

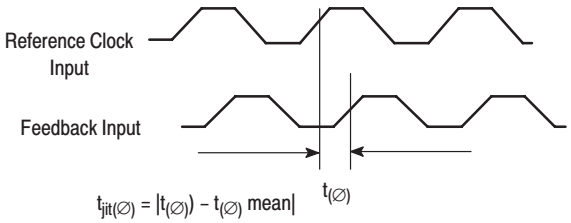


**Figure 8. Phase Jitter**

### Jitter Values and Data Sheets

Definitions of the various types of jitter and the equations for calculating the values are necessary for an understanding of

jitter and how it relates to a clock design. However, another important factor in understanding clock drivers is the metrics and methods used of the published specifications. These metrics may vary from manufacturer to manufacturer and also within a manufacturer's clock driver offering. The values may be given as RMS values or as a peak–to–peak value. They may be listed as typicals or as actual maximum values. Understanding of the background of the jitter values on a data sheet are necessary for circuit design as well as comparing clock driver devices.

Jitter measurements, whether cycle–to–cycle period or phase, are measured over some large number of samples. The data for a typical device, when plotted, represents a classic distribution Gausian or bell shaped curve where most of the clock cycles are close to the ideal frequency (in the case of period jitter) with fewer and fewer devices having increasing deviation from the ideal period.

In classical statistics, the distance from the center of the Gausian curve is defined in values of standard deviation or sigma; and the higher the sigma multiplier, the higher the confidence level is that a device will not exhibit a jitter value greater than a predefined amount.

Data sheet specifications that list RMS values imply a 1 sigma deviation above the mean and 1 sigma deviation below the mean or a total of 2 sigma confidence level. Table 1 lists these confidence factors for ±1 sigma through ±6 sigma. If data sheet values are specified as RMS values and higher levels of confidence are desired, then the data sheet values for jitter must be multiplied by the desired confidence factor.

Figure 9 shows the Gausian distribution curve and sigma points for a device with an output frequency of 400 MHz (period of 2.5 ns). A value of ±3 sigma or 6 sigma gives a confidence level or a probability that the clock edge is within the distribution of 0.9970007%. The ±3 sigma limits define the upper period limit of approximately 2.52 ns and the lower period limit of approximately 2.48 ns.

Figure 10 shows actual measurements made for the period jitter of a 400 MHz clock device.

In this example, the mean period is 2.49921 ns (approximately 2.5 ns) with the standard deviation being 6.48 ps and the peak–to–peak jitter being 57 ps. This data was captured with a sample size of 13100 samples.

**Table 1. Confidence Factor**

| Sigma | Value | Confidence Factor |
|---|---|---|
| ±1 | (2 sigma) | 0.68268948 |
| ±2 | (3 sigma) | 0.95449988 |
| ±3 | (6 sigma) | 0.99730007 |
| ±4 | (8 sigma) | 0.99993663 |
| ±5 | (10 sigma) | 0.99999943 |
| ±6 | (12 sigma) | 0.99999999 |

RMS values for jitter look better on the data sheet than peak–to–peak. However, peak–to–peak values may be needed for clock jitter analysis. If RMS values are specified, peak–to–peak values may be derived based upon the required system reliability for the specific applications. If the other cases where peak values are specified, these values may be used directly. However, the question that must be asked in order to use the manufacturer's peak–to–peak values is what level of uncertainty is being specified. These parameters may be specified differently on each manufacturer data sheet. Therefore, care must be taken to insure that when one is comparing values, the values are specified and measured in a similar fashion.

The above discussion assumes the jitter measurements have the classic Gausian curve or statistical distribution. This would be the case if the jitter is completely random. However, clock driver devices may have internal mechanisms that produce jitter that deviates from the classic bell curve. In this case, the total jitter is composed of the addition of a series of bell curves providing a more complex distribution. With care, the terms of RMS and the various sigma levels may still apply.

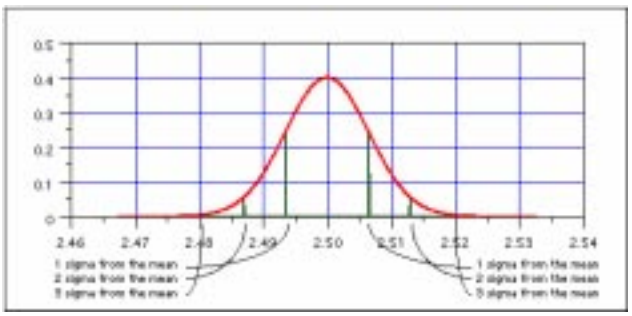


**Figure 9. Classic Gausian Distribution Curve**

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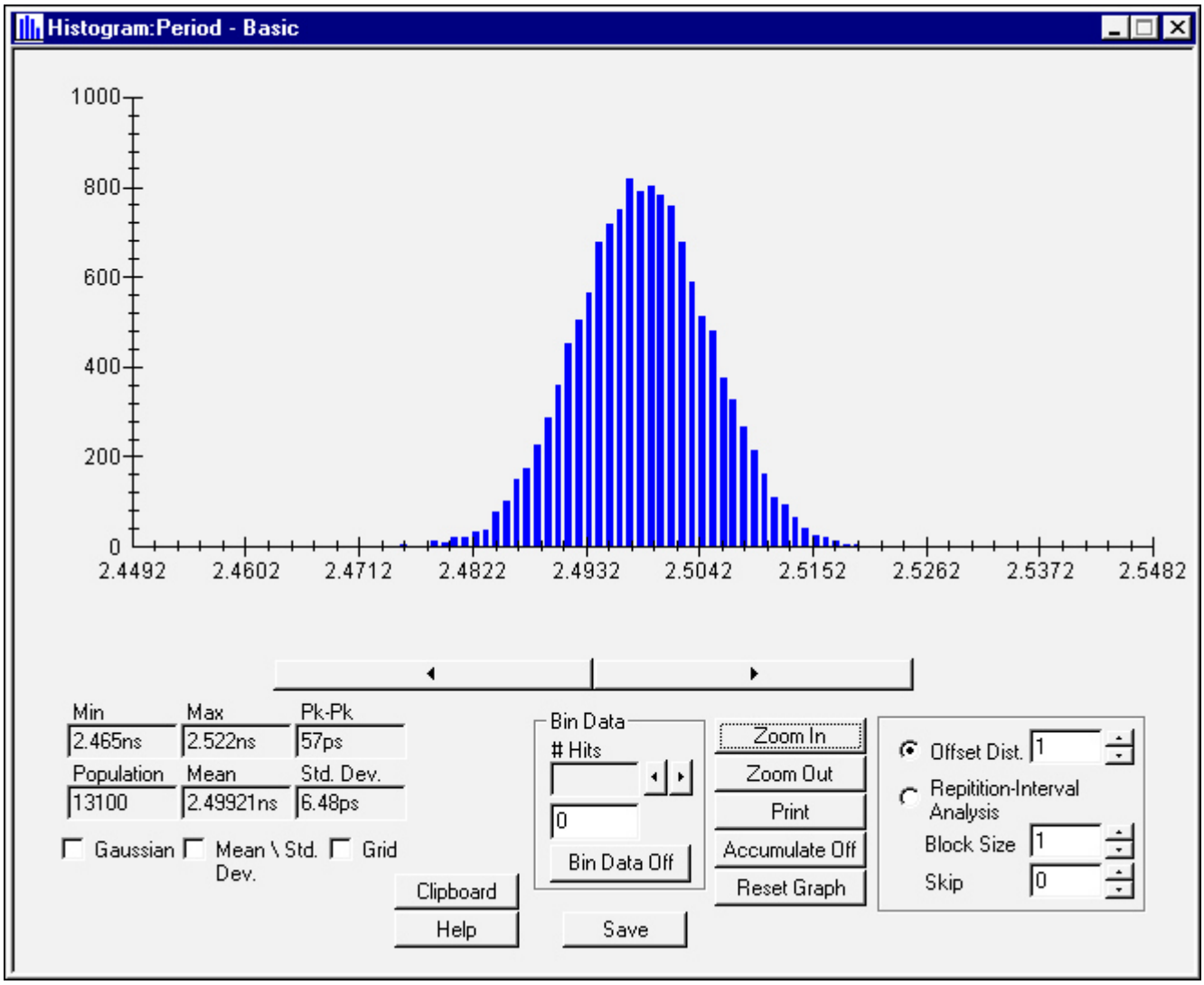


**Figure 10. Period Jitter for Typical PLL Clock Device with $F_{OUT}$ = 400 MHz**

**PLL Bandwidth and Jitter**

The PLL based clock driver locks on to a reference frequency and maintains an output frequency based upon that reference frequency. If the reference frequency changes, the PLL attempts to follow the change in the reference frequency. However, if the change is faster than the PLL can follow, the PLL based clock driver acts as a low pass filter and ignores or effectively filters out the higher frequency changes on its input. As with any low pass filters, the PLL has a cutoff frequency, or bandwidth, associated with it. This bandwidth becomes important to our clock tree design. High frequency noise and jitter will not pass through the PLL.

The actual bandwidth of the locked PLL is dependent on many factors, including the feedback divider ratio. The higher the divide ratio, the lower the bandwidth. Thus, those PLL clock driver devices that have selectable feedback divide ratios will have varying bandwidth values. Bandwidth may or may not be specified by the PLL clock driver manufacturer. If not specified, the information is usually available on request.

Figure 11 is a typical PLL frequency modulation bandwidth waveform. Note the cutoff frequency is about 300 kHz. As mentioned before, the cutoff frequency will vary with a change in the divide ratio in the feedback loop. Bandwidths of PLL–based clock drivers vary from low values of a few kHz to higher values of a MHz or more depending upon the intended application of the device. Clock synthesizers typically have the lowest bandwidth. Bandwidths of these devices are in the order of 30 to 50 kHz. Clock generators are next with bandwidths of a few hundred kHz. The devices with the highest bandwidth are the Zero–Delay–Buffers. The bandwidths of these devices are typically a MHz and above.

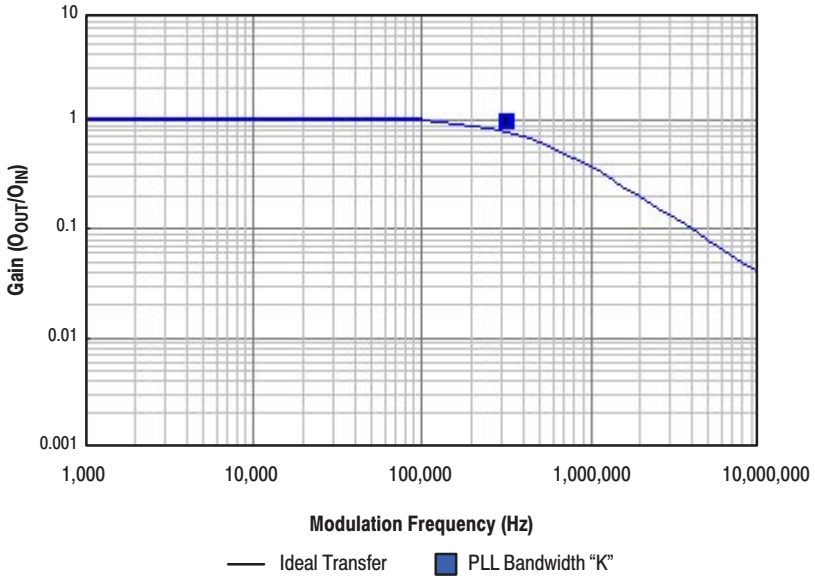


**Figure 11. PLL Bandwidth**

### Clock Tree Application Example Analysis

Figure 12 shows an example clock tree application which is used to show the effects of skew and jitter in a system. The goal of this design is to provide multiple phase aligned HSTL and LVCMOS outputs. The reference for this clock tree is a crystal oscillator while the outputs of the tree provide both HSTL and LVCMOS to various system locations. The tree starts with a crystal oscillator in the MC12430 integrated circuit. The MC12430 is a PLL based clock synthesizer that allows very fine control of the output frequency in 1 MHz steps.

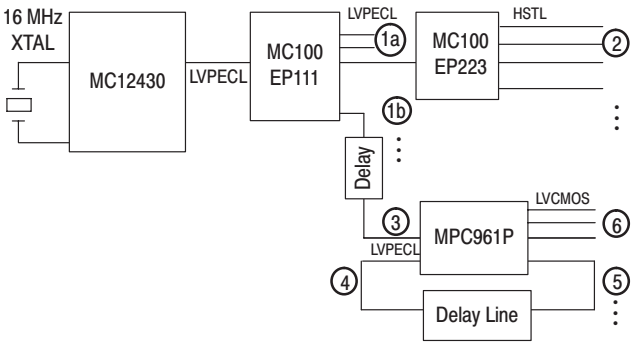


**Figure 12. Example Clock Tree**

The LVPECL output of the MC12430 drives the LVPECL input to the MC100EP111 fanout buffer.

The MC100EP111 consists of 10 LVPECL differential pairs of which one pair is connected to a MC100EP223 input and another pair connected to the MPC961P input. The MC100EP223 fanout buffer provides HSTL outputs while the MPC961P is a PLL–based clock generator that provides several LVCMOS outputs. Notice there is an introduced delay from the LVPECL output of the EP111 to the LVPECL input of the MPC961P zero–delay buffer. This introduced delay is due to backplane or cable distance which will skew the LVCMOS outputs to later than the HSTL outputs. To compensate for this delay, the MPC961P zero–delay buffer is used in conjunction with a PC board delay line in the feedback path.

Figure 13 provides an analysis of the example clock tree for the situation where we have no (or choose to ignore both) jitter and skew in the devices. Later, in Figure 14, an analysis with both jitter and skew is shown. The circled numbers in Figure 12 are used as reference points on the clock analysis waveforms.

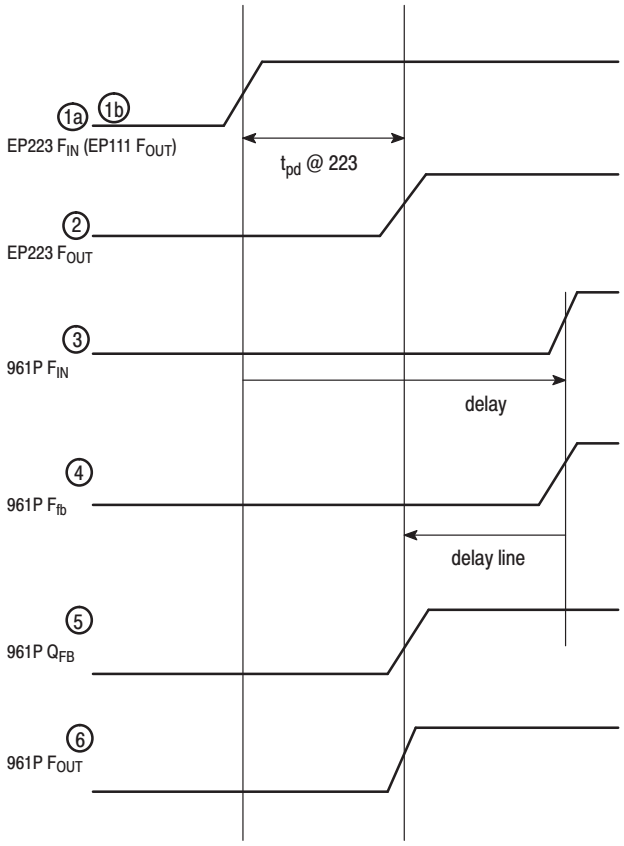


**Figure 13. Example Clock Tree Analysis without Jitter and Skew**

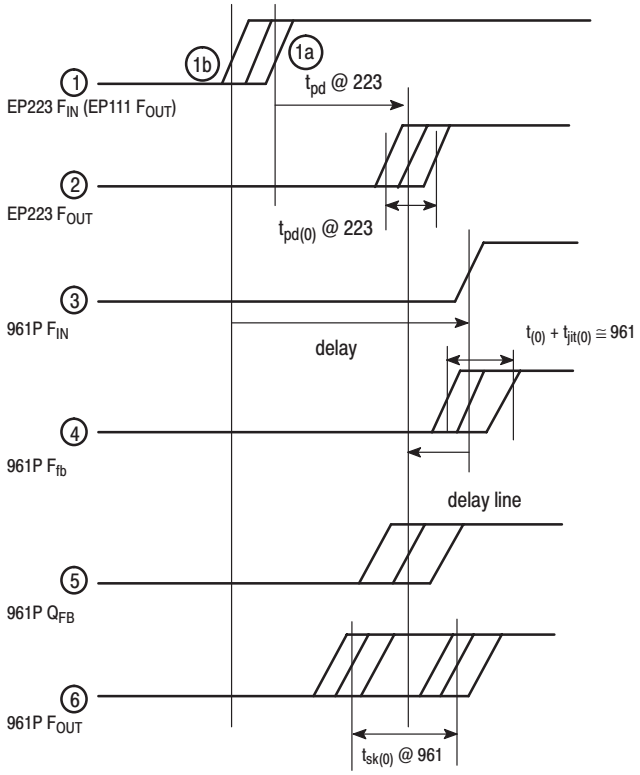


**Figure 14. Example Clock Tree Analysis with Jitter and Skew**

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The first analysis of the clock tree is with the assumption that there is zero output–to–output skew and zero jitter. With zero skew between the outputs of the MC100EP111, the signals 1a and 1b are identical. The waveform at point 2 is delayed due to propagation delay, $t_{pd}$, of the MC100EP223.

The waveform at point 3 is delayed due to the delay associated with the backplane or cable distribution. By using the MPC961P zero–delay buffer and placing the appropriate trace delay in the feedback path of the PLL, we can compensate for the backplane trace and bring the waveform for points 5 and 6 back in line with the output of the MC100EP223.

Next, we will do the same analysis but we will include the output skew on the MC100EP111, the MC100EP223, and the phase jitter for the MPC961. (See Figure 14.)

Initially, we have the output–to–output skew for the EP111. We will assume that the output connected to the MC100EP223 is the slowest and thus the longest delay output and that the output connected through the delay line to the input of the MPC961C is the fastest or shortest delay output. This analysis must also be done for the opposite situation; where the MPC961P is connected to the slowest output and the MC100EP223 is connected to the fastest output.

The waveform at point 2 is delayed from point 1a by the propagation delay, $t_{pd}$, of the MC100EP223 as we had in Figure 13. However, by including the output–to–output skew for the MC100EP223, we find uncertainty in the location of point 2 as shown in the waveform of point 2 of Figure 14.

Point 3 shows the waveform arriving at the input to the MPC961P. Point 4 is the feedback input to the MPC961P and, in the ideal case, is exactly the same as point 3. However, in this situation, we have the uncertainty caused by the combination of the static phase offset, $t_{(\phi)}$ and the phase jitter for the MPC961P. Figure 14 depicts these two values added together. The waveform of point 5 now moves back in time due to the delay line in the feedback path of the PLL such that the nominal output now coincides with the HSTL outputs of point 2. Point 6 shows the added uncertainty of the outputs due to the output–to–output skew from the MPC961P. Note that Figure 14 is not to scale and the magnitudes of the skew and jitter are actually much smaller than indicated.

Table 2 lists the skew and jitter values for the 3 devices used in the example. The MC100EP111 has a specification for output–to–output skew. The MPC961P has parametric values for Static Phase Offset, phase jitter and output–to–output skew. The MC100EP223 has values for propagation delay and output–to–output skew.

**Table 2. Confidence Factor**

| Device | Parameter |
|---|---|
| MC100EP111 | tsk(o): 70 ps |
| MPC961P | $t_{(\varnothing)}$ : –50 to 225 ps<br>$t_{jit(\varnothing)}$ ÂF ~ 100 ps<br>$t_{sk(o)}$ ÂFÂ @ 150 ps |
| MC100EP223 | $t_{pd}$: estimated 700 ps<br>$t_{sk(o)}$: estimated 50 ps |

A similar analysis can be done for the case where the MC100EP111 outputs connected to the MC100EP223 and MPC961P are reversed in time. Thus, the MC100EP111 output connected to the MC100EP223 is the fastest and the output connected to the MPC961P is the slowest.

One last comment on the example is that the jitter associated with the clock source, MC12429, was not mentioned in the analysis. This value was ignored for this example due to the fact that all of the clock outputs are derived from the same source, and jitter that occurs on one output would show up on all outputs. Applications that have clock outputs derived from different sources, or have the clock source compared to a frequency standard, would mandate the need to include the source jitter in the analysis.

## SUMMARY

Skew and jitter are real characteristics of clock driver devices and may or may not be of importance to a clock tree design. Understanding data sheet values and applying this knowledge to clock tree design can sometimes be a real challenge. With a bit of analysis, one can determine which parameters are critical to a specific clock tree design and be able to compare the values of these parameters from one device/vendor to another. Lastly, data sheet values of jitter are often measured in a lab environment under the best of conditions. Real designs with clock drivers on PC boards with other digital circuitry, noisy power supplies, long traces, and other clock sources can make the overall jitter worse. Careful design practices are a must for the best clock driver design.

# Chapter Nine

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9

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